MOSFET – Dual P-Channel POWERTRENCH®

-30 V, -3.3 A, 87 mΩ

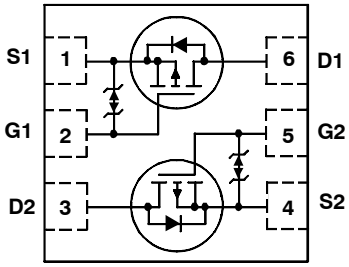
FDMA3027PZ, FDMA3027PZ-F130

WDFN6 2X2, 0.65P
CASE 511DA

Description

This device is designed specifically as a single package solution for dual switching requirements such as gate driver for larger Mosfets. It features two independent P−Channel MOSFETs with low on−state resistance for minimum conduction losses.

The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications. G−S zener has been added to enhance ESD voltage level.



Features

- Max $R_{DS(on)}$ = 87 mΩ at V_{GS} = −10 V, I_D = −3.3 A
- Max $R_{DS(on)}$ = 152 mΩ at V_{GS} = −4.5 V, I_D = −2.3 A
- HBM ESD Protection Level > 2 kV Typical (Note 3)
- Low Profile − 0.8 mm Maximum − in the New Package MicroFET 2x2 mm
- These Devices are Pb−Free and are RoHS Compliant

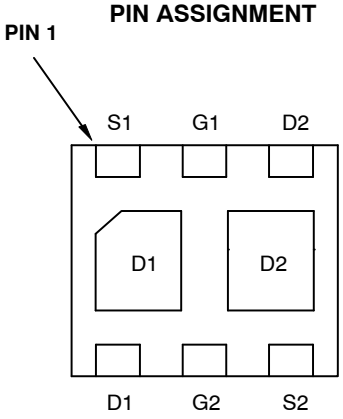
Typical Applications

- Load Switch
- Discrete Gate Driver

MARKING DIAGRAM

Z	= Assembly Plan Code
XY	= Date Code (Year & week)
KK	= Lot Run Traceability Code
327	= Specific Device Code

PIN ASSIGNMENT



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	−30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current −Continuous (Note 1a)	−3.3	A
	−Pulsed	−15	
P_D	Power Dissipation (Note 1a)	1.4	W
	Power Dissipation (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1a)	86	°C/W
	Thermal Resistance for Single Operation, Junction to Ambient (Note 1b)	173	°C/W
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c)	69	°C/W
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d)	151	°C/W
	Thermal Resistance for Single Operation, Junction to Ambient (Note 1e)	160	°C/W
	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1f)	133	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

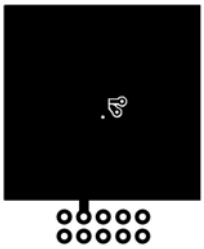
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−30	−	−	V
$\frac{\Delta BV_{DSS(th)}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	−22	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V	−	−	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V	−	−	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−1	−1.9	−3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	5	−	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −3.3 A	−	69	87	mΩ
		V_{GS} = −4.5 V, I_D = −2.3 A	−	108	152	
		V_{GS} = −10 V, I_D = −3.3 A, T_J = 125°C	−	97	122	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −3.3 A	−	6	−	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f =1 MHz	−	324	435	pF
C_{oss}	Output Capacitance		−	59	80	pF
C_{rss}	Reverse Transfer Capacitance		−	53	80	pF
R_g	Gate Resistance		−	12	−	Ω
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −15 V, I_D = −3.3 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	−	5.2	11	ns
t_r	Rise Time		−	3	10	ns
$t_{d(off)}$	Turn−Off Delay Time		−	17	31	ns
t_f	Fall Time		−	11	25	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to −10 V, V_{DD} = −15 V, I_D = −3.3 A	−	7.2	10	nC
		V_{GS} = 0 V to −5 V, V_{DD} = −15 V, I_D = −3.3 A	−	4.1	6	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −15 V, I_D = −3.3 A	−	1.0	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	1.9	−	nC

ELECTRICAL CHARACTERISTICS (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain−Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −3.3 A (Note 2)	−	−0.94	−1.3	V
t_{rr}	Reverse Recovery Time	I_F = −3.3 A, di/dt = 100 A/μs	−	20	32	ns
Q_{rr}	Reverse Recovery Charge		−	10	18	nC

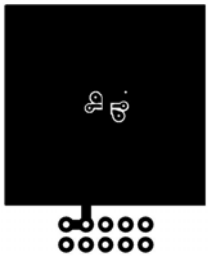
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a) $R_{\theta JA}$ = 86°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
   (b) $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   (c) $R_{\theta JA}$ = 69°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
   (d) $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.
   (e) $R_{\theta JA}$ = 160°C/W when mounted on a 30 mm^2 pad of 2 oz copper. For single operation.
   (f) $R_{\theta JA}$ = 133°C/W when mounted on a 30 mm^2 pad of 2 oz copper. For dual operation.



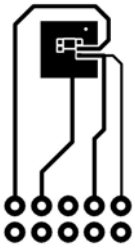
a. 86 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 173 °C/W when mounted on a minimum pad of 2 oz copper

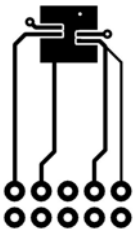


c. 69 °C/W when mounted on a 1 in^2 pad of 2 oz copper

d. 151 °C/W when mounted on a minimum pad of 2 oz copper



e. 160 °C/W when mounted on 30 mm^2 pad of 2 oz copper



f. 133 °C/W when mounted on 30 mm^2 pad of 2 oz copper

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
3. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

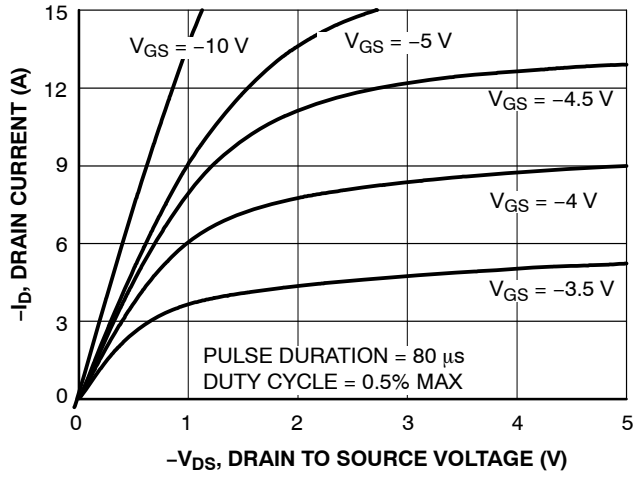


Figure 1. On−Region Characteristics

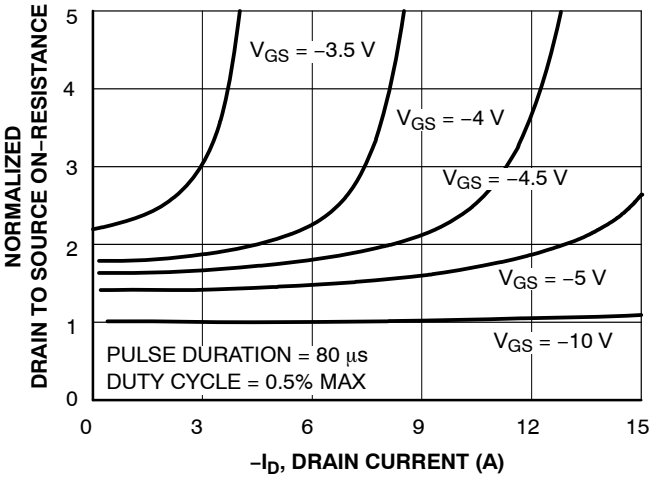


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

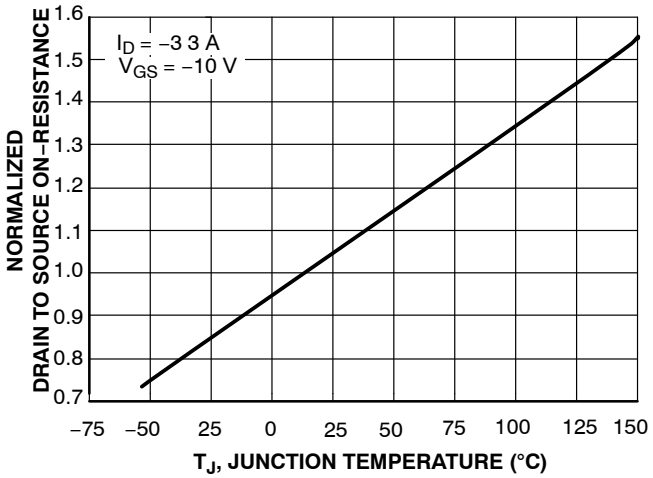


Figure 3. Normalized On−Resistance vs Junction Temperature

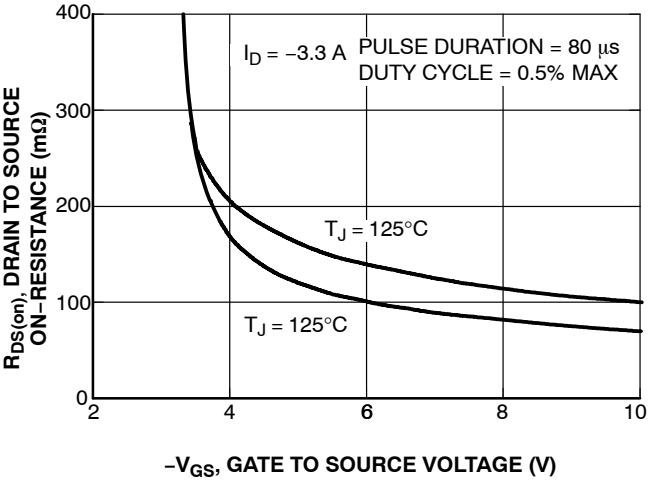


Figure 4. On−Resistance vs Gate to Source Voltage

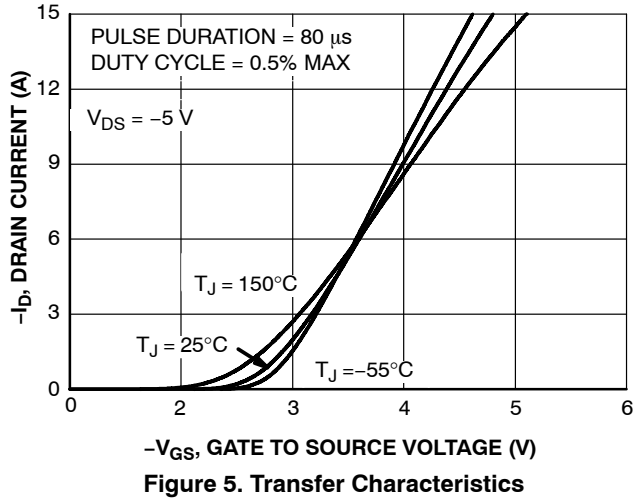


Figure 5. Transfer Characteristics

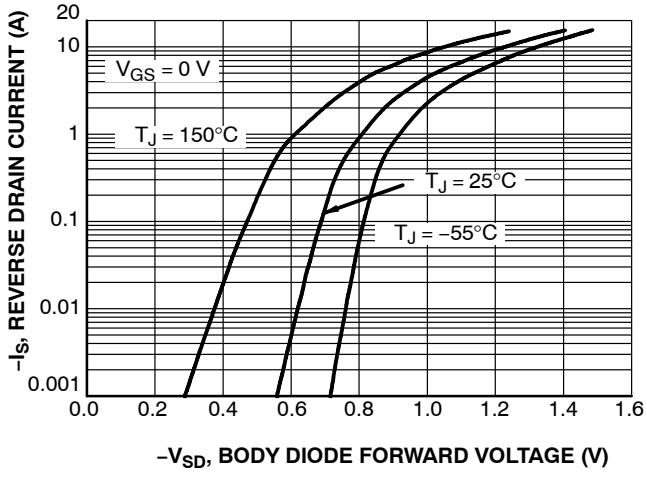


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

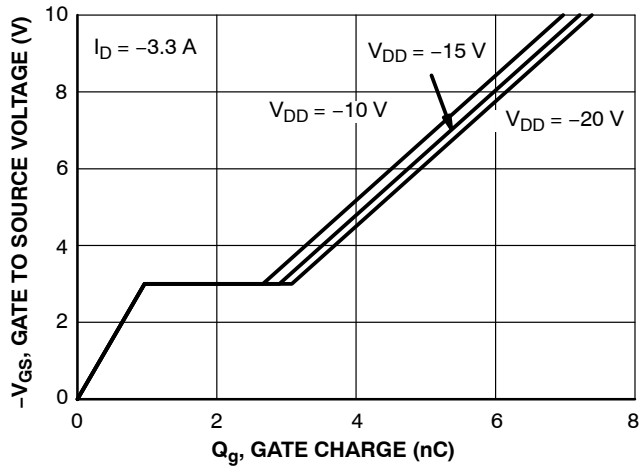


Figure 7. Gate Charge Characteristics

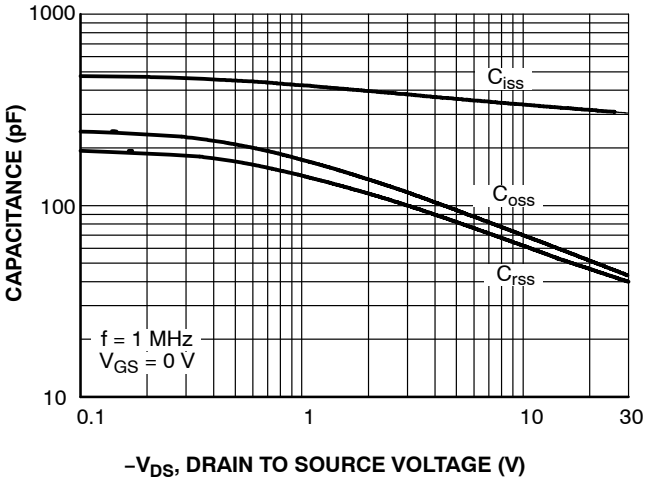


Figure 8. Capacitance vs Drain to Source Voltage

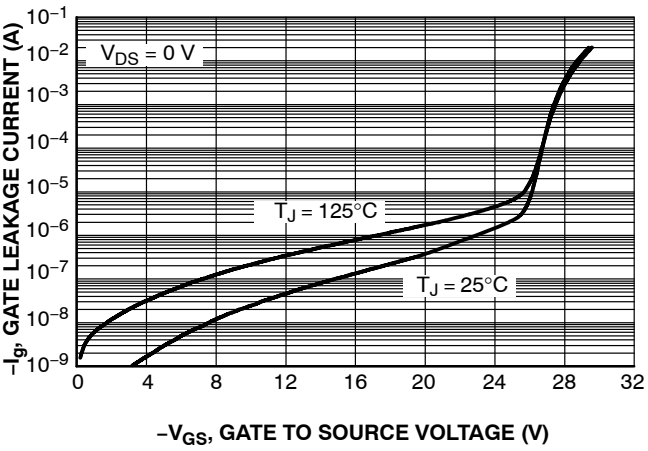


Figure 9. Gate Leakage Current vs Gate to Source Voltage

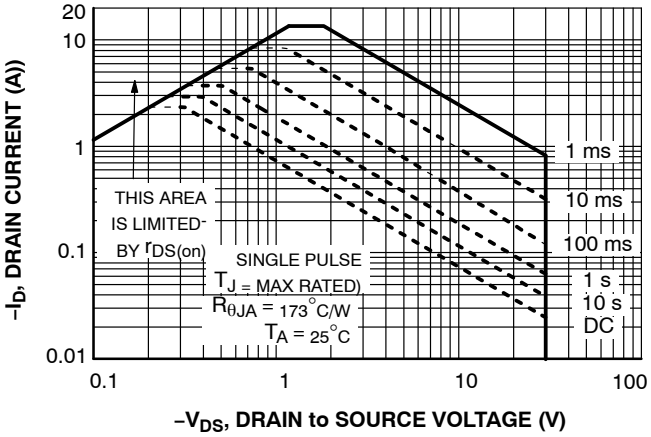


Figure 10. Forward Bias Safe Operating Area

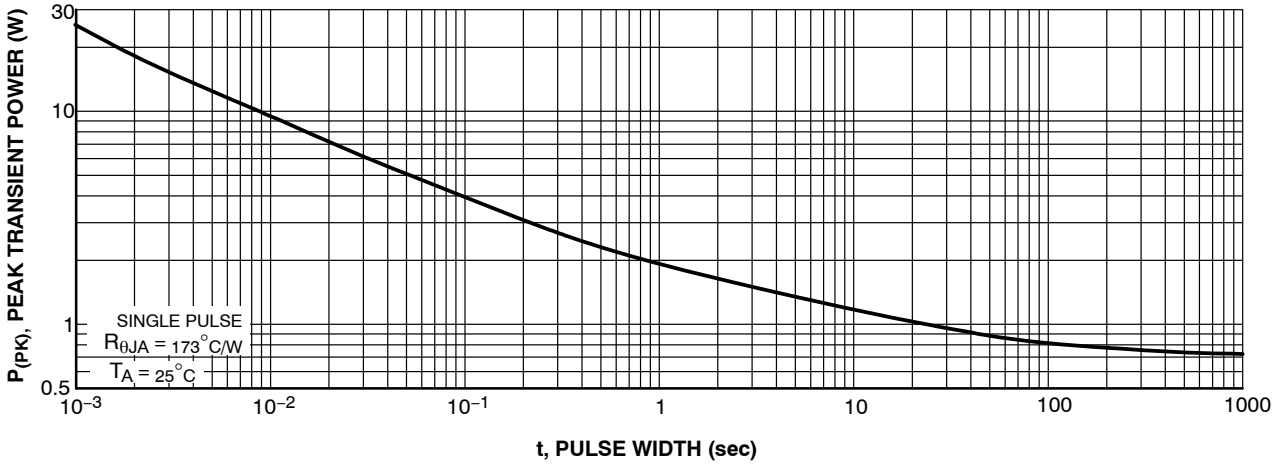


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

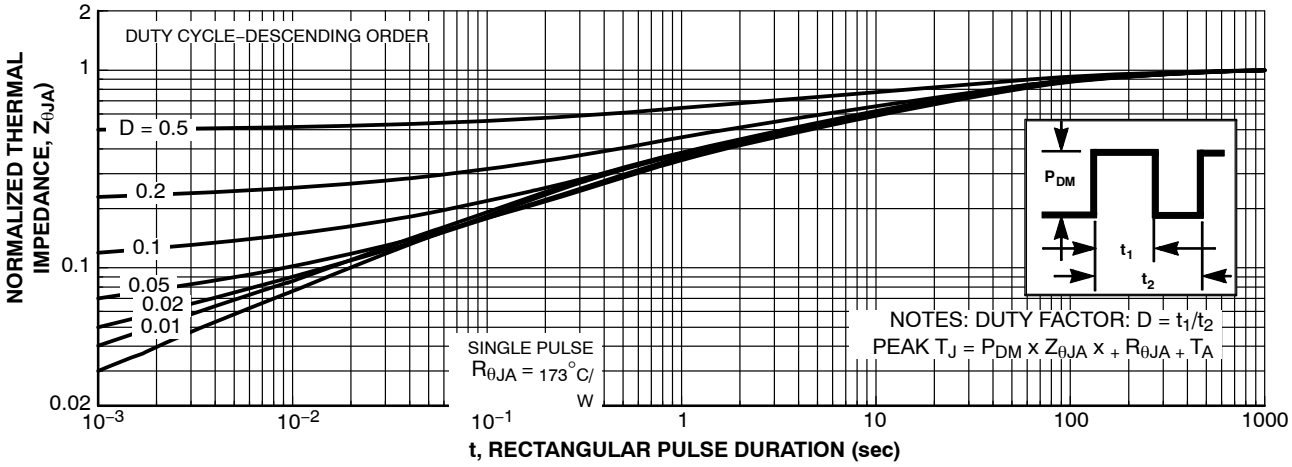


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

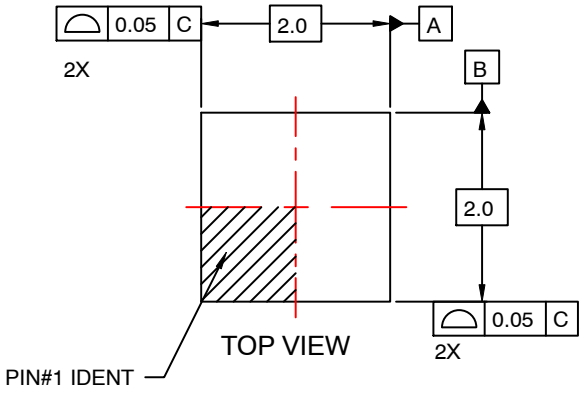
ORDERING INFORMATION

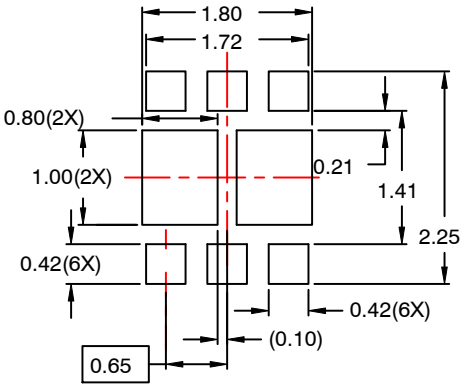
Device Order Number	Package Type	Pin 1 Orientation in Tape Cavity	Shipping†
FDMA3027PZ	WDFN−6 (Pb−Free/Halide Free)	Top Left	3000 / Tape and Reel
FDMA3027PZ−F130	WDFN−6 (Pb−Free/Halide Free)	Top Right	3000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

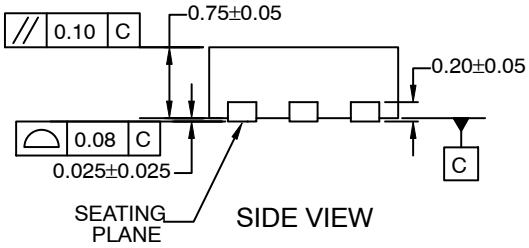
WDFN6 2x2, 0.65P
CASE 511DA
ISSUE O

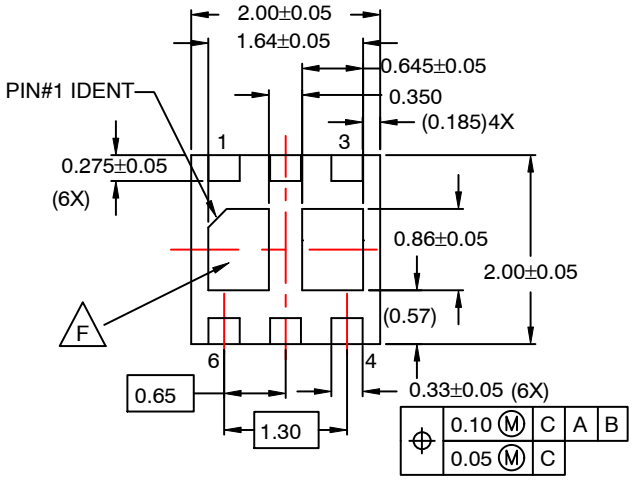
DATE 31 JUL 2016





RECOMMENDED
LAND PATTERN





BOTTOM VIEW

NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO−229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

F. NON−JEDEC DUAL DAP

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