1. DESCRIPTION

The 7705B is a 16-bit A/D converter chip mainly used for low-frequency measurements, which can directly convert tiny signals measured by sensors to A/D.

The 7705B has two fully differential channels and utilizes SPI 3-wire serial communication. Built-in configurable analog front-end gain, signal polarity, and update rate. Features self-calibration and system calibration, gain as well as offset errors in the device itself and in the system can be eliminated.

The 7705B also features high resolution, excellent noise immunity, and low voltage and power consumption, making it ideal for instrumentation, industrial control, and other applications.

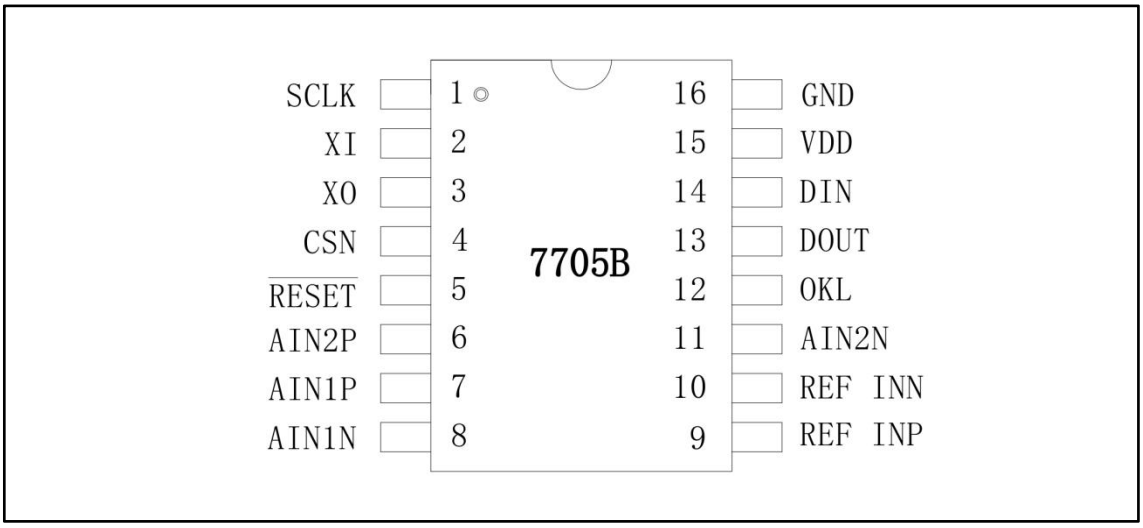
2. FEATURES

- ADC with Dual Fully Differential Input Channels
- 16-bit Σ-Δ analog-to-digital conversion
- Integral nonlinearity less than 0.01%
- 1～128 Programmable gain: 1 to 128
- Three-wire serial communication
- Buffering capability for analog inputs
- 3V or 5V operating voltage, ±5% range
- Maximum power consumption of 1mW at 3V
- 8μA Power-down mode, current maximum of 8μA
- Package Format DIP-16(XD7705B), SOP-16W(XL7705B)

3. APPLICATION

- Pressure gauges
- Temperature measuring equipmen
- Microcontrol system
- Weather sounder

4. PIN CONFIGURATIONS AND FUNCTIONS



DIP-16/SOP-16W

Pin Functions

NO.	PIN	I/O	DESCRIPTION
1	SCLK	I	Serial Clock Input
2	XI	I	Clock input, crystal or external clock
3	XO	O	clock output
4	CSN	I	Chip select, input active low
5	$\overline{\text{RESET}}$	I	Reset, active low
6	AIN2P	I	Differential analogue positive input for channel 2
7	AIN1P	I	Differential analogue positive input for channel 1
8	AIN1N	I	Differential analogue negative input for channel 1
9	REF INP	I	Positive input for reference voltage
10	REF INN	I	Negative input for reference voltage
11	AIN2N	I	Differential analogue negative input for channel 2
12	OKL	O	AD conversion completion logic output flag bit
13	DOUT	O	Serial data output
14	DIN	I	Serial data input
15	VDD	-	Power supply
16	GND	-	Ground pin

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

（TA = +25℃， Unless otherwise stated）

PARAMETER	SYMBOL	VALUE	UNIT
Logic Supply Voltage	VDD	-0.3V ～7	V
Analogue input voltage	Vin	-0.3 ～V_{DD}+0.3	V
Digital Input Voltage			
Digital output voltage	Vout	-0.3 ～V_{DD}+0.3	V
Operating Temperature Range	Topr	-40～85	℃
Storage temperature range	Tstg	-45～125	℃
Junction temperature	Tj	125	℃
Electrostaticdischarge (ESD)	Human-body model（HBM）	2000	V

5.2. Electrical Characteristics

（Unless otherwise stated，VDD=+5V，REF =2.5V；TA=25℃ ）

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Guaranteed filter trap <60hz		16		Bits
Integral nonlinearity			0	0.01%	%of FSR
Unipolar misalignment drift			0.5		μV/℃
Bipolar zero drift	PGA=1-4		0.5		μV/℃
	PGA=8-128		0.1		μV/℃
Full scale drift			0.5		μV/℃
Gain Error Drift			0.5		ppm of FSR/ ℃
Bipolar negative full scale error		0	-	0.01%	%of FSR/℃
Bipolar negative full scale drift			1		μV/℃
			0.6		μV/℃
REF IN Absolute/Common ModeVoltage		0		V_{DD}	V
AIN Absolute/Common Mode Voltage	BUFEN=0	-0.03		V_{DD}+0.03	V
	BUFEN=1	0.05		V_{DD}-1.5	V
AIN Input Current				1	nA
AINAcquisition Capacitance				10	pF
AIN Differential voltage	Unipolar input	0		V_{REP}/GAIN	
	Bipolar input	-V_{REP}/GAIN		V_{REP}/GAIN	
AIN Stable sampling rate	Gain1-4	GAIN×f_{CLKIN}/64			
	Gain8-128	f_{CLKIN}/8			
REFINP—REFINN Difference	VDD=3V,Vref=1.225V	1		1.75	V
	VDD=5V,Vref=2.5V	1		3.5	
REF INN Input Stable Sampling sample rate			f_{CLKIN}/64		

Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIL	V_{DD}=5V			0.8	V
	V_{DD}=3V			0.4	V
VIH		2.0			V
Schmitt trigger input (SCLK)					
V_{T+}	V_{DD}=5V	1.4		3	V
V_{T-}		0.8		1.4	
V_{T+}—V_{T-}		0.4		0.8	
V_{T+}	V_{DD}=3V	1		2.5	
V_{T-}		0.4		1.1	
V_{T+} V_{T-}		0.375		0.8	
XI					
Input Low Level	V_{DD}=5V			0.8	V
Input High Level		3.5			
Input Low Level	V_{DD}=3V			0.4	
Input High Level		2.5			
Data output code	unipolar	Binary			
	bipolar	Biased binary code			

Power Supply Parameter Characteristics

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
	BUFEN	f_{CLKIN}（MHZ）	Gain				
At 3V supply voltage, the digital IO interface or control port is grounded or connected to VDD.（XI AND OSCDIS=1）							
Supply Current	0	1	1-128			0.32	mA
	1	1	1-128			0.6	
	0	2.4576	1-4			0.4	
	0	2.4576	8-128			0.6	
	1	2.4576	1-4			0.7	
	1	2.4576	8-128			1.1	
At 5V supply voltage, the digital IO interface or control port is grounded or connected to VDD.（XI AND OSCDIS=1）							
Supply Current	0	1	1-128			0.45	mA
	1	1	1-128			0.7	
	0	2.4576	1-4			0.6	
	0	2.4576	8-128			0.85	
	1	2.4576	1-4			0.9	
	1	2.4576	8-128			1.3	
Power-down mode current	V_{DD}=5V, XI=0V /V_{DD}.					16	uA
	V_{DD}=3V，XI=0V / V_{DD}.					8	
Power Supply Rejection Ratio	Supply Voltage		Gain		86		dB
	VDD=3V		1				
	VDD=3V		2		78		
	VDD=3V		4		85		
	VDD=3V		8-128		93		
	VDD=5V		1		90		
	VDD=5V		2		78		
	VDD=5V		4		84		
	VDD=5V		8-128		91		

5.3. Timing Description

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	PARAMETER
Master Clock Frequency	f_{CLKIN}	-	400		2500	kHz
Master Clock Low Level Time	Tlow	t_{CLKIN}=1/ f_{CLKIN}	0.4*tCLKIN			ns
Master Clock High Time	Thigh		0.4*tCLKIN			ns
OKL High pulse	tO			500*tCLKIN		ns
$\overline{\text{RESET}}$ Pulse width	t_R		100			ns
Read-write timing						
CSN↓→SLCK First rising edge	Tcsn1		120			ns
Slck↓→DIN Effective acquisition interval	tdo	V_{DD}=5V	0	-	80	ns
		V_{DD}=3V	0	-	100	ns
SCLK↑→CSN↑C	Tcsn2		0			ns
Sclk↑Post-bus withdrawal time	tsout	V_{DD}=5V	10		60	ns
		V_{DD}=3V			100	ns
DIN efficiently→SCLK↑Acquisition time	tds		30			ns
DIN efficiently→SCLK↑Holding time	tdh		20			ns
OKL↓→ CSN↓Holding time	toc		0			ns
Clock Pulse width high (low) level	tspw		100			ns

6. FUNCTION DESCRIPTION AND TIMING DIAGRAM

The 7705B uses serial communication to perform on-chip register read/write operations. The serial interface consists of five signal interfaces: SCLK, DIN, DOUT, OKL and CSN, and the order of data transmission adopts the high bit first.

DIN ： Data input port, writes data on the rising edge of the clock.

DOUT： Data output port, outputs data on the falling edge of the clock.

SCLK： Read/write serial clock input.

OKL： Indication signal, indicates whether the data in the ADC result register is updated or not. A low level indicates that the ADC data has been converted and the ADC data can be read from the ADC result register. A high level indicates that the ADC is being converted or updated, and the data cannot be read at this time.

CSN： Chip Select Signal, only when CSN is first pulled down to enable, can the register be read or written, and CSN should be pulled up after reading or writing.

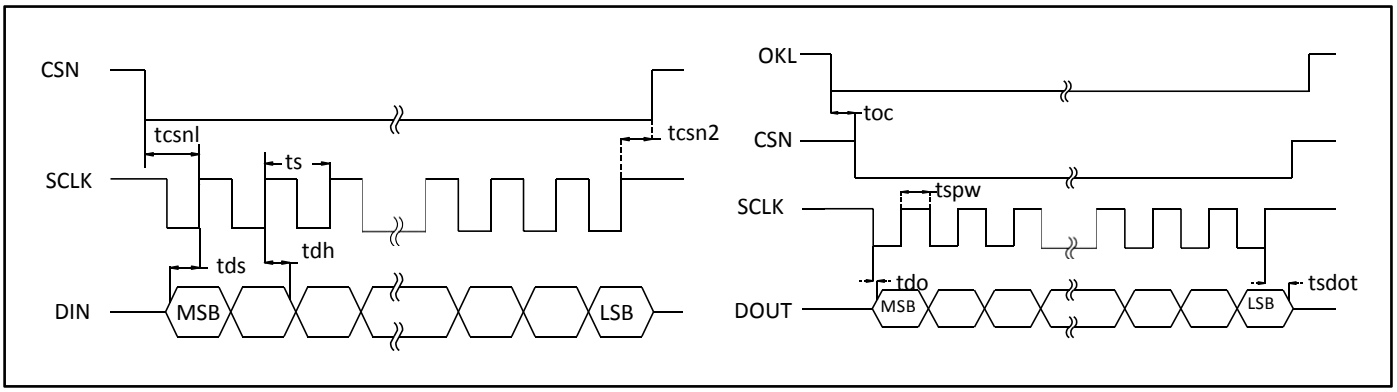


Figure 3 Write Timing

Figure 4 Read Timing

6.1. Register Descriptions

There are 8 registers inside the 7705B, the first one is the communication register, because any operation of the other registers must operate the communication register before the operation of its registers. The 7705B will be reset if more than 32 pulses are sent during a DIN high write operation.

Table 1 Communication Register 8-bit Description Power-up/reset status：00 Hex

MSB	**B7**	**0/OKL**	Chip reserved use bit. Default is "0", write "0" to write, don't write "1".		
	B6	**RSAD0**	Register address bits	000：Communication register 001：Configuration register 010：Frequency register 011：ADC Result register 100：Test Register 101：NC Register 110：Zero Offset Register 111：Gain Coefficient Register	
	B5	**RSAD1**			
	B4	**RSAD2**			
	B3	**R/WL**	The read/write select bit, "0" indicates that the operation is a write and "1" indicates that the operation is a read.		
	B2	**PD**	Write "1" for power down mode. Write "0" for normal operation mode.		
	B1	**CHH**	**0**	**0**	**1**
LSB	**B0**	**CHL**	**0**	**1**	**0**
	Channel Selection		AIN1	AIN2	AIN1N Internal short-circuit
	Calibrating register pairs		Register pair 0	Register Pair 1	Register pair 0

Table 2 onfiguration Register 8-bit Description Power-up/Reset Status: 01 Hex

MSB	**B7**	**MDH**	Working mode selection bit: 00：For normal working mode 01：For self-calibration 10：For zero offset system correction 11：For gain coefficient system correction						
	B6	**MDL**							
	/	**PGA Configure**	**1**	**2**	**4**	**8**	**16**	**32**	**64**	**128**
	B5	**PGA_2**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
	B4	**PGA_1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**
	B3	**PGA_0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
	B2	**U/**BL	Unipolar "1"+FSR output 0xFFFFH, ZERO=0x0000H, -FSR=Ox0000H, Bipolar "0"+FSR output 0xFFFFH, ZERO=0x8000H, -FSR=Ox0000H,						
	B1	**BUFEN**	Input buffer enable, "0" disable, internal buffer short circuit, "1" enable						
LSB	**B0**	**SYNC**	Filter Sync, default is 0, if "1" reset the modulator and digital filter. The ability to collect samples from analogue inputs from a known point in time to reach system synchronisation.						

Table 3 Frequency register 8-bit description Power-up/reset status：05 Hex

MSB	B7	Z0	To ensure correct operation, zeros must be written to these bits. Failure to do so results in unspecified operation of the device.						
	B6	Z1							
	B5	Z2							
	B4	OSCDIS	Clock Disable Bit. The default value is 0. A "1" indicates that XO is low to reduce power consumption.						
	B3	OSCDIV	Clock divider bit. oscdiv=1, the clock frequency at the XI pin is divided by 2 before it is used by the device.						
	OSC Clock		1MHz				2.4576MHz		
	Output Update Rate		20Hz	25Hz	100Hz	200 Hz	50 Hz	60Hz	250 Hz	500 Hz
	Filter -3dB Cutoff Frequency		5.24Hz	6.55Hz	26.2 Hz	52.4 Hz	13.1 Hz	15.7 Hz	65.5 Hz	131 Hz
	B2	OSC	0	0	0	0	1	1	1	1
	B1	DRH	0	0	1	1	0	0	1	1
LSB	B0	DRL	0	1	0	1	0	1	0	1

The ADC result register is a 16-bit read-only register used to store the latest conversion result, and the high bit comes out first when reading the data. **Power-up/reset status: 0000 Hex.**

The test registers are 8-bit registers used to test the device. It is recommended that the user does not change it arbitrarily. (Automatically set to all 0's at power-up or reset). **Power-Up/Reset Status： 00 Hex**

The Zero Offset Register is a 24-bit read/write register. 7705B has several independent sets of Zero Offset Registers, different input channels are responsible by the corresponding Zero Offset Registers. 24-bit data must be written before it can be transferred to the Zero Offset Register. **Power-Up/Reset Status：1F4000 Hex**

The gain factor registers are 24-bit read/write registers. 7705B has several independent sets of gain factor registers, and different input channels are handled by the corresponding gain factor registers. 24-bit data must be written before it can be transferred to the gain factor registers. **Power-Up/Reset Status： 5761AB Hex**

The Gain Coefficient Register and Zero Offset Register are used together to form a register pair, as described above in Communication Registers.

7. APPLICATION CIRCUITRY

The basic circuit diagram of the 7705B (Figure 5) shows the analogue voltages as +5V/3V; a precision +2.5V/1.225V reference provides the reference voltage for the device. On the digital signal side, the device is configured for three-wire operation with CSN ground.

A quartz crystal provides the master clock source; the resistance of R is 1MΩ, and the capacitance values of C1 and C2 are generally in the range of 30pF to 50pF.

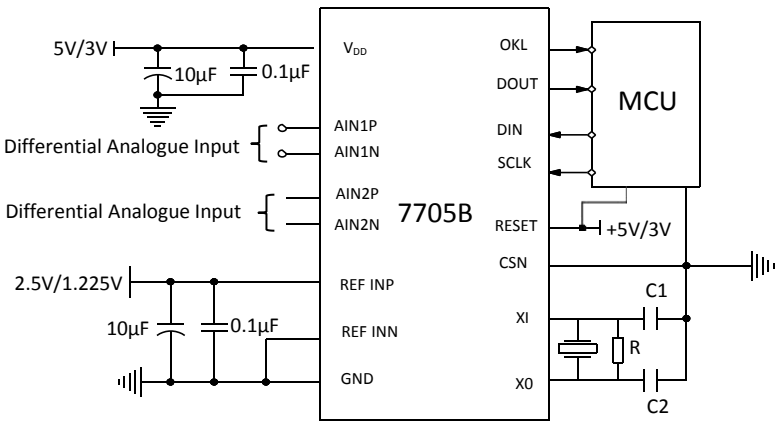


Figure 5 Circuit diagram of the 7705B

7.1. Ways to improve the accuracy of the 7705B in electronic scale applications

(1) When using a master clock of 2.4576MHz, it is strongly recommended to set the clock register to 84H, as shown in the table below：

ZO	Z1	Z2	OSCDIS	OSCDIV	OSC	DRH	DRL
1	0	0	0	0	1	0	0

At this time, the data output update rate is 10Hz, i.e., every 0.1S to output a new data.

(2) When the main clock is 1MHz, it is strongly recommended to set the clock register to 80H as shown in the table below:

ZO	Z1	Z2	OSCDIS	OSCDIV	OSC	DRH	DRL
1	0	0	0	0	0	0	0

At this time, the data output update rate is 4Hz, i.e., a new data is output every 0.25S.

7.2. Reset and power-down modes

The reset input circuit resets all logic, digital filters, and analogue modulators, while setting all on-chip registers to their default state. Reset is accomplished by pulling the RESET pin low or sending the RESET =0 instruction.

The PD bit in the Communicate register allows the user to set the device to operate in power-down mode to reduce power consumption, and when out of power-down mode, the device

After power-down mode, the device enters normal mode and all registers remain in the same state as before power-down mode without reconfiguration.

7.3. External Reference Voltage

REFINP and REFINN provide the differential reference voltage function for the 7705B. When operating with a 5V/3V supply voltage, the reference voltage is +2.5V/1.225V. When the reference voltage is less than 1V, the device can operate but the output noise becomes larger, resulting in a degradation of performance. Therefore, it is necessary to ensure that REFINP > REFINN to ensure that the device can work properly.

7.4. Error Calibration

When the ambient temperature, operating voltage, selected gain, filter traps, and unipolar/bipolar input range change. The device must be calibrated to ensure correct analogue-to-digital conversion.The 7705B has a variety of calibration options that can be programmed through the MDH and MDL bits of the configuration register. Calibration removes bias and gain errors generated on the device.

7.5. Self-Calibration

When the self-calibration command is sent, the chip performs zero offset correction and gain factor correction at the channel specified in the communication register and at the set gain. For zero offset correction, the input channel specified by the chip is automatically shorted internally (zero input); for gain factor correction, the input channel specified by the chip is connected to the internal Vref/voltage of the selected gain (full scale). After the calibration is completed, the values of the Zero Offset Register and the Gain Factor Register are automatically updated. Meanwhile, during the calibration process, OKL is kept high, when OKL is pulled low, it indicates that the calibration is completed, and at this time, it automatically returns to the normal operating mode, i.e., MDH MDL=00 state.

7.6. System calibration

System calibration can correct the bias error and gain error within the chip and the system, because the system calibration must be carried out after inputting the input signal. System correction includes offset error correction and gain error correction.

For zero offset error correction, the input must be required to be a differential voltage of 0V, and the MDH and MDL in the configuration registers are written to (1, 0) to start the zero offset. The chip calculates the zero offset error value of the system and writes it to the zero offset register. It will be compensated for in subsequent operation.

For gain coefficient error correction, a positive full-amplitude voltage must be input, and MDH and MDL in the configuration register are written to (1, 1) to start gain error correction. The chip calculates the gain error value of the system and writes it to the gain coefficient register. Compensation is given during subsequent operation.

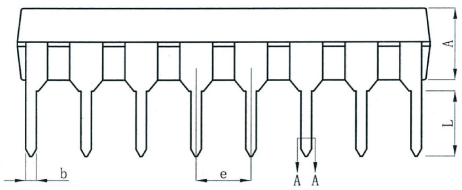
8. ORDERING INFORMATION

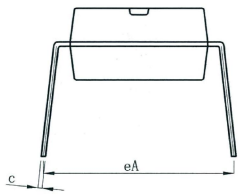
Ordering Information

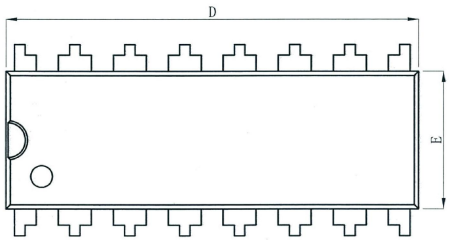
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL7705B	XL7705B	SOP16W	10.45 * 7.5	-40 to +85	MSL3	T&R	1000
XD7705B	XD7705B	DIP16	19.05 * 6.35	-40 to +85	MSL3	Tube 25	1000

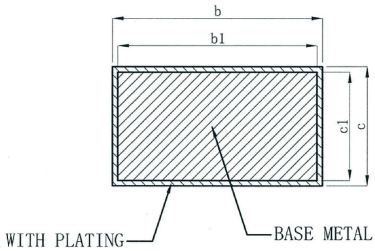
9. DIMENSIONAL DRAWINGS

DIP-16



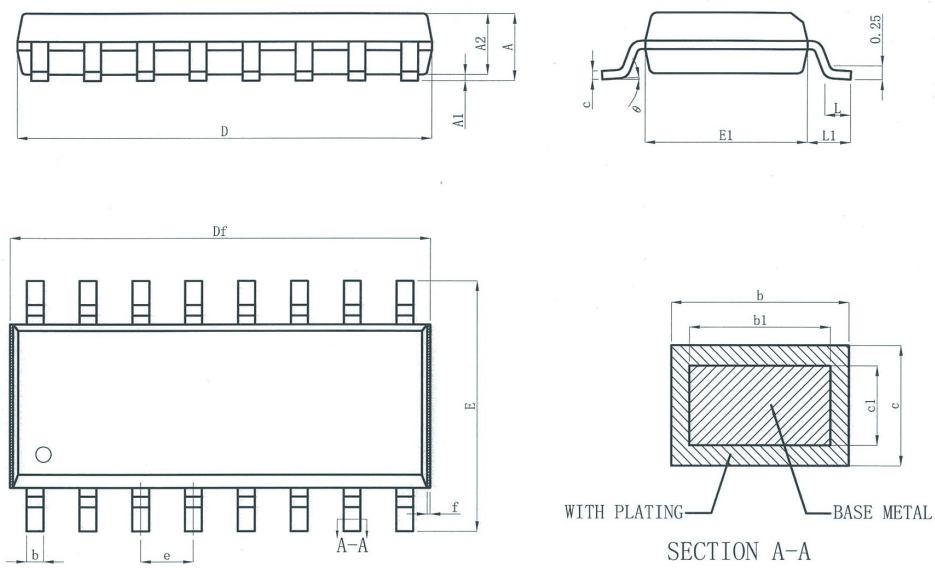


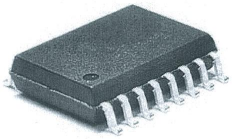




symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

SOP-16W





symbol	millimeter		
	Min	Nom	Max
A	---	---	2.65
A1	0.10	0.20	0.30
A2	2.20	2.30	2.40
b	0.39	---	0.47
b1	0.38	0.41	0.43
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	10.10	10.20	10.30
Df	10.20	---	10.70
E	10.26	10.41	10.60
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.55	---	0.85
L1	---	1.40	---
θ	0°	---	8°
f	0.05	---	0.20