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TVS



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SN74LVC1G3157XXXX-MS

Product specification





DESCRIPTION

The SN74LVC1G3157XXXX-MS is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power–supply range (from VCC to GND).

The Select pin has over voltage protection that allows voltages above VCC, up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

FEATURES

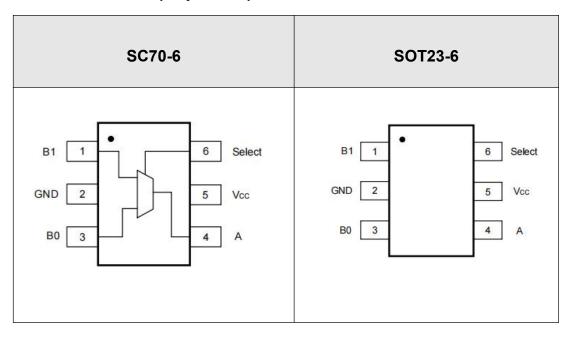
- Low power dissipation
- High speed
- Standard CMOS logic levels
- High bandwidth, improved linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- be used for Clock Switching, Data Mux'ing,etc.
- Low RDSON
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Operating temperature -55C ~ +125C
- package: SC70-6, DFN1.45 × 1.0-6, SOT23-6

ORDER INFORMATION

P/N	PKG	QTY
SN74LVC1G3157DCKR-MS	SC70-6	Tape and Reel, 3000
SN74LVC1G3157DBVR-MS	SOT23-6	Tape and Reel, 3000



PIN CONFIGURATION (Top View)



PIN DESCRIPTIONS

Pin	I/O	Pin Function
A, B0 , B1	I/O	Data port
Select	I	Controlling choice
VCC	1	Power supply port
GND	1	Ground

FUNCTIONS DESCRIPTION

Select input port	Function
L	B0 Connected to A
Н	B1 Connected to A



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 ~ +7.0	V
DC Switch Voltage (1)	Vs	-0.5 ~ V _{CC} +0.5	V
DC Input Voltage (1)	V _{IN}	-0.5 ~ +7.0	V
DC Input Diode Current @ V _{IN} < 0 V	I _{IK}	-50	mA
DC Output Current	lout	128	mA
DC V _{CC} or Ground Current	Icc/I _{GND}	100	mA
Storage Temperature Range	Tstg	-65 ~ +150	С
Junction Temperature Under Bias	T _J	150	С
Junction Lead Temperature (Soldering, 10 Seconds)	T _L	260	С
Power Dissipation @ +85°C	P _D	180	mW

NOTE:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

CAUTION

This integrated circuit can be damaged by **ESD** if you don't pay attention to **ESD** protection. recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

QCSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact sales office to get the latest datasheet.



RECOMMENDED OPERATING CONDITIONS (2)

Ch	Symbol	Min	Max	Unit	
Supply	Voltage Operating	VCC	1.65	5.5	V
Sele	ct Input Voltage	VIN	0	VCC	V
Swit	VIN	0	VCC	V	
0	utput Voltage	VOUT	0	VCC	V
Opera	TA	-55	+125	С	
Input Disc and Fall Time	Control Input VCC = 2.3 V ~ 3.6 V	tr tf	0	10	no/\/
Input Rise and Fall Time	Control Input VCC = 4.5 V ~ 5.5 V	tr,tf	0	5.0	ns/V

Note:

2. Select input must be held HIGH or LOW, it must not float.



ELECTRICAL CHARACTERISTICS

Symph al	Danamatan	Test		TA = 25C			TA = -40C ~ +85C		
Symbol	Parameter	Conditions	VCC	Min	Тур	Max	Min	Max	Unit
DC ELE	CTRICAL CHA	RACTERISTICS						1	
			1.65 ~ 1.95				0.75Vcc		
	High Level Input		2.3 ~ 2.8				1.5		V
VIH	Voltage		3 ~ 4.2				2.4		
			4.5 ~ 5.5				0.6Vcc		
			1.65 ~ 1.95					0.25VCC	
VIL	Low Level Input Voltage		2.3 ~ 2.8					0.4	V
			3 ~ 5.5					0.3Vcc	
liN	Input Leakage Current	0 < VIN < 5.5 V	0 ~ 5.5		±0.05	±0.1		±1	uA
IOFF	OFF State Leakage Current	0 < A, B < Vcc	1.65 ~ 5.5		±0.05	±0. 1		±1	uA
ICC	Quiescent Supply	VIN = Vcc or GND IOUT = 0	5.5			1.0		10	uA
	Analog Signal Range		VCC	0		VCC	0	VCC	V
		VIN = 0 V, IO = 30 mA			3.0			7.0	Ω
		V _{IN} = 2.4 V, I _O = -30 mA			5.0			12	Ω
		VIN = 4.5 V, IO = -30 mA	4.5		7.0			15	Ω
		VIN = 0 V, IO = 24 mA			4.0			9.0	Ω
		VIN = 3 V , IO = -24 mA	3.0		10			20	Ω
RON	Switch On Resistance ⁽³⁾	VIN = 0 V, IO = 8 mA			5.0			12	Ω
	resistance	VIN = 2.3 V, IO = -8 mA	2.3		13			30	Ω
		VIN=0V, IO =4 mA			6.5			20	Ω
		VIN = 1.65 V, IO = -4 mA	1.65		17			50	Ω
	On Resistance	IA = -30 mA 0 ≤ VBn ≤ VCC	4.5					25	Ω
RRANGE	Over Signal Range ⁽³⁾⁽⁷⁾	I _A = -24 mA 0 ≤ V _{Bn} ≤ V _{CC}	3					50	Ω



ELECTRICAL CHARACTERISTICS (continued)

o	D	T1 0 - 1111	vcc		TA = 25	С	TA = -4	0C ~ +85C	
Symbol Parameter	Parameter	Test Conditions		Min	Тур	Max	Min	Max	Unit
	On Resistance Over Signal	IA = -8 mA 0 ≤ VBn ≤ VCC	2.3					100	Ω
RRANGE	Range(3)(7)	IA = -4 mA 0 ≤ VBn ≤ VCC	1.65					300	Ω
		IA = -30 mA VBn = 3.15	4.5		0.15				Ω
		IA = -24 mA VBn = 2.1	3		0.2				Ω
ΔRON	On Resistance Match Between	IA = -8 mA VBn = 1.6	2.3		0.5				Ω
ΔRON	Channels(3)(4)(5)	IA = -4 mA VBn = 1.15	1.65		0.5				Ω
		IA = -30 mA 0 ≤ VBn ≤ VCC	5		6.0				Ω
		IA = -24 mA 0 ≤ VBn ≤ VCC	3.3		12				Ω
DELAT	On Resistance	IA = -8 mA 0 ≤ VBn ≤ VCC	2.5		28				Ω
RFLAT	Flatness(3)(4)(6)	IA = -4 mA 0 ≤ VBn≤ VCC	1.8		125				Ω
ELECT	RICAL CHARACT	TERISTICS							
			1.65 ~ 1.95						nS
	Propagation		2.3 ~ 2.7					1.2	nS
tPHL	Delay Bus to	Figure 1	3.0 ~ 3.5					0.8	nS
tPLH	Bus (8)	VI = OPEN	4.5 ~ 5.5					0.3	nS
	Output Enable	Figure 1	1.65 ~ 1.95			23	7.0	24	nS
tPZL	Time,	VI = 2*VCC for	2.3 ~ 2.7			13	3.5	14	nS
	Turn On Time	tPZL ,VI = 0 V for	3.0 ~ 3.5			6.9	2.5	7.6	nS
tPZH	(A to Bn)	tPZH	4.5 ~ 5.5			5.2	1.7	5.7	nS
			1.65 ~ 1.95			12.5	3.0	13	nS
	Output Disable	Figure 1	2.3 ~ 2.7			7.0	2.0	7.5	nS
	Time, Turn Off	VI = 2*VCC for	3.0 ~ 3.5			5.0	1.5	5.3	nS
tPLZ tPHZ	Time (A Port to	tPLZ ,VI = 0 V for							



ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Т	TA = 25C		TA = -40	C ~ +85C	
Symbol	Farameter	rest Conditions	VCC	Min	Тур	Max	Min	Max	Unit
			1.65 ~ 1.95				0.5		nS
	Break Before	Figure2 ,	2.3 ~ 2.7				0.5		nS
tB-M	Make Time (7)	CL = 50 pF ,	3.0 ~ 3.5				0.5		nS
	Make Time \ /	RL = 600 Ω	4.5 ~ 5.5				0.5		nS
		Figure 3, CL = 0.1 nF ,	5.0		7.0				рС
Q	⁽⁷⁾ Charge Injection	VGEN = 0 V , RGEN = 0 Ω	3.3		3.0				рС
OIRR	Off Isolation ⁽⁹⁾	Figure 4, RL = 50Ω , f = $10MHz$	1.65 ~ 5.5		-57				dB
		Figure 5,							
Xtalk	Crosstalk	RL= 50 Ω , f = 10MHz	1.65 ~ 5.5		-54				dB
BW	−3 dB Bandwidth	Figure 8, RL = 50 Ω	1.65 ~ 5.5		350M				Hz
THD	Total Harmonic Distortion ⁽⁷⁾	RL = 600 Ω, 0.5VP-P f = 600 Hz ~ 20 kHz	5.0		0.011				%
CIN	Select Pin Input Capacitance (10)		0		2.3				pF
CIO-B	B Port Off Capacitance (10)	Figure 6	5.0		5.0				pF
CIOA- O N	A Port Capacitance when Switch is Enabled ⁽¹⁰⁾	Figure 7	5.0		15.5				pF



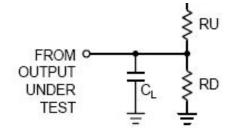
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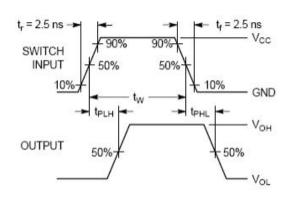
- 3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
- 4. Parameter is characterized but not tested in production.
- 5. Δ RON = RON max RON min measured at identical VCC, temperature and voltage levels.
- 6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
- 7. Guaranteed by Design.
- 8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
- 9. Off Isolation = 20 log10 [VA/VBn].
- 10. TA = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

TEST CIRCUITS

NOTE: Input driven by 50 Ω source terminated in 50 Ω

NOTE: C_L includes load and stray capacitance NOTE: Input PRR = 1.0 MHz; t_W = 500 ns





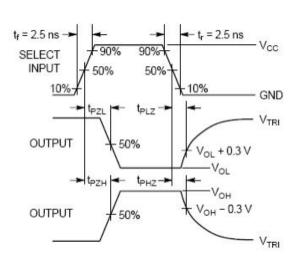
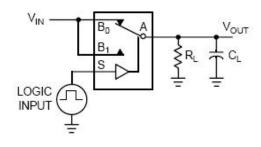


Figure 1. AC Test Circuit ,AC Waveforms



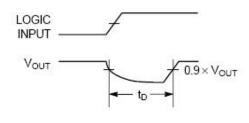


Figure 2. Break Before Make Interval Timing



TESTCIRCUITS(continued)

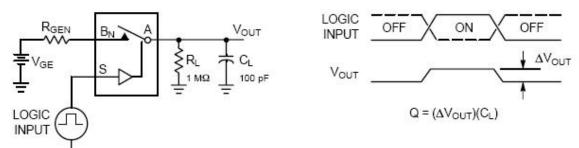


Figure 3. Charge Injection Test

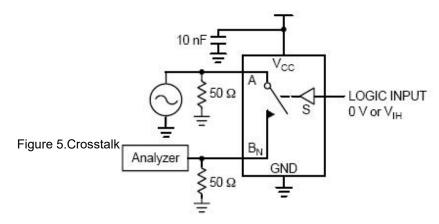


Figure 4. Off Isolation

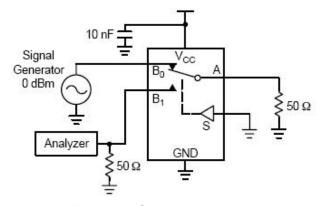


Figure 5.Crosstalk

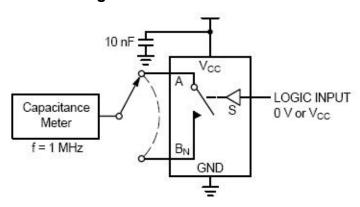


Figure 6. Channel Off Capacitance



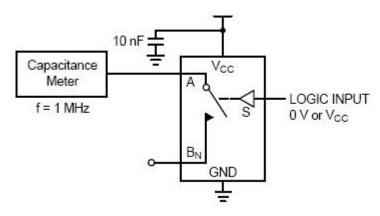


Figure 7. Channel On Capacitance

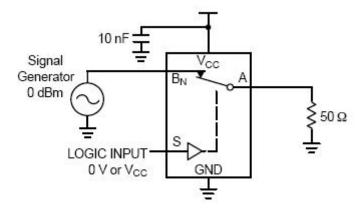
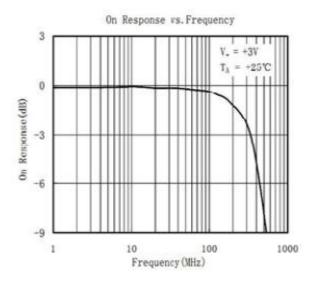
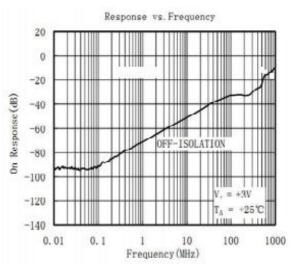
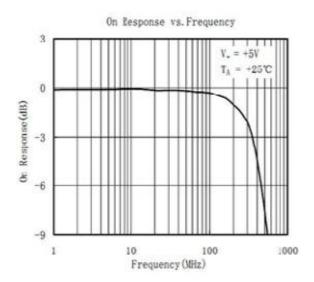


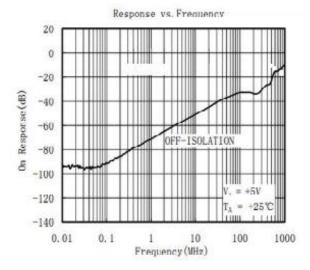
Figure 8. Bandwidth







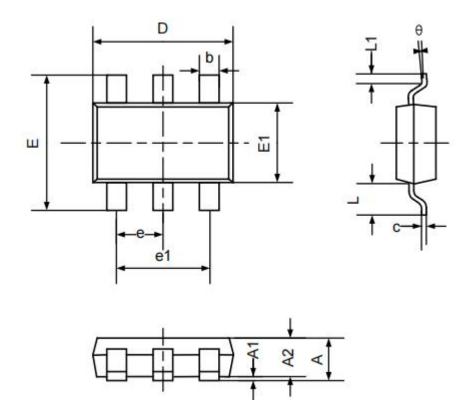






PACKAGE OUTLINE

SC70-6

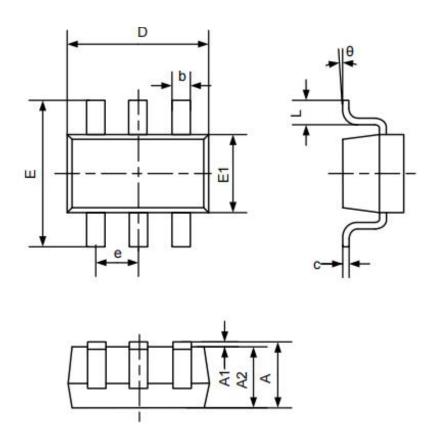


Symbol	Dimensions in Millimeters					
	Min	Max				
A	0.85	1.05				
A1	0.00	0.10				
A2	0.80	1.00				
b	0.15	0.35				
С	0.08	0.22				
D	2.02	2. 12				
E	2.20	2.40				
E1	1.25	1.35				
е	0	.65BSC				
e1	1	.30BSC				
L	0	0.50REF				
L1	0.28	0.38				
θ	0°	8°				



PACKAGE OUTLINE

SOT-23-6



Symbol	Dimensions in Millimeters						
	Min	Nom	Max				
A			1.240				
A1	0.010	0.050	0.090				
A2	1.050	1.100	1.150				
b	0.300	0.300 0.350					
С	0.117	0.117					
D	2.870	2.870 2.920					
E	2.720	2.800	2.880				
E1	1.550	1.550 1.600					
е		0.950BSC					
1		1.900BSC					
L	0.320	0.400	0.480				
θ	0°		5°				



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