5V,7A,5A Low-side GaN and MOSFET Driver For 1ns Pluse Width Applications

Features

- Low-Side, Ultra-Fast Gate Driver for GaN andSilicon FETs
- 1 ns Minimum Input Pulse Width
- 3.0 ns Typical,4.5 ns Maximum Propagation Delay
- 5-V Supply Voltage
- UVLO and Overtemperature Protection

Size：1.28mm×0.84mm×0.60mm

BGA-6

Applications

- LiDAR
- Time-of-Flight Laser Drivers
- Power Converters
- GaN-Based Synchronous Rectifier

Description

The LMG1020YF device is a single, low-side driver designed for driving GaN FETs and logic-level MOSFETs in high-speed applications including LiDAR, time-of-flight, facial recognition, and any power converters involving low side drivers. The design simplicity of the LMG1020YF enables extremely fast propagation delays of 3 nanoseconds and minimum pulse width of 1 nanosecond.The drivestrength is independently adjustable for the pull-up and pull-down edges by connecting external resistors between the gate and OUTH and OUTL, respectively.

The driver features undervoltage lockout (UVLO) and overtemperature protection (OTP) in the event of overload or fault conditions. 0.8mm×1.2mm WCLSP package of LMG1020YF minimizes gate loop inductance and maximizes power density in high-frequency applications.

Functional Block Diagram

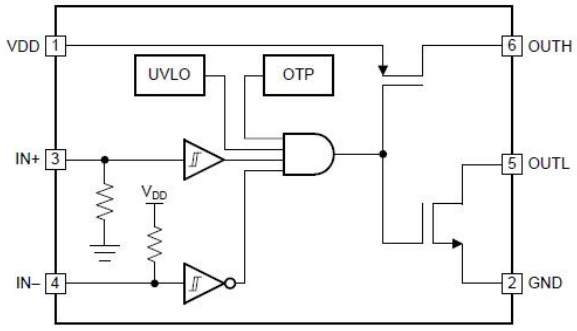


Fig 1 Functional Block Diagram of LMG1020YFFR

Electrical Characteristics (V_{DD}=5V， T_A=25℃， unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD,Q}$	VDD Quiescen Current	IN_+=IN_-=0V		56	70	uA
$I_{VDD,op}$	VDD Operating Current	f=30MHz, 2Ω, 0.1pF load		36		mA
		f=30MHz, 2Ω, 100pF load		48		mA

$V_{DD,UVLO}$	Under-voltage Lockout	V_{DD} rising		4.20	4.30	V
$\Delta V_{DD,UVLO}$	UVLO Hysteresis			100		mV
V_{IH}	IN+,IN- high threshold		1.7	2.3	2.6	V
V_{IL}	IN+,IN- low threshold		1.1	1.4	1.8	V
V_{HYST}	IN+,IN- hysteresis		0.5		1	V
R_{IN+}	Positive input pull-down resistance	To GND	200	250	300	KΩ
R_{IN-}	Negative input pull-up resistance	To V_{DD}	200	250	300	KΩ
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH}=100mA,IN_+=5V,IN_-=0V		43	50	mV
V_{OL}	OUTL voltage	I_{OUTL}=100mA,IN_+=IN_-=0V		35	40	mV
I_{OH}	Peak source current (1)	V_{OUTH}=0V,IN+=5V,IN-=0V		7		A
I_{OL}	Peak sink current (1)	V_{OUTL}=5V,IN+=IN-=0V		5		A
t_{start}	Startup Time, VDD rising above UVLO	IN-=GND,IN+=VDD,VDD rising up 4.2V to OUTH rising		40	70	us
t_{off}	ULVO falling	IN-=GND,IN+=VDD,VDD falling below 4.1V to OUTH falling	1	2	3	us
t_r	Output rise time	0Ω series 100 pF load(2)		400		ps
t_f	Output fall time	0Ω series 100 pF load(2)		500		ps
t_{min}	Minimum input pulse width	0Ω series 100 pF load(2)		1		ns
t_{pdr}	Propagation delay,turn on	IN_-=0V,IN+ to OUTL,100 pF load		3.0	4.5	ns
t_{pdf}	Propagation delay,turn off	IN-=0V,IN+ to OUTH,100 pF load		3.0	4.5	ns

(1) Insured by design

(2) rise and fall calulated as a 20% to 80%

Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply voltage V_{DD}		5.75	V
IN+, IN- pin voltage V_{IN}	0	V_{DD}	V
OUTH, OUTL pin voltage V_{OUT}	0	5.75	V
Operating Temperature T_A	-55	150	℃
Storage Temperature T_S	-65	150	℃

Recommended Operating Conditions

PARAMETER	MIN	MAX	UNIT
Supply voltage V_{DD}	4.50	5.50	V
IN+, IN- pin voltage V_{IN}	0	V_{DD}	V
Operating Temperature T_A	-55	125	℃

Timing Diagram

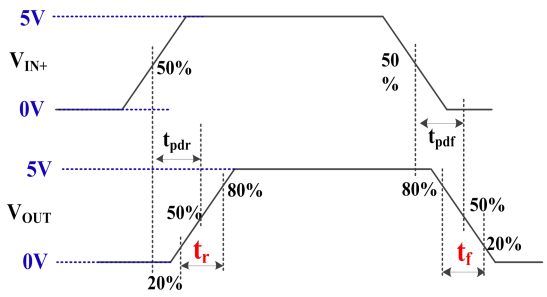


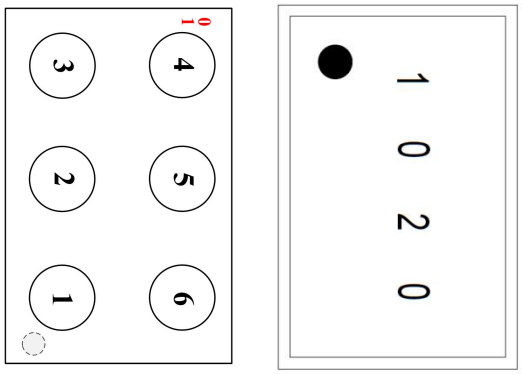
Fig 2 Timing Diagram of LMG1020YFFR

Device Functional Modes

Table 1 Truth Table

IN–	IN+	OUTH	OUTL
L	L	OPEN	L
L	H	H	OPEN
H	L	OPEN	L
H	H	OPEN	L

Pin Configuration and Functions



NO.	NAME	DESCRIPTION
1	VDD	supply voltage
2	GND	Ground
3	IN+	Positive logic-level input
4	IN-	Negative logic-level input
5	OUTL	Pulldown gate drive output.
6	OUTH	Pullup gate drive output

Fig 3 Pin Functions of LMG1020YFFR

Typical Application

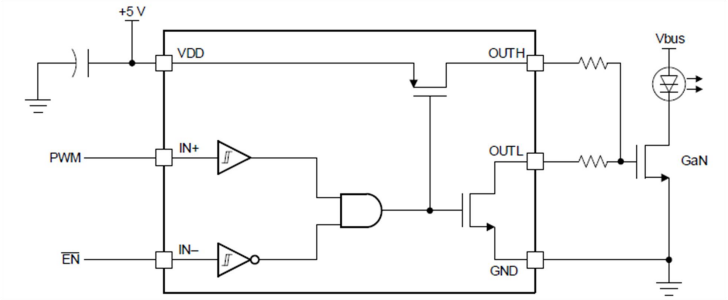


Fig 4 Typical Implementation of LMG1020YFFR

We recommends using at least a 2Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing.Ringing overshoot must not exceed the maximum absolute supply voltage.

We recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to the IC, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1 µF of 0402 or feed-through capacitor (closest toLMG1020YF) and a 1µF 0603 capacitor is recommended.

Typical Characteristics

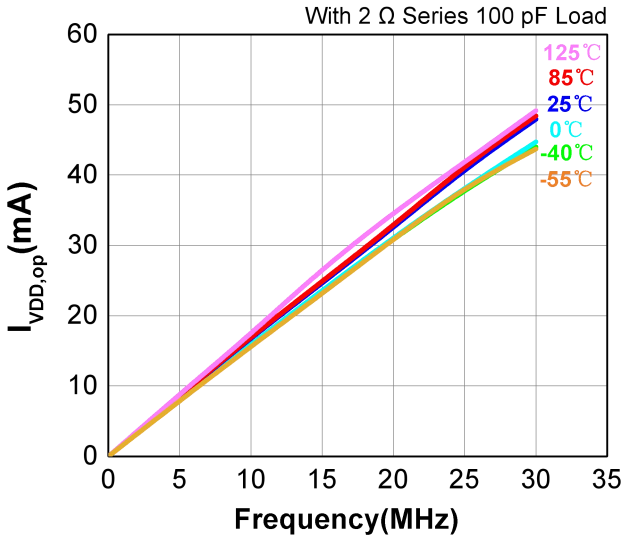


Fig 5 $I_{VDD,op}$ VS Frequency

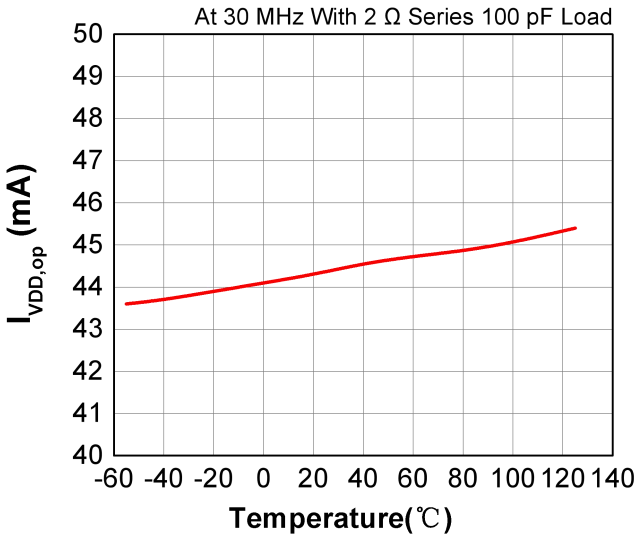


Fig 6. $I_{VDD,op}$ VS Temperature

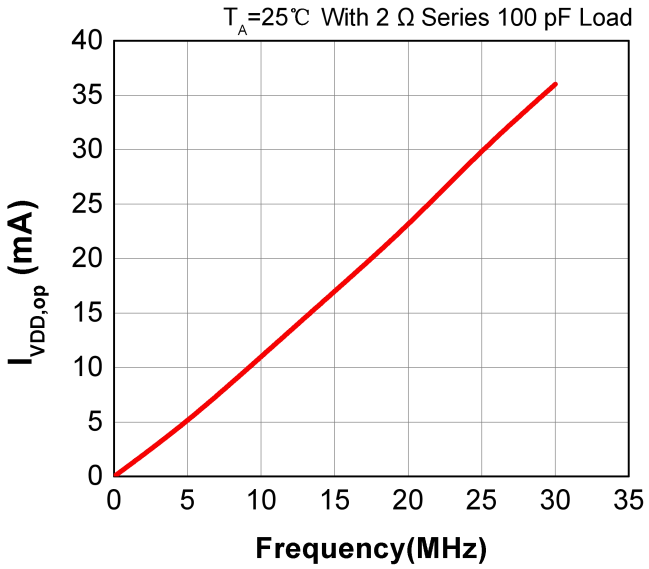


Fig 7 $I_{VDD,op}$ VS Frequency at T_A=25℃

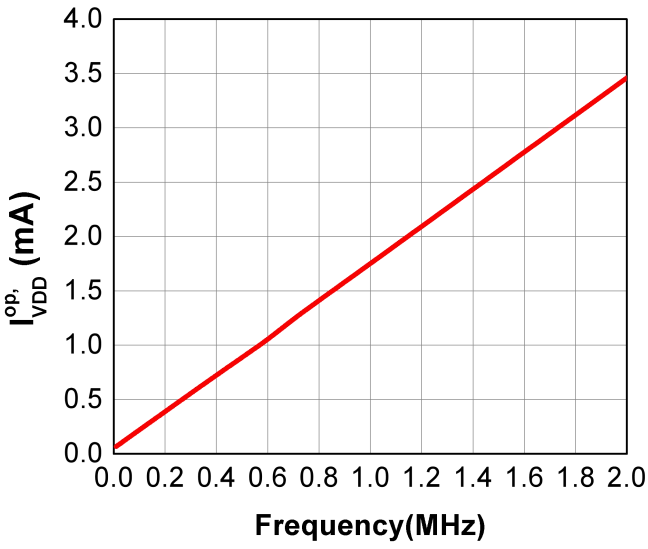


Fig 8 $I_{VDD,op}$ VS Low Frequency at T_A=25℃

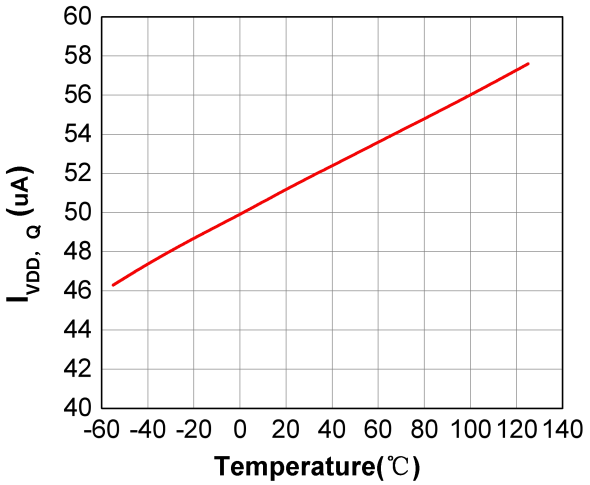


Fig 9 Quiescent Current VS Temperature

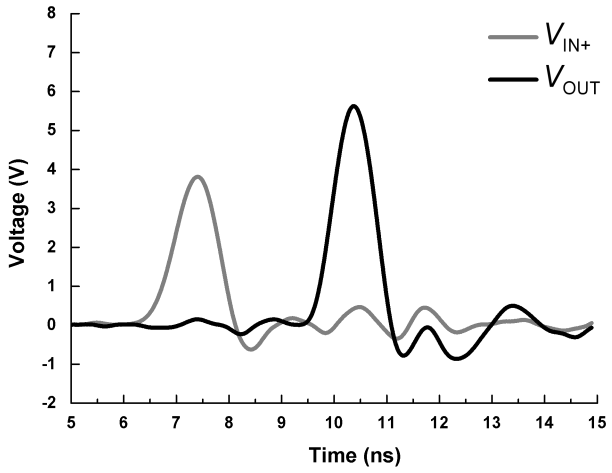


Fig 10 The delay time for V_{IN+} to V_{OUT}

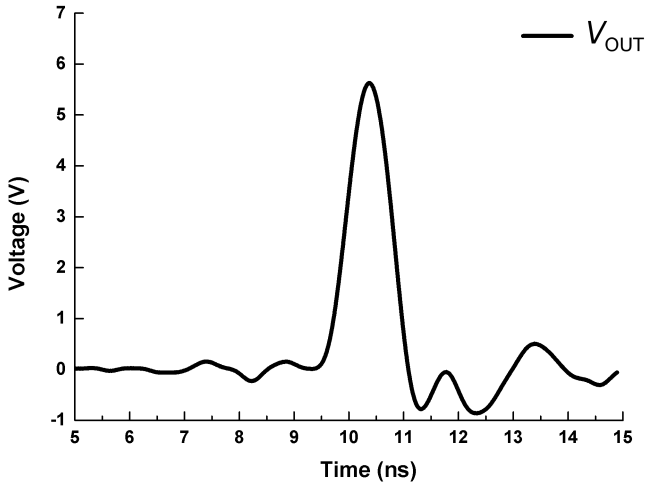


Fig 11 The pulse width for V_{OUT}

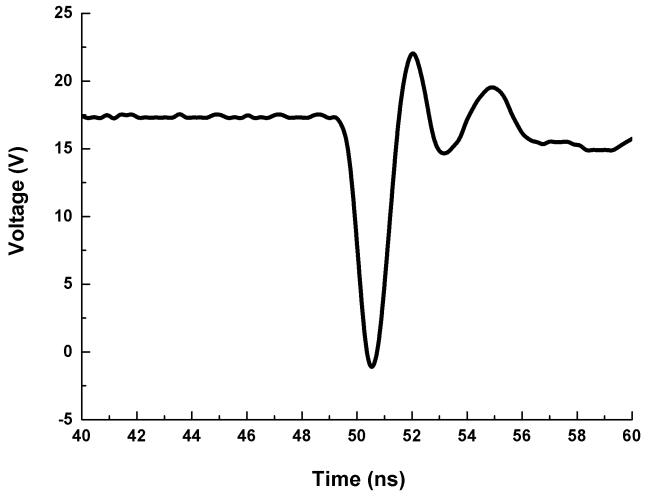


Fig 12 The GaN HEMT drain signal at V_{BUS}=18V，EPC2039 Load

PACKAGE OUTLINE

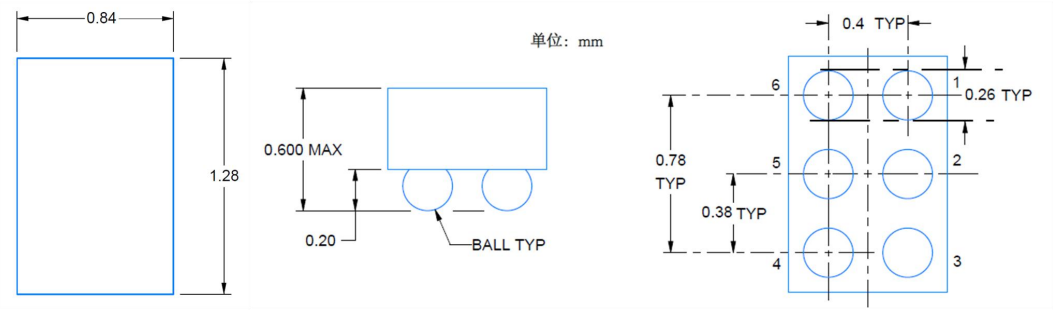


Fig 13 The Package Outline of LMG1020YFFR