PSMN5R6-100YSF

NextPower 100 V, 6 mΩ N-channel MOSFET in LFPAK56 package

19 February 2018 — Preliminary data sheet

1. General description

NextPower 100 V standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial & consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Qualified to 175 °C
- Low Q_G x R_{DSon} FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- LED lighting
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

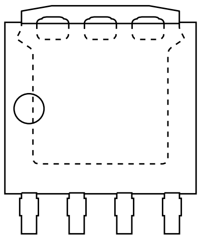
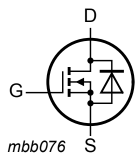
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	120	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	294	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	4.5	5.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 11		-	7.3	8.7	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	13.5	-	nC
$Q_{G(tot)}$	total gate charge			-	65.1	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 41.8 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4; Unclamped	[1]	-	-	440	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 16		-	67.3	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56E; Power-SO8 (SOT1023)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN5R6-100YSF	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch; 4.58 mm x 5.13 mm x 1.03 mm body	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN5R6-100YSF	5F6S10

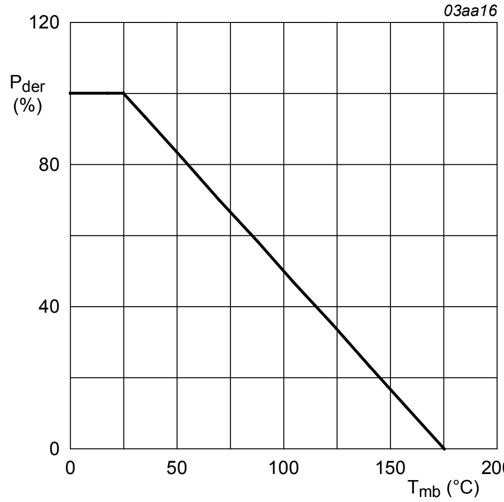
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

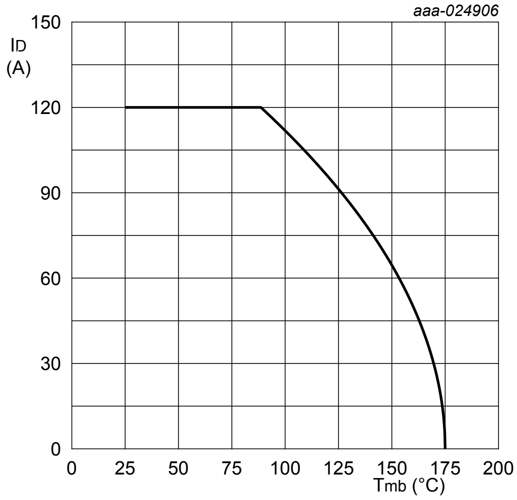
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	294	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	120	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	112	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	480	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	120	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	480	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 41.8 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4; Unclamped	[1]	-	440	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	41.8	A

[1] Protected by 100% test



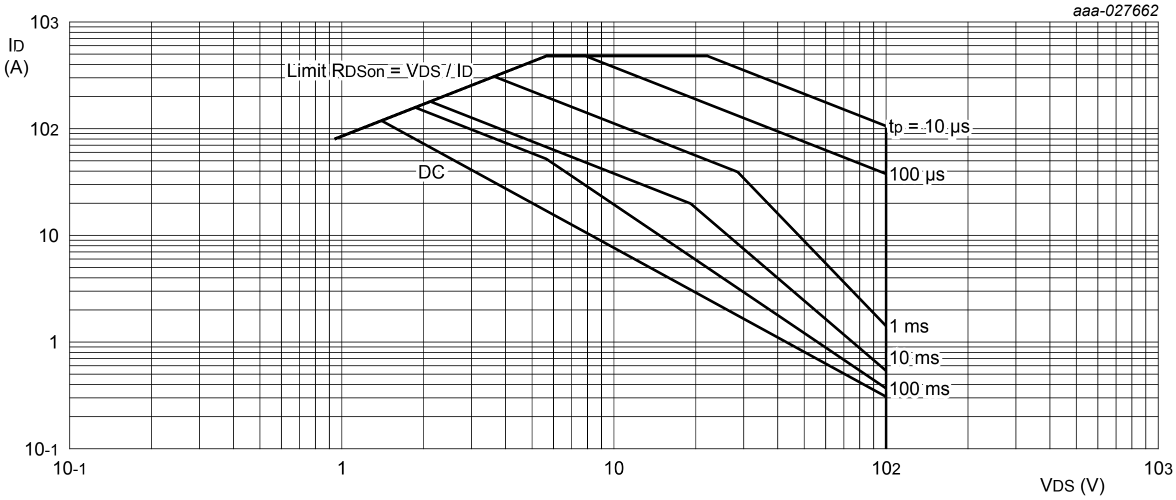
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



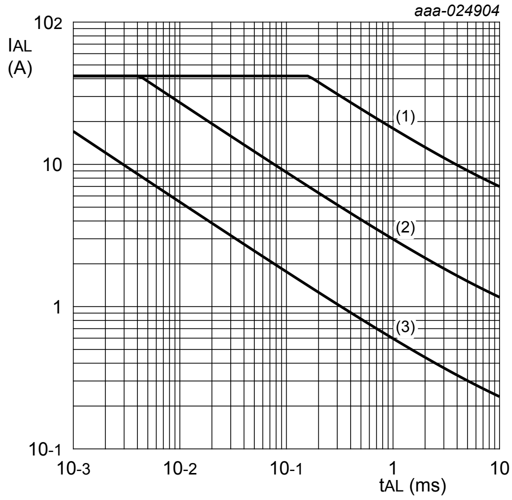
V_{GS} ≥ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.45	0.51	K/W

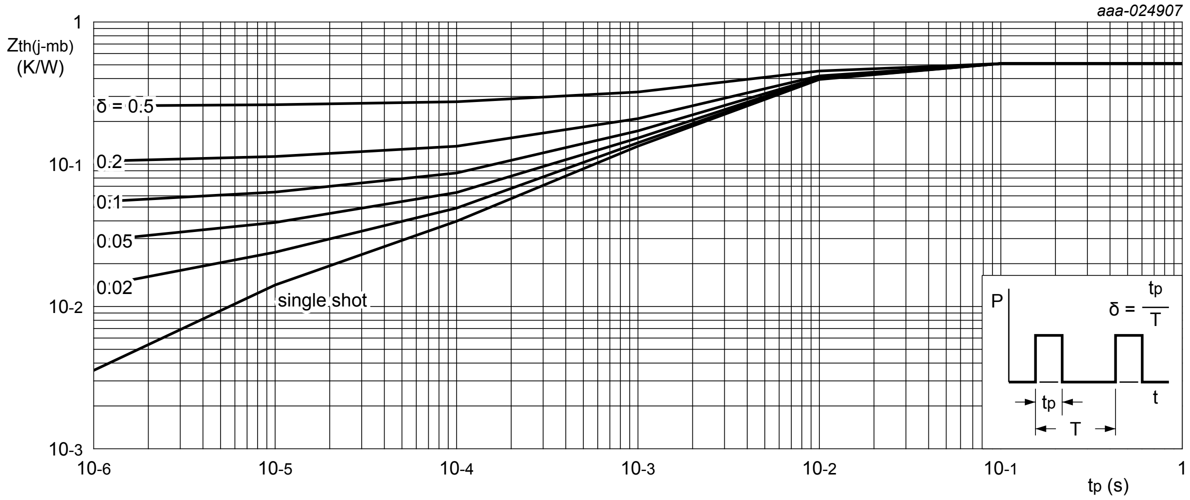


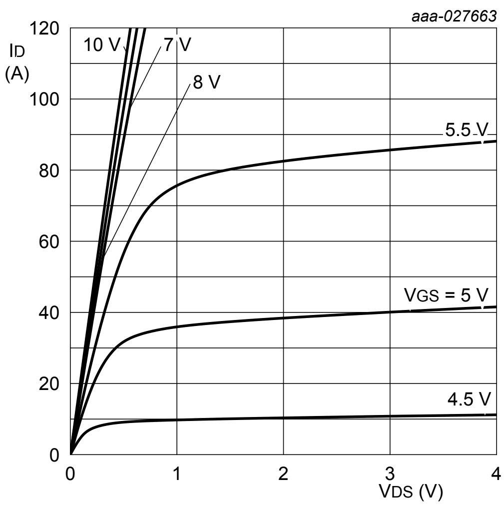
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

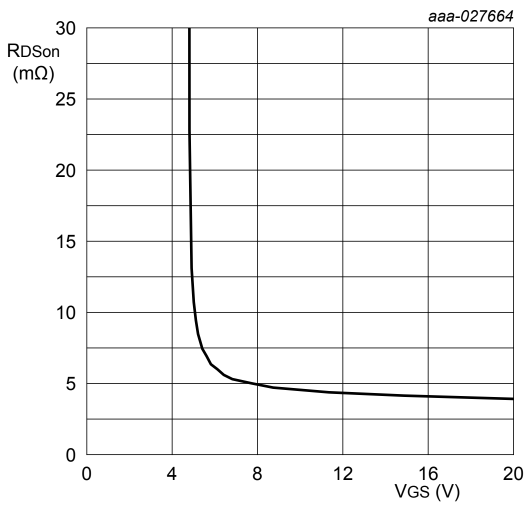
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.6	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.8	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9		2	3.1	4	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 175 °C		-	-8.8	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.03	5	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	5	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	5	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	4.5	5.6	mΩ
		V_{GS} = 7 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	5.1	7.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 11		-	7.3	8.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 11		-	10.3	12.3	mΩ
R_G	gate resistance	f = 1 MHz		-	0.9	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	65.1	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	32.2	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	20.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	12.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	7.9	-	nC
Q_{GD}	gate-drain charge			-	13.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; Fig. 12; Fig. 13		-	4.8	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	4616	-	pF
C_{oss}	output capacitance			-	805	-	pF
C_{rss}	reverse transfer capacitance			-	12	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	17.4	-	ns
t_r	rise time			-	16.3	-	ns
$t_{d(off)}$	turn-off delay time			-	35.1	-	ns
t_f	fall time			-	19.7	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 16		-	51.4	-	ns
Q_r	recovered charge			-	67.3	-	nC



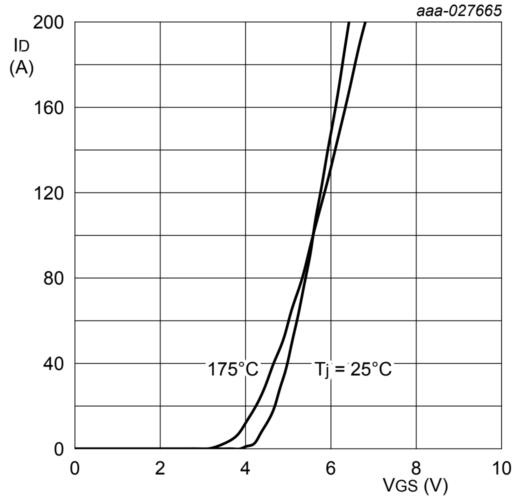
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



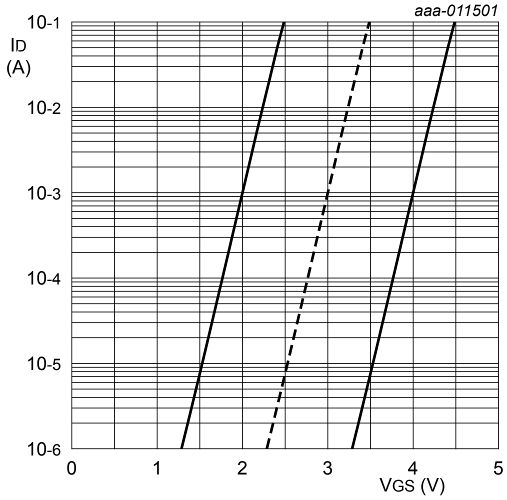
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



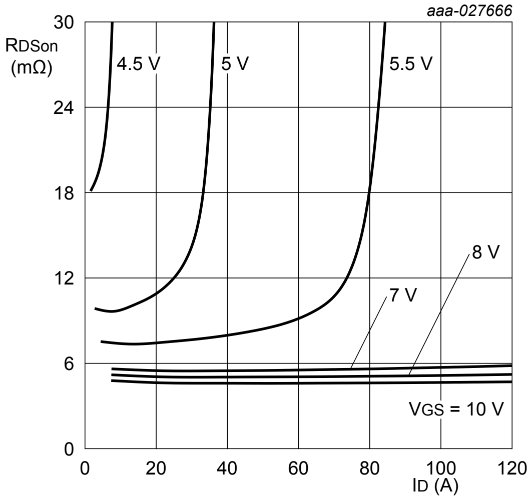
V_{DS} = 12 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



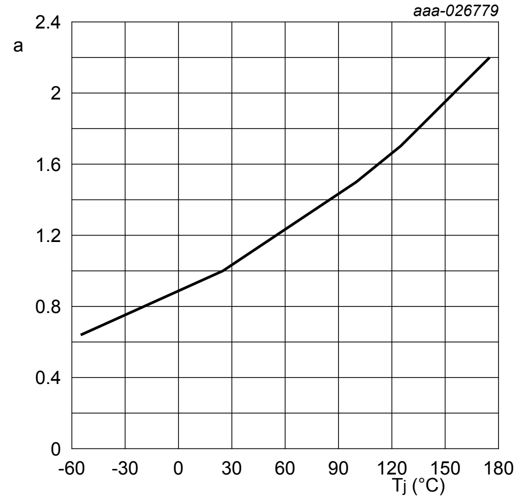
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



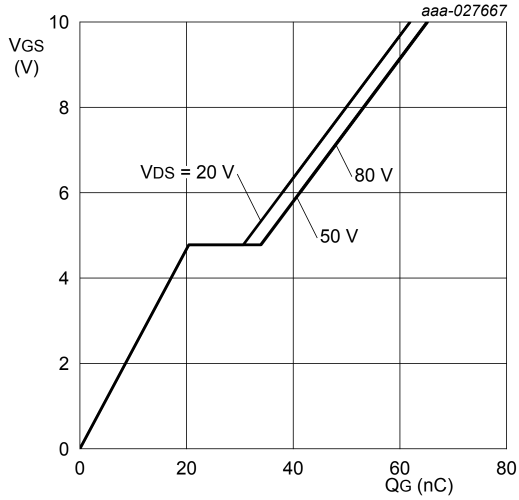
T_j = 25 °C

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 12. Gate-source voltage as a function of gate charge; typical values

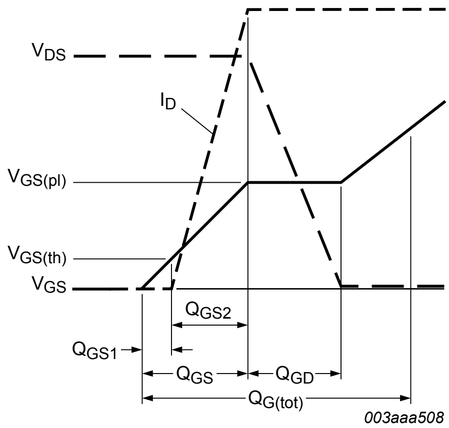
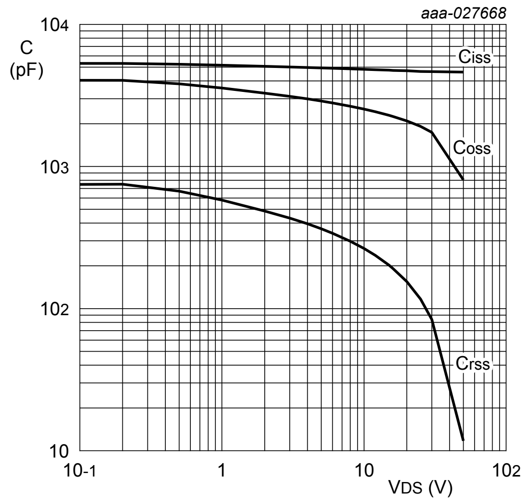
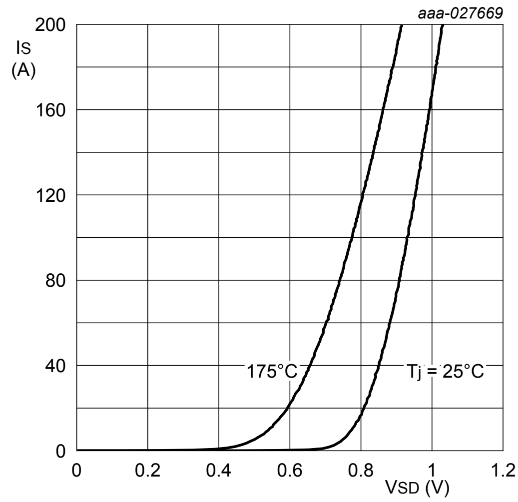


Fig. 13. Gate charge waveform definitions



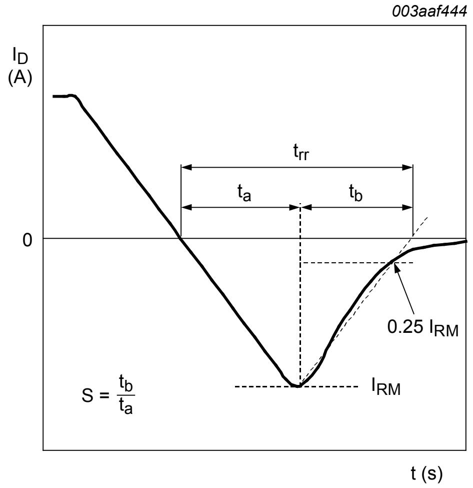
V_{GS} = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

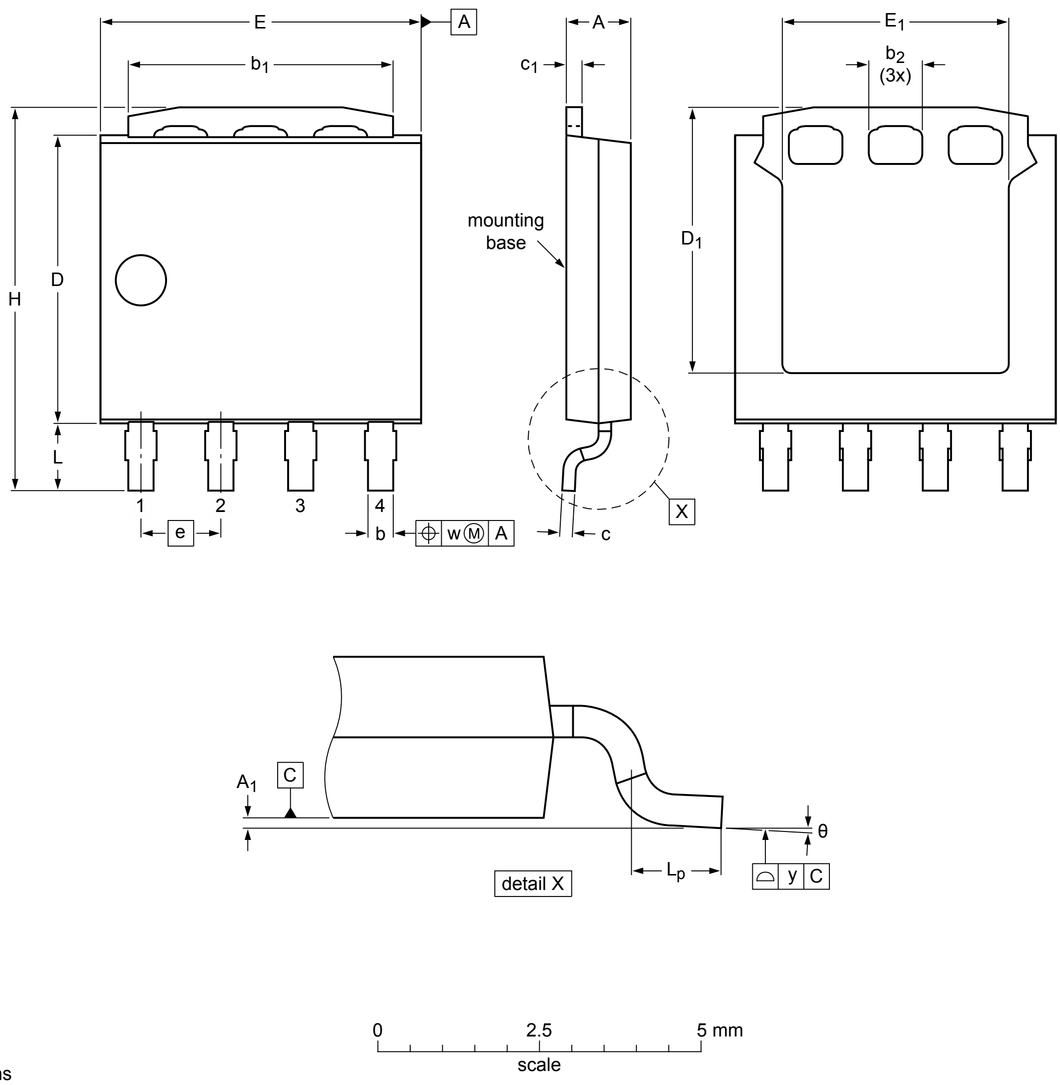


$$t_{rr} = t_a + t_b$$

Fig. 16. Reverse recovery waveform definitions

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 17. Package outline LFPAK56E; Power-SO8 (SOT1023)

12. Soldering

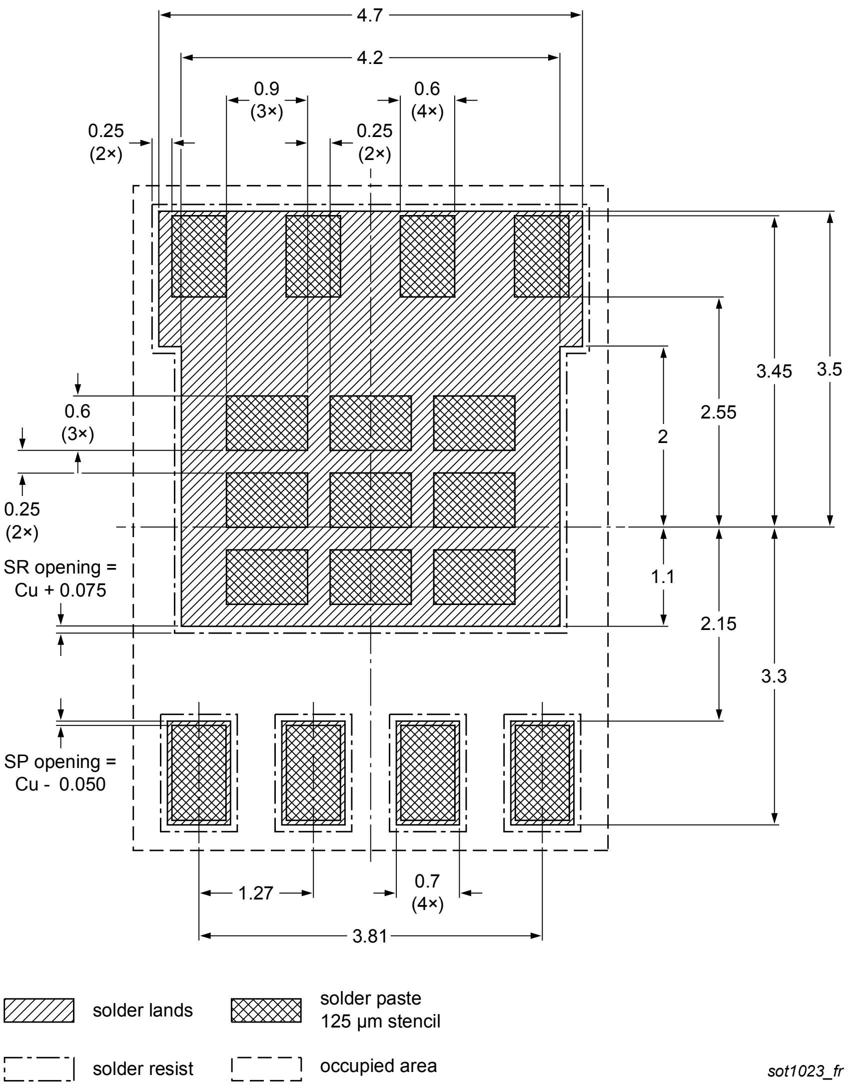


Fig. 18. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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Date of release: 19 February 2018