QM2538N3

N-Channel 20V Fast Switching MOSFET

General Description

The QM2538N3 is the highest performance trench N-Channel MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the Battery MOSFET Switch.

The QM2538N3 meet the RoHS and Green Product requirement.

Product Summary

Green

BVDSS	RDSON (VGS=4.5V)	ID (Tc=25℃)
20V	6.0mΩ	56A

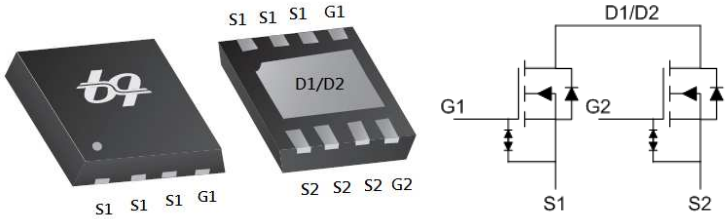
Applications

- Battery MOSFET Switch

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available
- Embedded ESD Protection
- HBM 2KV / MM200V Verified

DFN 3X3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±8	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	56	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	35	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	13	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	10	A
I_{DM}	Pulsed Drain Current[2]	100	A
EAS	Single Pulse Avalanche Energy[3]	45	mJ
I_{AS}	Avalanche Current	30	A
P_D@T_C=25℃	Total Power Dissipation[4]	31	W
P_D@T_A=25℃	Total Power Dissipation[4]	1.6	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	75	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	4	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.01	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=3A	2.3	3.9	6.0	mΩ
		V_{GS}=4.0V , I_D=3A	2.4	4.0	6.8	
		V_{GS}=3.9V , I_D=3A	2.4	4.0	6.8	
		V_{GS}=3.8V , I_D=3A	2.4	4.0	6.8	
		V_{GS}=3.1V , I_D=3A	2.6	4.4	7.5	
		V_{GS}=2.5V , I_D=3A	2.8	4.7	8.0	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.5	0.7	1	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.7	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃	---	---	1	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±8V , V_{DS}=0V	---	---	±10	uA
gfs	Forward Transconductance	V_{DS}=5V , I_D=3A	---	40	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	19.2	---	Ω
Q_g	Total Gate Charge	V_{DS}=10V , V_{GS}=4.5V , I_D=3A	---	41.1	---	nC
Q_{gs}	Gate-Source Charge		---	2.9	---	
Q_{gd}	Gate-Drain Charge		---	12.2	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=4.5V , R_G=3.3Ω , I_D=3A	---	8.3	---	ns
T_r	Rise Time		---	34.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	406.7	---	
T_f	Fall Time		---	189.8	---	
C_{iss}	Input Capacitance	V_{DS}=10V , V_{GS}=0V , f=1MHz	---	2571	---	pF
C_{oss}	Output Capacitance		---	334	---	
C_{rss}	Reverse Transfer Capacitance		---	318	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	56	A
I_{SM}	Pulsed Source Current[2,5]		---	---	100	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.Pluse width limited by maximum junction temperature.
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=8V,L=0.1mH
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

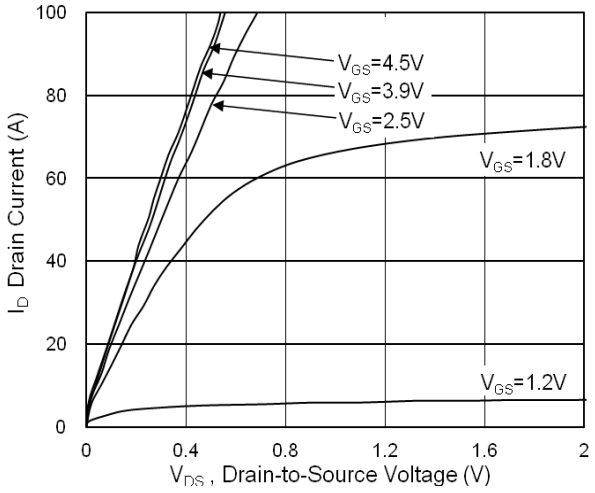


Fig.1 Typical Output Characteristics

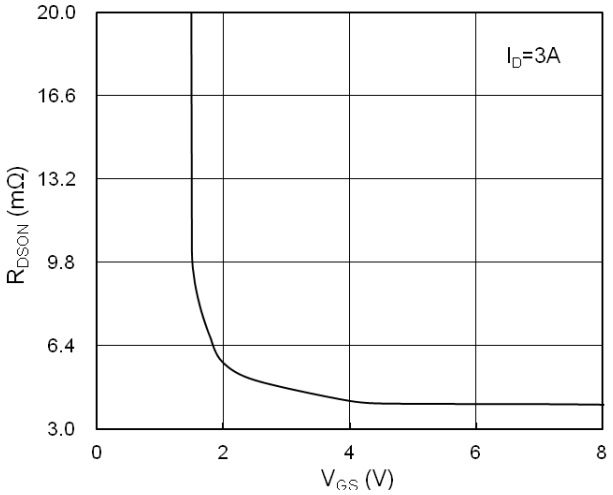


Fig.2 On-Resistance vs. Gate-Source

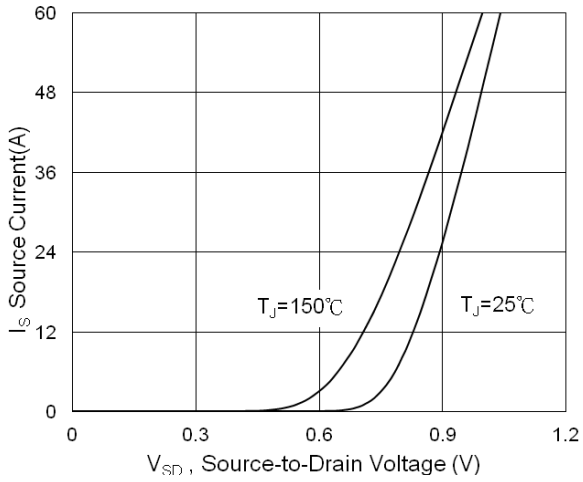


Fig.3 Forward Characteristics of reverse

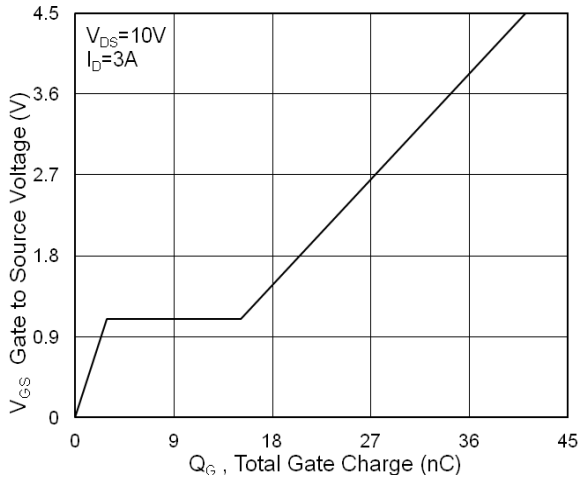


Fig.4 Gate-Charge Characteristics

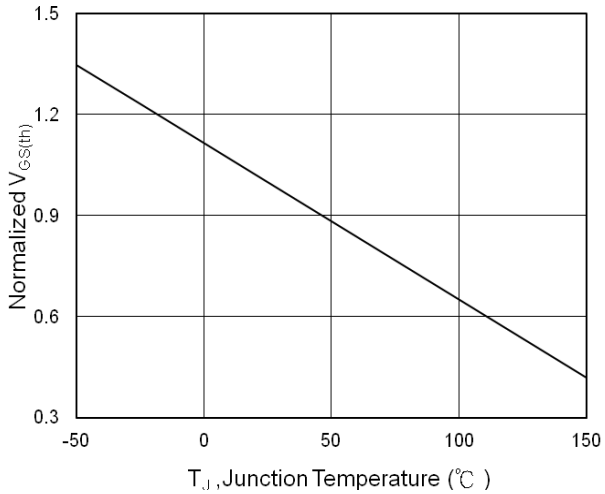


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

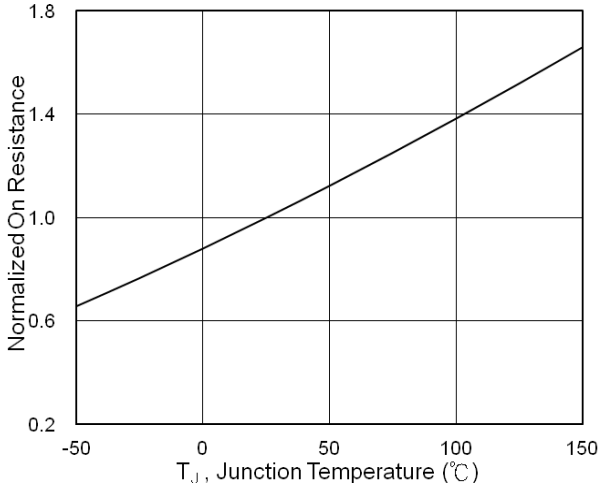


Fig.6 Normalized R_{DSON} vs. T_J

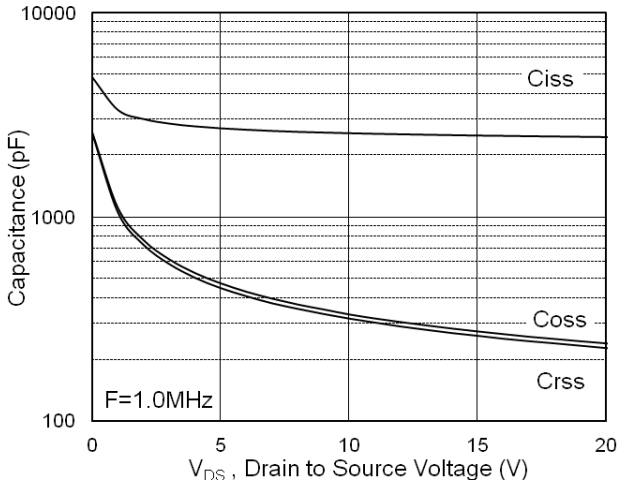


Fig.7 Capacitance

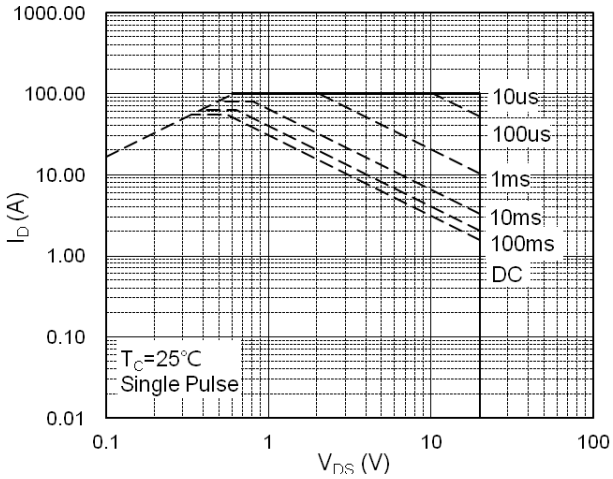


Fig.8 Safe Operating Area

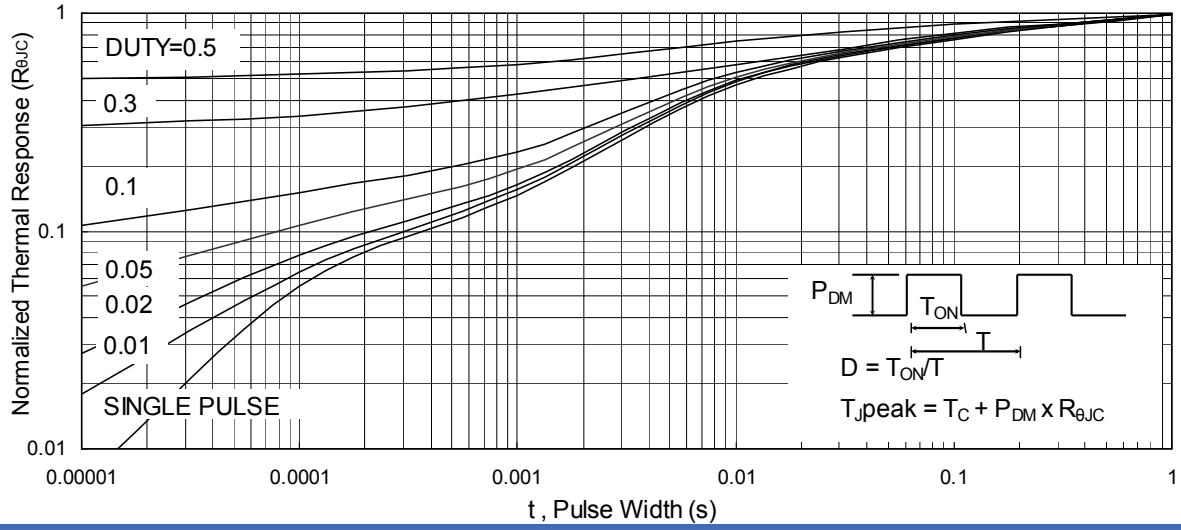


Fig.9 Normalized Maximum Transient Thermal Impedance

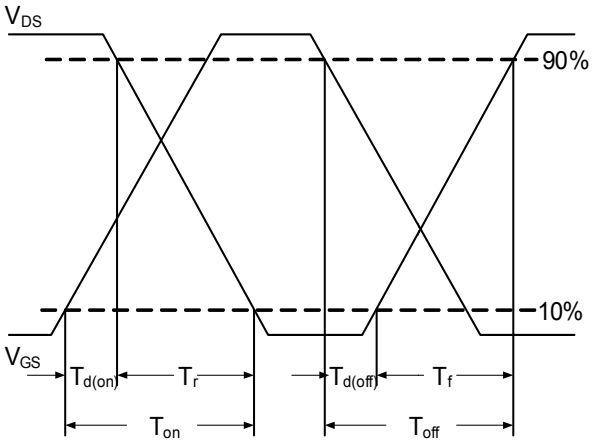


Fig.10 Switching Time Waveform

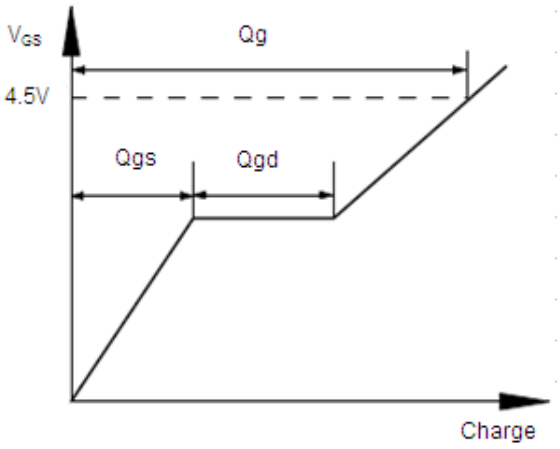
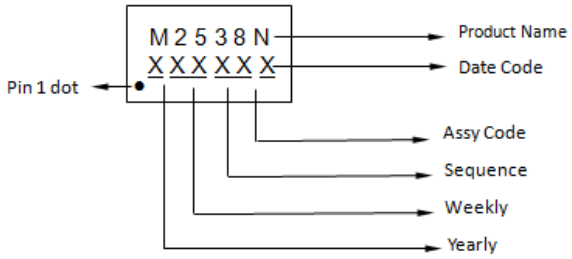
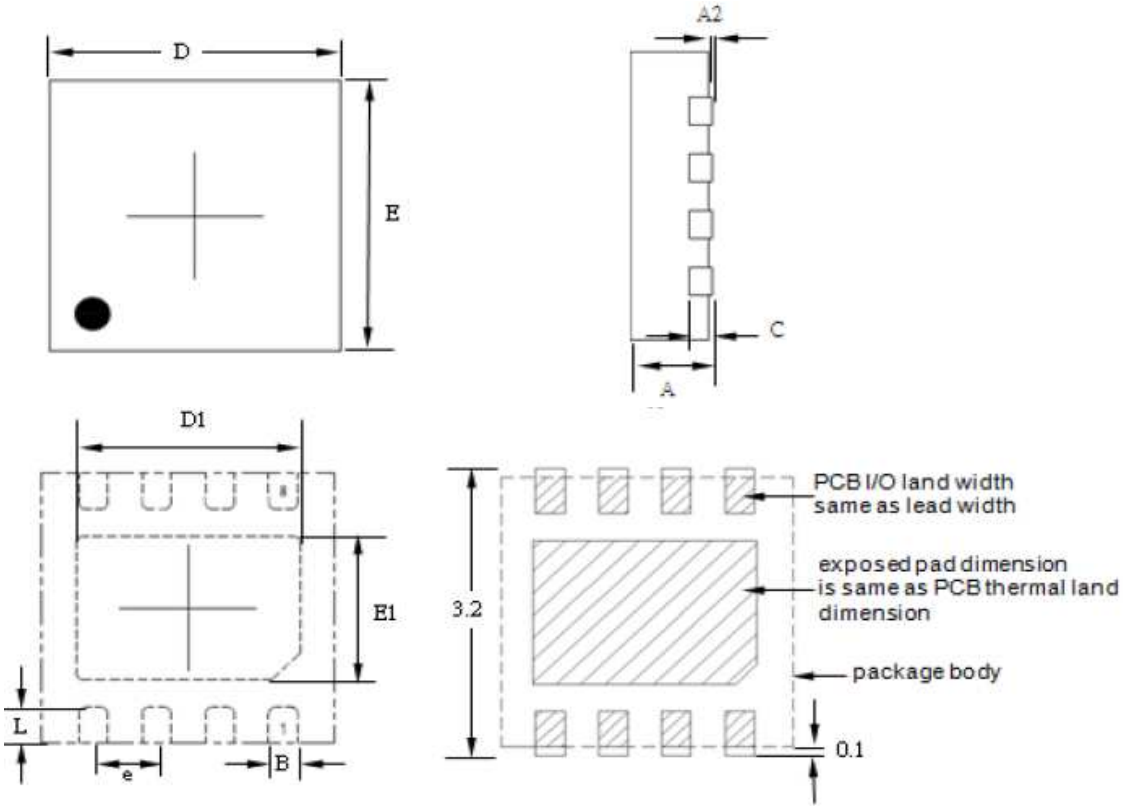


Fig.11 Gate Charge Waveform



X		XX	XX	X
1' st code		2、3nd code	4、5th code	6th code
Year (The 1' st code display with English letter when the wafer supplier is second source)		Weekly	Sequence	Assembly house codes
0:2010	A:2010	01	01	A
1:2011	B:2011	|	|	|
2:2012	C:2012	53	99	Z
3:2013	D:2013			
4:2014	E:2014			
5:2015	F:2015			
6:2016	G:2016			
7:2017	H:2017			
8:2018	I:2018			
9:2019	J:2019			
0:2020	A:2020			
1:2021	B:2021			

Fig.12 Top Marking



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A2	0.00	--	0.05	0.000	--	0.002
B	0.25	0.30	0.35	0.010	0.012	0.014
C	0.20	0.203	0.21	0.008	0.008	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.25	2.30	2.35	0.089	0.091	0.093
E1	1.55	1.60	1.65	--	0.063	--
L	0.35	0.40	0.45	0.014	0.016	0.018
e	--	0.65	--	--	0.026	--

Note:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.CONTROLLING DIMENSION IS MILLIMETER CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACTLY
Revision History:
2015/02/12: Change A from 0.8~1.0 (mm) to 0.7~0.8 (mm)

Fig.13 DFN 3X3 Package Outline Drawing