AiP74LVT2244
Octal Buffer/Line Driver with Termination Resistors; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-12-A1	2017-12	New
2021-12-A2	2021-12	Modify Ordering Information

1、General Description

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-state outputs.

The AiP74LVT2244 is designed with series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

Features:

- Octal bus interface
- 3-state buffers
- Output capability: +12mA and -12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5V bus
- Packaging information: SOP20/TSSOP20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVT2244SA20.TB	SOP20	74LVT2244	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74LVT2244TA20.TB	TSSOP20	74LVT2244	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVT2244SA20.TR	SOP20	74LVT2244	2000 PCS/reel	4000 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74LVT2244TA20.TR	TSSOP20	74LVT2244	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

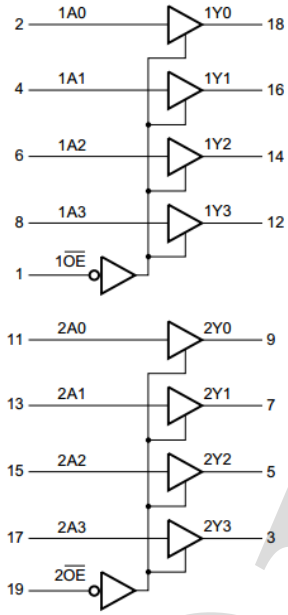


Figure 1. Logic symbol

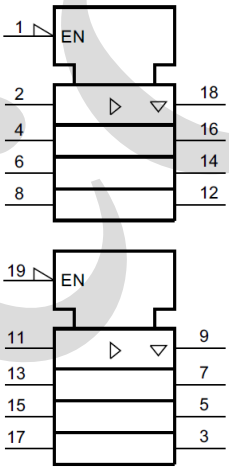
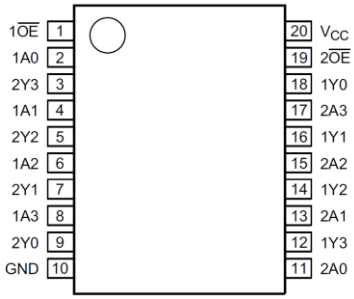


Figure 2. IEC logic symbol

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1,19	$1\overline{OE}$,$2\overline{OE}$	output enable input (active low)
2,4,6,8	1A0, 1A1, 1A2, 1A3	data input
9,7,5,3	2Y0, 2Y1, 2Y2, 2Y3	data output
10	GND	ground (0V)
11,13,15,17	2A0, 2A1, 2A2, 2A3	data input
18,16,14,12	1Y0, 1Y1, 1Y2, 1Y3	data output
20	V_{CC}	supply voltage

2.4、Function Table

Control	Input	Output
n$\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

Note:H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.) [1][2]

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+4.6	V
input voltage	V_I	-[3]	-0.5	+7.0	V
output voltage	V_O	output in OFF-state or HIGH-state[3]	-0.5	+7.0	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output current	I_O	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-[2]	-	+150	℃
total power dissipation	P_{tot}	-[4]	-	500	mW
Soldering temperature	T_L	10s	250		℃

Note:

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal

environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150℃.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[4] For SOP20 packages: above 70℃ derate linearly with 8mW/K.
For TSSOP20 packages: above 60℃ derate linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.7	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
HIGH-level output current	I_{OH}	-	-	-	-12	mA
LOW-level output current	I_{OL}	-	-	-	12	mA
ambient temperature	T_{amb}	in free-air	-40	-	+85	℃
input transition rise and fall rate	Δt/ΔV	outputs enabled	-	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}= -18mA		-1.2	-0.9	-	V
HIGH-level input voltage	V_{IH}	-		2.0	-	-	V
LOW-level input voltage	V_{IL}	-		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_{CC}=3.0V; I_{OH}= -12mA		2.0	2.5	-	V
LOW-level output voltage	V_{OL}	V_{CC}=3.0V; I_{OL}=12mA		-	-	0.8	V
input leakage current	I_I	all input pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	1	10	uA
		control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	±0.1	±1	uA
		data pins[2]	V_{CC}=3.6V;V_I=V_{CC}	-	0.1	1	uA
			V_{CC}=3.6V; V_I=0V	-5	-1	-	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	1	±100	uA
bus hold LOW current	I_{BHL}	V_{CC}=3V; V_I=0.8V[3]		75	150	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3V; V_I=2.0V		-	-150	-75	uA
bus hold LOW overdrive current	I_{BHLO}	nAn input; V_{CC}=0V to 3.6V;V_I=3.6V		500	-	-	uA

bus hold HIGH overdrive current	I_{BHHO}	nAn input; V_{CC}=0V to 3.6V;V_I=3.6V		-	-	-500	uA
external current	I_{EX}	nYn output in HIGH-state when $V_O > V_{CC}$;V_O = 5.5V; V_{CC} = 3.0V		-	60	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; n$\overline{OE}$ =don't care[4]		-	±1	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	V_O=3.0V	-	1	5	uA
			V_O=0.5V	-5	-1	-	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	output HIGH	-	0.12	0.19	mA
			output LOW	-	3	12	mA
			outputs disabled[5]	-	0.12	0.19	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V and other inputs at V_{CC} or GND[6]		-	0.1	0.2	mA
input capacitance	C_I	V_I=0V or 3.0V		-	4	-	pF
output capacitance	C_O	outputs disabled; V_O=0V or 3.0V		-	7	-	pF

Note:

[1] All typical values are at T_{amb}=25℃.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.2、AC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	nAn to nYn; see Figure 4	V_{CC}=2.7V	-	-	5.3	ns
			V_{CC}=3.0V to 3.6V	1	2.9	4.4	ns
HIGH to LOW propagation delay	t_{PHL}	nAn to nYn; see Figure 4	V_{CC}=2.7V	-	-	4.4	ns
			V_{CC}=3.0V to 3.6V	1	2.9	4.1	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nYn; see Figure 5	V_{CC}=2.7V	-	-	7.7	ns
			V_{CC}=3.0V to 3.6V	1	3.7	5.9	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nYn; see Figure 5	V_{CC}=2.7V	-	-	6.2	ns
			V_{CC}=3.0V to 3.6V	1.1	3.7	5.5	ns

HIGH to OFF-state propagation delay	t_{PHZ}	$n\overline{OE}$ to nYn; see Figure 5	V_{CC}=2.7V	-	-	6.8	ns
			V_{CC}=3.0V to 3.6V	1.9	4.3	6.1	ns
LOW to OFF-state propagation delay	t_{PLZ}	$n\overline{OE}$ to nYn; see Figure 5	V_{CC}=2.7V	-	-	4.5	ns
			V_{CC}=3.0V to 3.6V	1.8	3.3	4.5	ns

Note:

[1] All typical values are at V_{CC}=3.3V and T_{amb}=25℃.

4、Testing Circuit

4.1、AC Testing Circuit

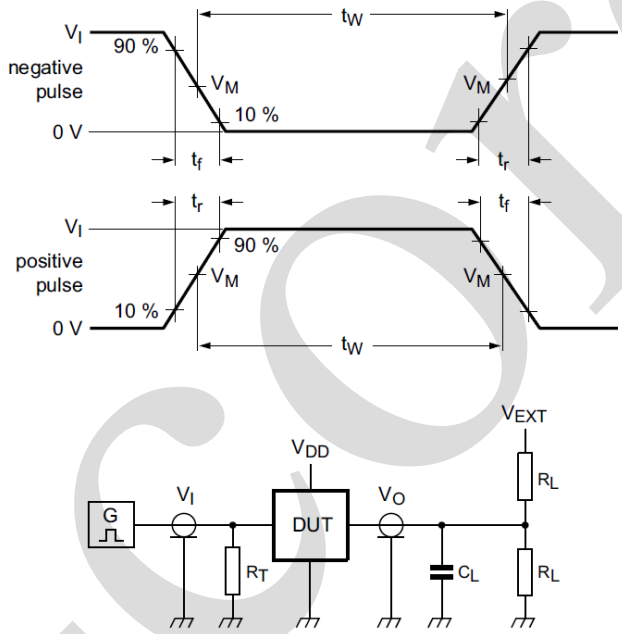


Figure 3. Load circuitry for switching times

Definitions test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

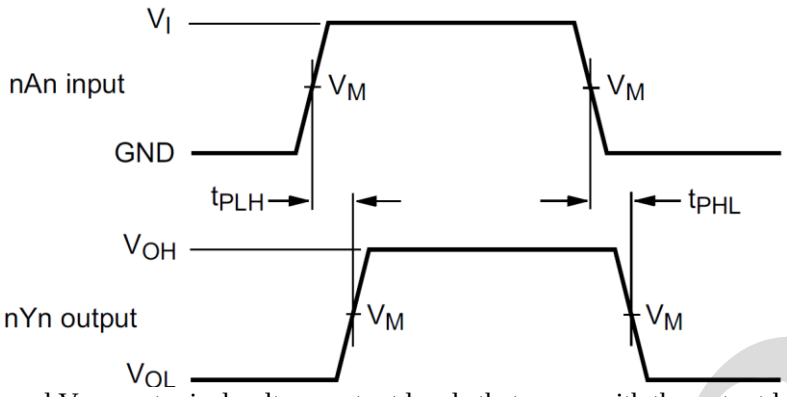
R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT}=Test voltage for switching times.

4.2、Test Data

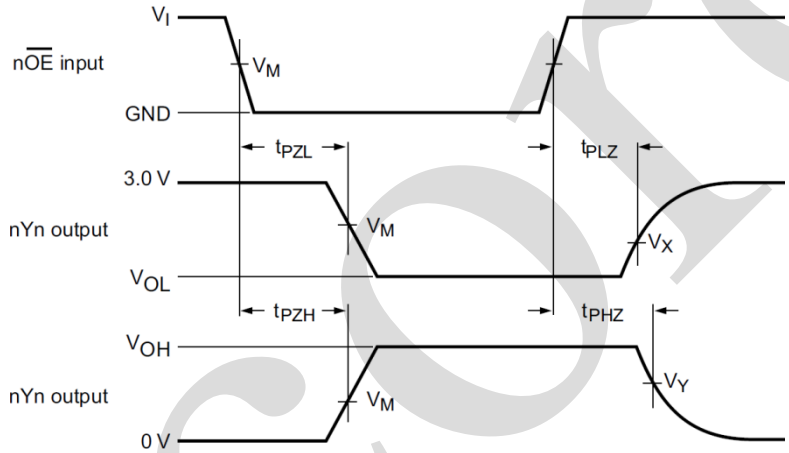
Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ},t_{PZH}	t_{PZH},t_{PLZ}	t_{PZL},t_{PLH}
2.7V	≤10MHz	500ns	≤2.5ns	50pF	500Ω	GND	6V	open

4.3、AC Testing Waveforms



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. Propagation delay input (nAn) to output (nYn) propagation delays



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

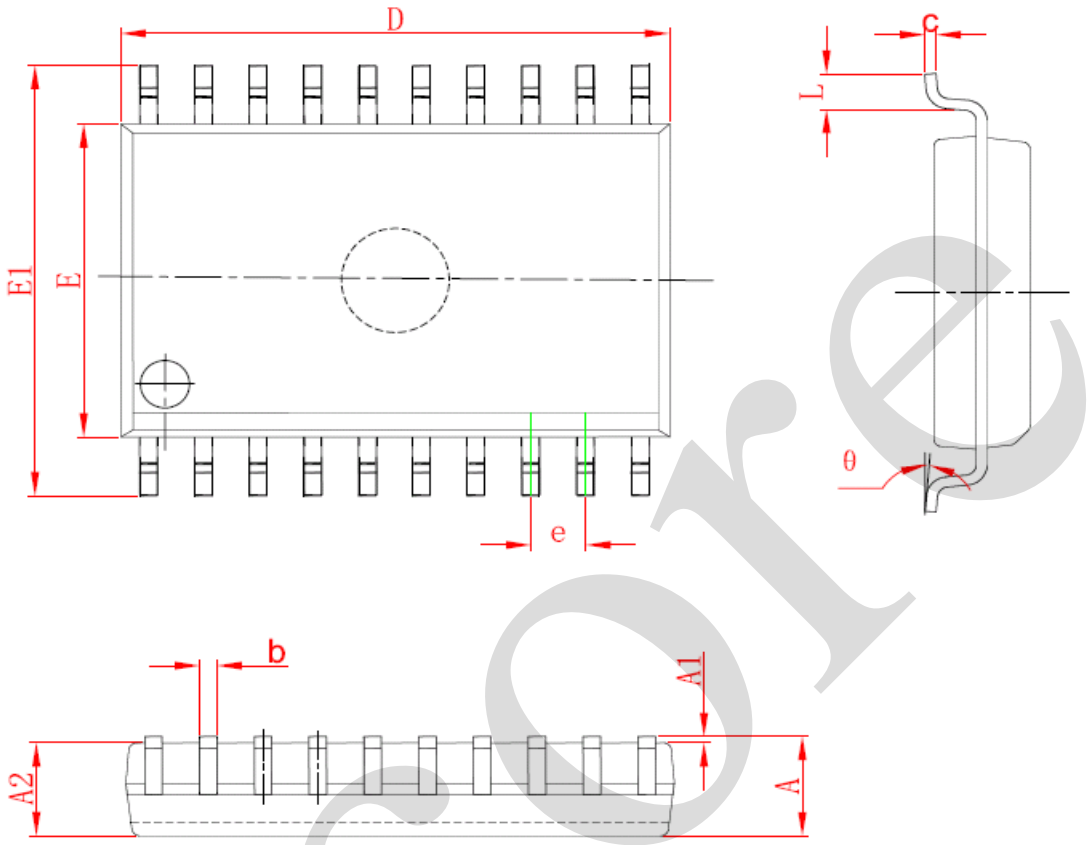
Figure 5. 3-state output enable and disable times

4.4、Measurement Points

Input	Output		
V_M	V_M	V_X	V_Y
1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

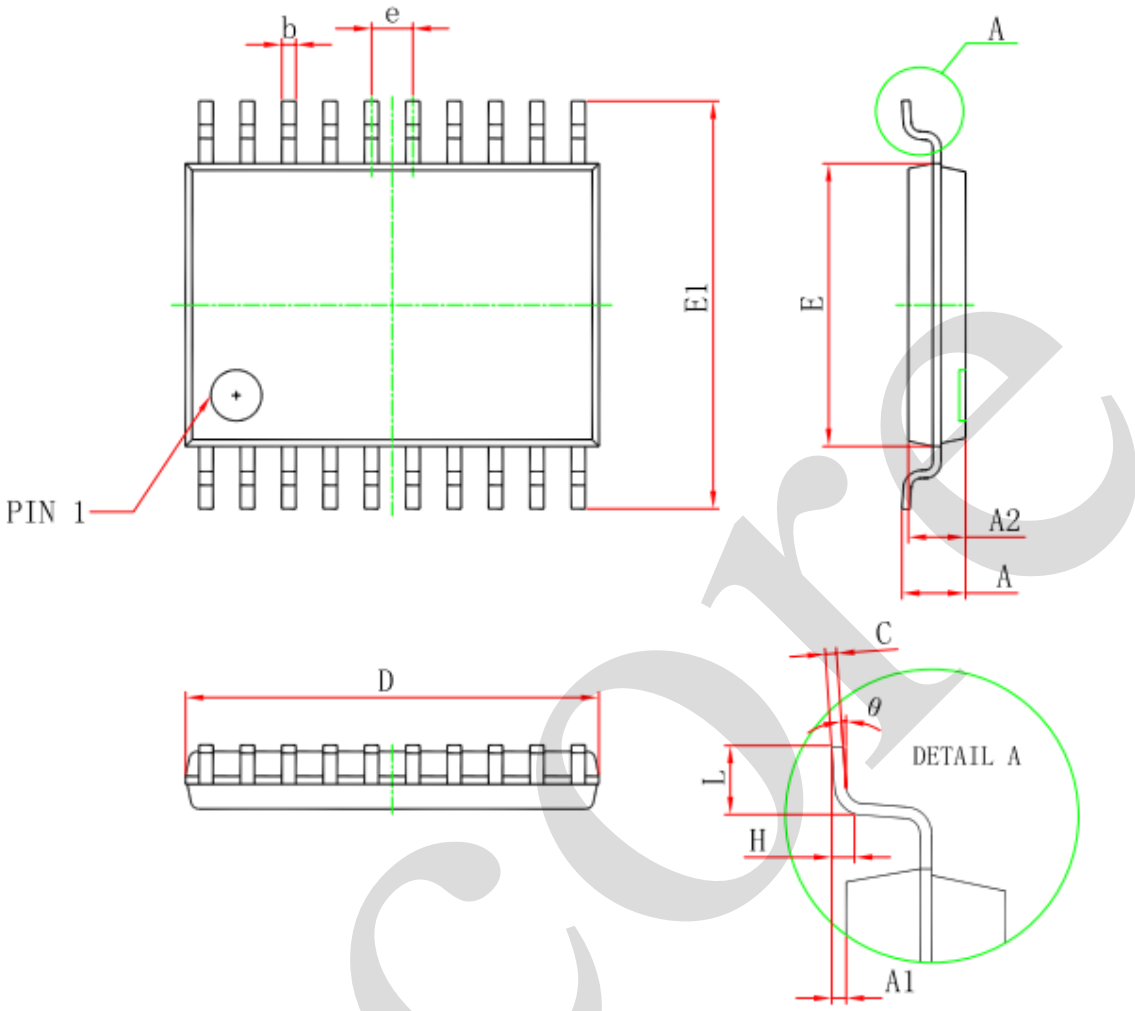
5、Package Information

5.1、SOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.2、TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

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