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YT6801/ YT6801S(H)

Datasheet

INTEGRATED 10/100/1000M GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

VERSION V1.02

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Revision History

Revision	Release Date	Summary
Draft 01	2021/12/27	First version.
Draft 02	2022/04/12	Modified mechanical information.
Draft 03	2022/05/28	Complete the LED related pin descriptions; Fix some typo;
Draft 04	2022/08/09	Add LDO/SWR description; Add DC Characteristics; Add Power Requirements; Add Thermal Resistance; Add Ordering Information;
Draft 05	2022/08/18	Add Power Sequence; Add Crystal Requirements; Add Oscillator Requirements;
Draft 06	2022/08/29	Fix pin assignment typo;
V1.01	2022/12/08	Add 5. Function Description; Add 9. PCI Express Bus Parameters; Add 10.5 Maximum Power Consumption;
V1.02	2022/02/08	Add Industrial Grade YT6801SH information;

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1. General Description

The YT6801/YT6801S is a single gigabit port Ethernet controller. It integrates IEEE802.3 Ethernet media access controller (MAC), single triple-speed physical layer (PHY) port, One Time Programmable (OTP) and PCI Express x1 controller. It is highly compacted to 32 pin QFN 4x4 package.

The embedded PHY is fully IEEE 802.3 standard compliant which supports 1000Base-T, 100Base-TX and 10Base-Te. With AFE, DFE, echo canceller, cross-talk canceller, packets transmit and receive at 1000Mbps rate with no error over 100m or longer CAT.5E cable. Besides, good ESD/Surge performance is also achieved due to the robust analog design. Other features, such as Auto-Crossover, polarity correction and EEE/smart-EEE are also supported.

The MAC supports full duplex and half duplex modes. Flow control is supported. It also introduces rich protocol offload functions: ARP/NS offload, TCP large send offload, TCP/UDP checksum offload, IPV4/IPV6 checksum offload. Receive-Side scaling (RSS) is supported to balance the loading of CPUs. Customer can remote wake up PC with WOL function which supports frame pattern matching, magic packet, link change and Microsoft WPI.

The PCIe 1.1 controller is enhanced to support various power states, including L0, L1, L1SS, L2 and L3. Together with ASPM/ACPI function, the whole system could enter various low power states, such as Sleep, Hibernation and Modern Stand-by, to save more power. And the controller supports Latency Tolerance Reporting (LTR). MSI and MSI-X are also supported.

Only 1 external power rail (3.3V) is needed. Analog and digital core power are generated by the built-in LDO (YT6801) and SWR regulator (YT6801S).

Note: YT6801S: Consumer Grade; YT6801SH: Industrial Grade.

1.1. Target Applications

- PCI Express 1000/100/10Mbps Ethernet on motherboard, notebook or embedded systems

2. Features

Ethernet PHY

- Single IEEE802.3 standard-compliant 10/100/1000Mbps transceiver
- Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Auto-Negotiation
- MDI/MDIX and auto crossover
- Polarity auto correction
- EEE and Smart EEE
- Link/power down power saving
- Crystal-less WOL

MAC

- IEEE 802.3 compliant over 1000/100/10Mbps rate
- IEEE 802.3P layer 2 priority encoding
- IEEE 802.3Q VLAN tagging
- IEEE 802.3az (EEE)
- Protocol offloading: ARP, NS
- Checksum offloading: IPV4, IPV6, TCP, UDP
- TCP segmentation task offloading: Large send v1/v2
- Receive-Side Scaling (RSS)
- WOL by magic packet, frame pattern matching, link change
- Microsoft Wake Packet Indication (WPI)
- Statistics MIB counters
- Jumbo frame up to 9KB
- Multicast filtering
- RX/TX flow control
- Interrupt moderation

PCI Express

- PCIe Ver1.1 1-lane 2.5Gbps

- Multiple power states: L0, L1, L1ss, L2, L3
- Latency Tolerance Reporting (LTR)
- PCIe MSI/MSI-X
- PME generation
- Out of Band wakeup

Interface

- Ethernet MDI interface
- PCI express x1 interface

Misc.functions

- 3 configurable LEDs
- Built-in LDO (YT6801) and SWR (YT6801S) to generate core power from 3.3V main power
- One Time Programmable (OTP)

Package

- 32 pin QFN 4x4 "Green" package

3. Block Diagram

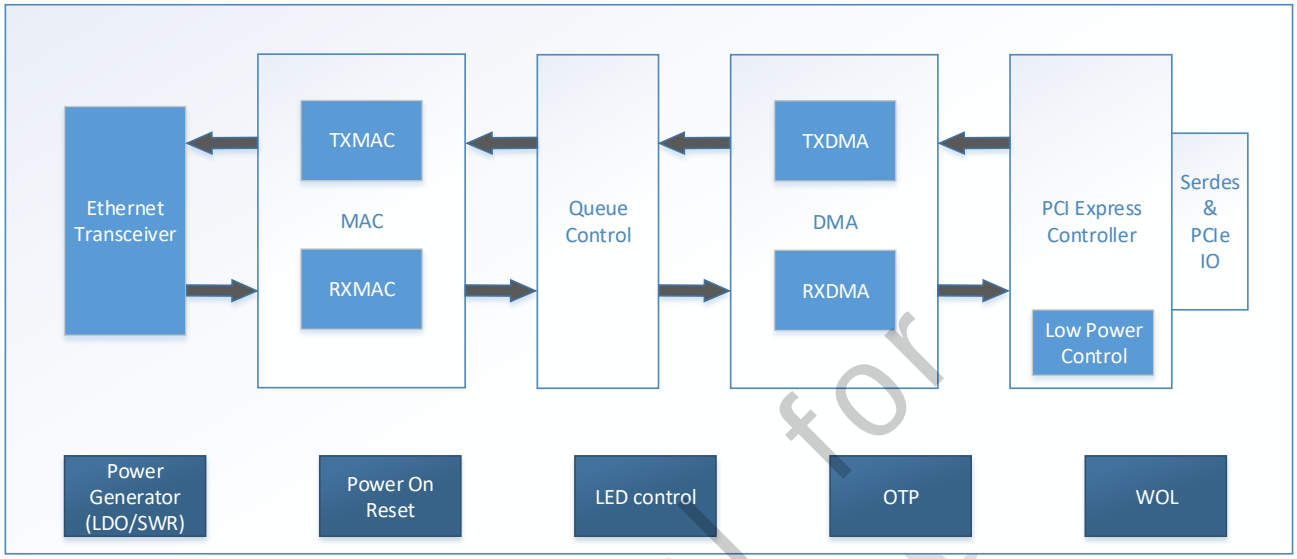
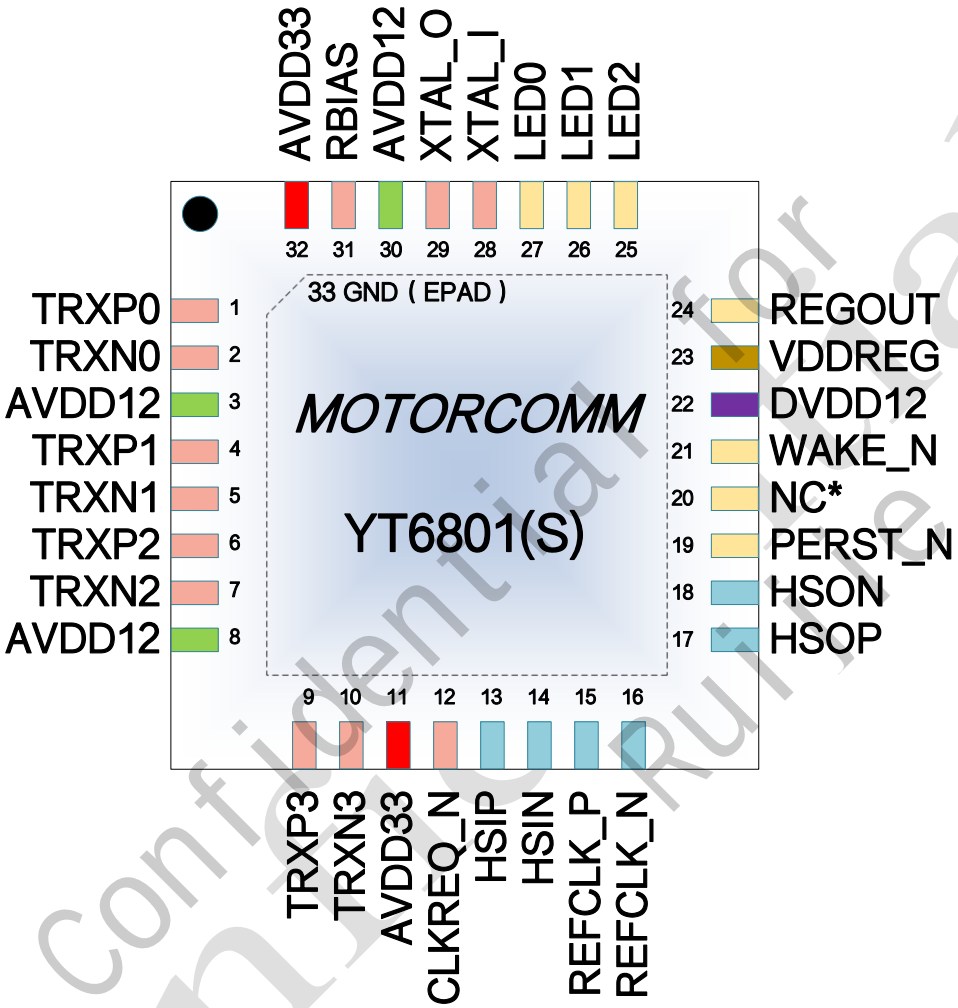


Figure 1. Block Diagram

4. Pin Assignment

4.1. YT6801(S) QFN32



Note:
The same color system represents the same power domain.
Red: AVDD33: Analog power 3.3V.
Yellow: VDDREG: Digital power 3.3V.
Blue: DVDD12 or AVDD12: Digital or Analog power 1.2V.
Green: AVDD12: Analog power 1.2V.
Purple: DVDD12: Digital power 1.2V.

**Note:*
Pin 20 is NC, which means no connection.

Figure 2. Pin Assignment Diagram

4.2. Pin Assignment

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Power
- G: Ground
- OD: Open Drain
- PU: Internal pull up
- PD: Internal pull down
- I_c: 1.8V/3.3V compatible input

Table 1. Pin Assignment

No.	Pin Name	Type
1	TRXP0	IO
2	TRXN0	IO
3	AVDD12	P
4	TRXP1	IO
5	TRXN1	IO
6	TRXP2	IO
7	TRXN2	IO
8	AVDD12	P
9	TRXP3	IO
10	TRXN3	IO
11	AVDD33	P
12	CLKREQ_N	I_c/OD/PU
13	HSIP	I
14	HSIN	I
15	REFCLK_P	I
16	REFCLK_N	I

No.	Pin Name	Type
17	HSOP	O
18	HSON	O
19	PERST_N	I_c/PD
20	NC	
21	WAKE_N	I_c/OD/PU
22	DVDD12	P
23	VDDREG	P
24	REGOUT	O
25	LED2	O/PD
26	LED1	O/PD
27	LED0	O/PU
28	XTAL_I	I
29	XTAL_O	IO
30	AVDD12	P
31	RBIAS	I
32	AVDD33	P
33	GND	G

4.3. Transceiver Interface

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
1	TRXP0	IO	Media-dependent interface 0, 100Ω transmission line
2	TRXN0	IO	Media-dependent interface 0, 100Ω transmission line
4	TRXP1	IO	Media-dependent interface 1, 100Ω transmission line
5	TRXN1	IO	Media-dependent interface 1, 100Ω transmission line
6	TRXP2	IO	Media-dependent interface 2, 100Ω transmission line
7	TRXN2	IO	Media-dependent interface 2, 100Ω transmission line
9	TRXP3	IO	Media-dependent interface 3, 100Ω transmission line
10	TRXN3	IO	Media-dependent interface 3, 100Ω transmission line

4.4. Clock

Table 3. Clock

No.	Pin Name	Type	Description
28	XTAL_I	I	25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
29	XTAL_O	IO	25Mhz Crystal Output pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

4.5. PCI Express Interface

Table 4. PCI Express Interface

No.	Pin Name	Type	Description
12	CLKREQ_N	I_o/OD	YT6801(S) uses this signal to request starting of the PCI Express reference clock. Open drain; active low, 1.8V/3.3V compatible input/output mode, with weak external pull-up resistor. The L1 off mechanism also uses this signal. In this case, CLKREQ_N can be set by the system or YT6801(S) to initiate L1 exit.
13	HSIP	I	PCI Express interface, receive differential line.

14	HSIN	I	PCI Express interface, receive differential line.
15	REFCLK_P	I	PCI Express interface, differential reference clock source: 100MHz ± 300ppm.
16	REFCLK_N	I	PCI Express interface, differential reference clock source: 100MHz ± 300ppm.
17	HSOP	O	PCI Express interface, transmit differential line.
18	HSON	O	PCI Express interface, transmit differential line.
19	PERST_N	I_o/PD	PCI Express interface: fundamental reset 1.8V/3.3V compatible input, active low. When PERST_N is set in the power-on state, YT6801(S) returns to the specified values reset state which is defined in the PCI Express spec. and is ready to initialize and configure after PERST_N is deactivated.

4.6. LED Default Settings

Table 5. LED Default Settings

No.	Pin Name	Type	Description
25	LED2	O/PD	Light = Link up at 1000Mbps Blinking = Transiting or Receiving This is configurable. This pin should be pulled down for the YT6801(S) to work properly.
26	LED1	O/PD	Light = Link up at 100Mbps Blinking = Transiting or Receiving This is configurable. This pin should be pulled down for the YT6801(S) to work properly.
27	LED0	O/PU	Light = Link up at 10Mbps Blinking = Transiting or Receiving This is configurable. This pin should be pulled down for the YT6801(S) to work properly.

4.7. Regulator and Reference

Table 6. Regulator and Reference

No.	Pin Name	Type	Description
23	VDDREG	P	Digital 3.3V power supply for switching or LDO regulator.
24	REGOUT	O	LDO regulator 1.2V output for YT6801. Switching regulator 1.2V output for YT6801S.

31	RBIAS	I	Bias Resistor. An external 2.49 kΩ ± 1% resistor must be connected between the RBIAS pin and GND.

4.8. Power Related

Table 7. Power Related

No.	Pin Name	Type	Description
3, 8, 30	AVDD12	P	Analog power 1.2V.
22	DVDD12	P	Digital power 1.2V.
11, 32	AVDD33	P	Analog power 3.3V.
33	GND	G	Exposed PAD.

4.9. Management

Table 8. Management

No.	Pin Name	Type	Description
21	WAKE_N	I_o/OD/PU	Power management events (PME): open drain; active low, 1.8V/3/3V compatible input/output mode, with weak external pull-up resistor. Through this, the main power rail and reference clock of the slot can be restored, and then the link can be wake up, which is defined in the PCI Express CEM spec.

5. Function Description

5.1. PCI Express Bus Interface

The YT6801/YT6801S is compliant with PCI Express Base Specification Revision 1.1, and operates at a signaling rate of 2.5GHz with a link width of X1. It has one transmit and one receive differential pair.

5.1.1. PCI Express Transmitter

The PCI Express block of the YT6801/YT6801S receives digital data from the Ethernet interface and scrambles the data into 10-bit coded groups using linear feedback shift registers (LFSR) and 8B/10B coding techniques. Data scrambling is used to reduce the possibility of electrical resonance on the link and the 8B/10B encoding technique is used to increase the system overhead by adding two extra bits to facilitate embedded clocking, error detection and DC balancing. The data coding groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted via a differential driver to its upstream device.

5.1.2. PCI Express Receiver

The PCI Express block of the YT6801/YT6801S receives 2.5Gbps of serial data from its upstream device to generate parallel data. The receiver's PLL circuitry is re-synchronized to maintain bit and symbol lock. With 8B/10B decoding techniques and data descrambling, the original digital data is recovered and passed to the internal Ethernet MAC of the YT6801/YT6801S for transmission to the Ethernet media.

5.2. Customizable LED Configuration

The YT6801/YT6801S supports customizable LED operation modes via eFuse autoload register. The eFuse of YT6801/YT6801S defines the Byte0 bit4:0 of RegionA as the control of the LED, the Bit4:0 indicates the index of the LED lighting solution, different indexes have different LED behaviors:

5.2.1. Config Index 0

Table 9. Index_0 LED Behavior in Different Operating Modes and Power States

Power State	Operating Mode	LED0	LED1	LED2
S0	Link Down	Off	Off	Off
	Link Up at 1000M	Off	On	Off
	Traffic at 1000M	Blinking	On	Off
	Link Up at 100M	Off	On	Off
	Traffic at 100M	Blinking	On	Off
	Link Up at 10M	Off	On	Off
	Traffic at 10M	Blinking	On	Off
S3/S4/S5	/	Off	Off	Off

5.2.2. Config Index 1

Table 10. Index_1 LED Behavior in Different Operating Modes and Power States

Power State	Operating Mode	LED0	LED1	LED2
S0	Link Down	Off	Off	Off
	Link Up at 1000M	Off	Off	Off
	Traffic at 1000M	Off	Off	Off
	Link Up at 100M	Off	Off	Off
	Traffic at 100M	Off	Off	Off
	Link Up at 10M	Off	Off	Off
	Traffic at 10M	Off	Off	Off
S3/S4/S5	/	Off	Off	Off

5.2.3. Config Index 2

Table 11. Index_2 LED Behavior in Different Operating Modes and Power States

Power State	Operating Mode	LED0	LED1	LED2
S0	Link Down	Off	Off	Off
	Link Up at 1000M	Off	On	Blinking
	Traffic at 1000M	Off	On	Blinking
	Link Up at 100M	On	Off	Blinking
	Traffic at 100M	On	Off	Blinking
	Link Up at 10M	Off	Off	Blinking
	Traffic at 10M	Off	Off	Blinking
S3/S4/S5	/	Off	Off	Off

The YT6801/YT6801S also supports LED blinking frequency control. And for more customized LED behavior solutions, please contact us to support to meet the requirements.

5.3. PHY Transceiver

Based on state-of-the-art DSP technology and mixed-mode signal processing, the YT6801/YT6801S operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), 2-pair CAT.5 UTP cable (100Mbps), or CAT.3 UTP cable (10Mbps).

5.3.1. PHY Transmitter

GMII (1000Mbps) Mode

The PCS layer of the YT6801/YT6801S receives data bytes from the MAC through the GMII interface and generates sequential code sets via 4D five-level PAM coding techniques. These code sets are passed through a waveform shaping filter to minimize EMI effects and transmitted to 4 pairs of CAT5 cables at 125MBaud/s via a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles from the MAC (TXD[3:0]), clocked at 25MHz (TXC), are converted to 5B symbol codes by 4B/5B coding techniques, and then converted to 125MHz NRZ and NRZI signals by scrambling and serialization. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter, and transmitted to the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5/MHz (TXC), are serialized to 10 Mbps serial data. 10 Mbps serial data is converted to a Manchester-encoded data stream and transmitted to the media by the D/A converter.

5.3.2. PHY Receiver

GMII (1000Mbps) Mode

The input signal from the media is passed through a complex on-chip hybrid circuit that separates the transmitted signal from the input signal to effectively reduce near-end echoes. The received signal is processed with state-of-the-art techniques such as adaptive equalization, BLW (Baseline Wander) correction, crosstalk cancellation, echo cancellation, timing recovery, error correction and 4D five-level PAM decoding. 8-bit wide data is recovered and sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves packets from the receive MII/GMII interface and sends them to the RX buffer manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoders, descrambler, 4B/5B decoder, and then presented to the MII interface in 4-bit wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is first converted into a Manchester encoded stream. Next, this data stream is processed by the Manchester decoder and deserialized into 4-bit wide nibbles. These 4-bit nibbles are presented to the MII interface at a clock speed of 2.5 MHz.

5.3.3. Link Down Power Saving Mode

The YT6801/YT6801S implements link down power saving; greatly reducing power consumption when the network cable is disconnected. The YT6801/YT6801S automatically enters link down power saving mode 10 seconds after the network cable is disconnected. Once it enters link down power saving mode, it transmits normal link pulses on its TX pin and continues to monitor the RX pin to detect incoming signals. After detecting an incoming signal, it wakes up from link down power saving mode and operates in normal mode based on the result of the connection.

5.3.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 and manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

5.4. Power Management

The YT6801/YT6801S are compliant with ACPI (Rev 1.0, 1.0b, 2.0, 3.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), for example, supporting an Operating System-directed Power Management (OSPM) environment.

The YT6801/YT6801S can monitor the network for wake-up frames or magic packets and notify the system via WAKE_N pin and PCI Express Power Management Event (PME) messages when such packets or events occur. The system can then be restored to a normal state to process incoming jobs.

When the YT6801/YT6801S is in power-down mode (D1~D3):

- The RX state machine is stopped. the YT6801/YT6801S monitors the network for wake-up events, such as Magic Packet and Wake-Up Frame, to wake up the system. When in power-down mode, the YT6801/YT6801S does not reflect the status of any incoming packets in the ISR registers and does not receive any packets into the RX on-chip buffers.
- The YT6801/YT6801S holds the on-chip buffer status and the packets that have been received into the RX on-chip buffer before entering power-down mode.
- The transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held.
- After restoring to the D0 state, the YT6801/YT6801S transmits data that was not moved into the TX on-chip buffer during the power-down mode. Packets that were not fully transmitted last time are retransmitted.

A magic packet wake up will only occur if the following conditions are met:

- The destination address of a received Magic Packet is acceptable to the YT6801/YT6801S, e.g., a broadcast, multicast, or unicast packet addressed to the current YT6801/YT6801S.

- The received Magic Packet does not contain a CRC error.
- The YT6801/YT6801S driver has the required registers set (automatically) and the WAKE_N and PME messages can be asserted in the current power state.
- Magic Packet pattern matching, i.e. 6 * FFh + MISC (can be none) + 16 * DID (destination ID) in any part of a valid Ethernet packet.

A wake-up frame event occurs only when the following conditions are met:

- The destination address of the received wake-up frame is acceptable to the YT6801/YT6801S, e.g., a broadcast, multicast or unicast address to the current YT6801/YT6801S.
- The received wake-up frame does not contain CRC errors.
- The YT6801/YT6801S driver has set the required registers (automatic setting).
- The 16-bit CRC of the received wake-up frame matches the 16-bit CRC of the sample wake-up frame given by the local machine's operating system. Alternatively, the YT6801/YT6801S is configured to allow direct packet wake-up, e.g., a broadcast, multicast or unicast network packet.
- The 128 bytes of the received wake-up frame exactly match the 128 bytes of the sample wake-up frame given by the local machine's operating system.

The corresponding wake-up method (message or WAKE_N) is only asserted when the following conditions are met:

- The PME_En bit (bit8, PMCSR) in the PCI configuration space is set to 1.
- YT6801/YT6801S can assert the WAKE_N and PME messages, depending on the PME_Support (bits 15~11) setting of the PMC register in the PCI configuration space.
- A Magic Packet, Link Change, or Wake-Up Frame pattern has been received.
- Write a 1 to PME_Status (bit15) of the PMCSR register in the PCI configuration space to clear this bit and cause the YT6801/YT6801S to stop asserting the WAKE_N and PME messages if enabled.

5.5. Receive Side Scaling (RSS)

The YT6801/YT6801S are compliant with the Network Driver Interface Specification (NDIS) 6.0 Receive Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS is a network adapter driver technology that enables efficient distribution of network receive packet processing power across multiple processors in a multicore system, thereby spreading the CPU load, leveraging the power of multiple processors, and increasing the capacity and efficiency of data reception.

5.6. Energy Efficient Ethernet (EEE)

The YT6801/YT6801S supports IEEE 802.3az-2010 at 10Mbps, 100Mbps, and 1000Mbps, also known as Energy Efficient Ethernet (EEE). It provides a protocol to coordinate the transition to/from a lower power consumption level (low power idle mode) based on the link utilization. When no packets are being transmitted, the system goes into low-power idle mode to save power. Once packets need to be

transmitted, the system returns to normal mode and does this without changing the link state and without corrupting/dropping frames.

To save power, most circuits are disabled when the system is in low power idle mode, however, the transition time into/out of low power idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method that enables the link partner to determine whether to support EEE and to select the best set of parameters common to both devices.

For more detailed information, please refer to: https://www.ieee802.org/3/az/index.html

5.7. Latency Tolerance Reporting (LTR)

The YT6801/YT6801S supports Latency Tolerance Reporting (LTR).

The LTR mechanism enables endpoints to report the service latency requirements for memory reads/writes. The CPU utilizes LTR to determine transfers from low power (C10) to high power (C0) modes.

For more detailed information, please refer to PCIe Specification.

5.8. Microsoft Wake Packet Indication (WPI)

The YT6801/YT6801S supports Microsoft's Wake Packet Indication (WPI), which provides wake-up frame information to the operating system, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPI helps prevent unwanted/unauthorized wake-up of a sleeping computer.

For more detailed information, please refer to Microsoft Windows Hardware Certification Requirements.

5.9. L1 and L1ss

The YT6801/YT6801S supports PCIe L1 and L1ss power management features. PCIe L1 and L1ss are intended as a power savings state. The L1ss (L1.1 L1.2) state allows an additional power savings over L1 at the cost of additional resume latency. L1 PM substates establish a link power management regime that creates lower power substates of the L1 link state, and associated mechanisms for using those substates.

Table 12. L1 and L1ss PCIe Port Circuit Power On/Off

State	PLL	Rx/Tx	Common Mode Keepers
L1	On	Off/Idle	On
L1.1	Off	Off/Idle	On
L1.2	Off	Off/Idle	On

5.10. Wake-On-LAN (WOL)

The YT6801/YT6801S supports Wake-On-LAN (WOL), a power management feature that allows the device to wake the operating system from standby or hibernate mode if there is network activity. The YT6801/YT6801S supports the following ways for wake-up:

- Magic Packet
- Frame Pattern Matching
- Link Change

5.11. Crystal-less WOL

The YT6801/YT6801S supports board-level designs with an external 25MHz clock source instead of a crystal.

When in suspend mode (S3/S4/S5), the external clock source may stop generating the clock. To support Wake-On-LAN(WOL) function without external clock source, the YT6801/YT6801S will automatically change the source clock from external to internal self-oscillating auxiliary clock when entering suspend mode.

Please note that in suspend mode, the auxiliary clock can only establish a 10Mbps link for Ethernet PHY.

6. LDO Regulator (YT6801 Only)

The YT6801 integrates a linear low dropout (LDO) regulator with high supply ripple rejection and low output noise. the YT6801 embedded LDO regulator does not require a power inductor on the PCB. Only a 1.2V output capacitor for phase compensation needs to be placed between its 1.2V output and analog ground, which saves cost and PCB space.

The output capacitor (and bypass capacitor) should be located as close as possible to the power supply pins (AVDD12 and DVDD12) to allow for adequate filtering.

Please note that the 1.2V output pin (REGOUT) of the LDO regulator must be connected to DVDD12 and AVDD12 only (please do not supply this power to other devices).

7. Switching Regulator (YT6801S(H) Only)

The YT6801S uses a advanced switching regulator and requires a well-designed PCB layout to achieve good power supply efficiency with reduced output voltage ripple and input overshoot.

Please note that the 1.2V output pin (REGOUT) of the switching regulator must be connected to DVDD12 and AVDD12 only (please do not supply this power to other devices).

8. Timing and DC Characteristics

8.1. DC Characteristics

Table 13. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AVDD33	3.3V Supply Mean Voltage	–	2.97	3.3	3.63	V
AVDD12, DVDD12	1.2V Supply Mean Voltage	–	1.08	1.2	1.32	V
Voh	Minimum High Level Output Voltage	Ioh = −4mA	0.9*VDD33	–	AVDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	–	0.1*AVDD33	V
Vih	Minimum High Level Input Voltage for 3.3V & 1.8 V compatible Pinout	–	1.50	–	–	V
	Minimum High Level Input Voltage for 3.3V only Pinout	–	2	–	–	V
Vil	Maximum Low Level Input Voltage	–	–	–	0.8	V

8.2. Crystal Requirements

Table 14. Crystal Requirements

Symbol	Description/ Condition	Min	Typ	Max	Units
Fref	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type	–	25	–	MHz
Fref Stability	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. Ta=0°C~70°C	-30	–	+30	ppm
Fref Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. Ta=25°C	-50	–	+50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	–	60	%
ESR	Equivalent Series Resistance	–	–	50	ohm

DL	Drive Level	–	–	0.3	mW

8.3. Oscillator Requirements

Table 15. Oscillator Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency	–	–	25	–	MHz
Frequency Stability	Ta=0°C~70°C	-30	–	+30	ppm
Frequency Tolerance	Ta=25°C	-50	–	+50	ppm
Duty Cycle	–	40	–	60	%
Broadband Peak-to-Peak Jitter	–	–	–	200	ps
Vih	–	1.4	–	–	V
Vil	–	–	–	0.4	V
Rise Time	–	–	–	10	ns
Fall Time	–	–	–	10	ns
Operation Temp Range	–	0	–	70	℃

9. PCI Express Bus Parameters

9.1. Differential Transmitter Parameters

Table 16. Differential Transmitter Parameters

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.80	-	1.20	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eve Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω

$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+ 2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note 1: For the correct measurement environment settings for each parameter, refer to the PCI Express Base Specification, Revision 1.1.

Note 2: The data rate can be modulated with an SSC (spread spectrum clock) of +0 to -0.5% of the nominal data rate frequency, with a modulation rate in the range of no more than 30kHz-33kHz. The ± 300ppm requirement still exists, which requires modulation of both communication ports so that the total difference does not exceed 600ppm.

9.2. Differential Receiver Parameters

Table 17. Differential Receiver Parameters

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.20	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between The Jitter Median and Maximum Deviation from The Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	100k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note 1: For the correct measurement environment settings for each parameter, refer to the PCI Express Base Specification, Revision 1.1.

9.3. REFCLK Parameters

Table 18. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units
		Min	Max	
Rise Edge Rate	Rising Edge Rate of Differential Waveform	0.6	4.0	V/ns
Fall Edge Rate	Falling Edge Rate of Differential Waveform	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150	–	mV
V_{IL}	Differential Input Low Voltage	–	−150	mV
V_{CROSS}	Absolute Crossing Point Voltage of Single-Ended Waveform	+250	+550	mV
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges of Single-Ended Waveform	–	+140	mV
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy of Differential Waveform	−300	+300	ppm
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum) of Differential Waveform	9.847	10.203	ns
$T_{C-to-C-JITTER}$	Cycle to Cycle Jitter of Differential Waveform	–	150	ps
V_{MAX}	Absolute Maximum Input Voltage of Single-Ended Waveform	–	+1.15	V
V_{MIN}	Absolute Minimum Input Voltage of Single-Ended Waveform	−0.3	–	V
Duty Cycle	Duty Cycle of Differential Waveform	40	60	%
Rise-Fall Matching	Rising Edge Rate (REFCLK+) of Single-Ended Waveform to Falling Edge Rate (REFCLK−) of Single-Ended Waveform Matching	–	20	%
Z_{C-DC}	Clock Source DC Impedance of Single-Ended Waveform	40	60	Ω

Note 1: Rise/Fall Edge Rate is measured from −150mV to +150ml on the differential waveform (derived from REFCLK+ minus REFCLK−). The signal must be monotonic through the measurement region for rise and fall time. The 300ml measurement window is centered on the differential zero crossing.

Note 2: V_{CROSS}/ $V_{CROSS\ DELTA}$ is measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK−. V_{CROSS} refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing and refers to all crossing points for this measurement. And $V_{CROSS\ DELTA}$ is defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK−. This is the maximum allowed variance in V_{CROSS} for any particular system.

*Note 3: $T_{PERIOD\ AVG}$ refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations. PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm *300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater:*

Note 4: $T_{PERIOD\ ABS}$ is defined as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

Note 5: V_{MAX} is defined as the maximum instantaneous voltage including overshoot. And V_{MIN} is defined as the minimum instantaneous voltage including undershoot.

Note 6: Rise-Fall Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK−. It is measured using a +75ml window centered on the median cross point where REFCLK+ rising meets REFCLK− falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK−; the maximum allowed difference should not exceed 20% of the slowest edge rate.

10. Power Requirements

10.1. Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
AVDD33	Supply Voltage 3.3V	−0.3	3.7	V
AVDD12; DVDD12	Supply Voltage 1.2V	−0.2	1.4	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	−0.3	3.7	V
1.2V DCinput 1.2V DCoutput	Input Voltage Output Voltage	−0.3	1.4	V
N/A	Storage Temperature	−55	+125	℃

10.2. Recommended Operating Conditions

Table 20. Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Units
Supply Voltage	AVDD33	2.97	3.3	3.63	V
	AVDD12; DVDD12	1.08	1.2	1.32	V
Ambient Operating Temperature Ta (YT6801/YT6801S)		0	–	70	℃
Ambient Operating Temperature Ta (YT6801SH)		−40	–	85	℃
Maximum Junction Temperature		–	–	125	℃

10.3. Power Sequence

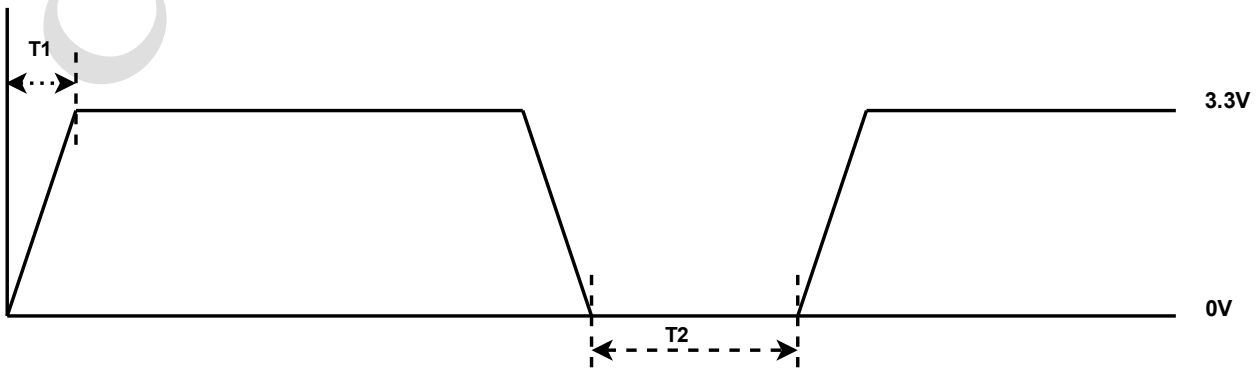


Figure 3. Power Sequence

Table 21. Power Sequence Parameters

Symbol	Description	Min	Typ	Max	Units
T1	3.3V rising time	0.5	–	100	ms
T2	3.3V off time	100	–	–	ms

10.4. Power Consumption

Table 22. YT6801 Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Link Down	49	106	511
Traffic @1000Mbps	91	228	1052

Table 23. YT6801S Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Link Down	48	46	310
Traffic @1000Mbps	89	112	663

10.5. Maximum Power Consumption

Table 24. YT6801 Maximum Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Traffic @1000Mbps	96	255	1158.3

Table 25. YT6801S Maximum Power Consumption

Condition	AVDD33 (mA)	VDDREG (mA)	Power Consumption (mW)
Traffic @1000Mbps	95	130	742.5

Note: Test by YT6801/YT6801S FF corner IC in 1000Mbps bidirectional traffic mode with AVDD33/VDDREG = 3.3V at high temperature 85℃.

11. Thermal Resistance

11.1. YT6801

Table 26. YT6801 Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θ JA	Thermal resistance – junction to ambient θ JA = (TJ – TA)/ P P = Total power dissipation	JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=25° C	40.57	° C/W
		JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=70° C	40.6	° C/W
θ JB	Thermal resistance – junction to board θ JB = (TJ – TB)/ Pbottom Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	12.2	° C/W
θ JC	Thermal resistance – junction to case θ JC = (TJ – TC)/ Ptop Ptop = Power dissipation from the top of the package	JEDEC with no air flow	24.6	° C/W

11.2. YT6801S(H)

Table 27. YT6801S Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θ JA	Thermal resistance – junction to ambient θ JA = (TJ – TA)/ P P = Total power dissipation	JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=25° C	41.6	° C/W
		JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow TA=70° C	41.54	° C/W
θ JB	Thermal resistance – junction to board θ JB = (TJ – TB)/ Pbottom Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	12.2	° C/W
θ JC	Thermal resistance – junction to case θ JC = (TJ – TC)/ Ptop Ptop = Power dissipation from the top of the package	JEDEC with no air flow	24.6	° C/W

12. Mechanical Information

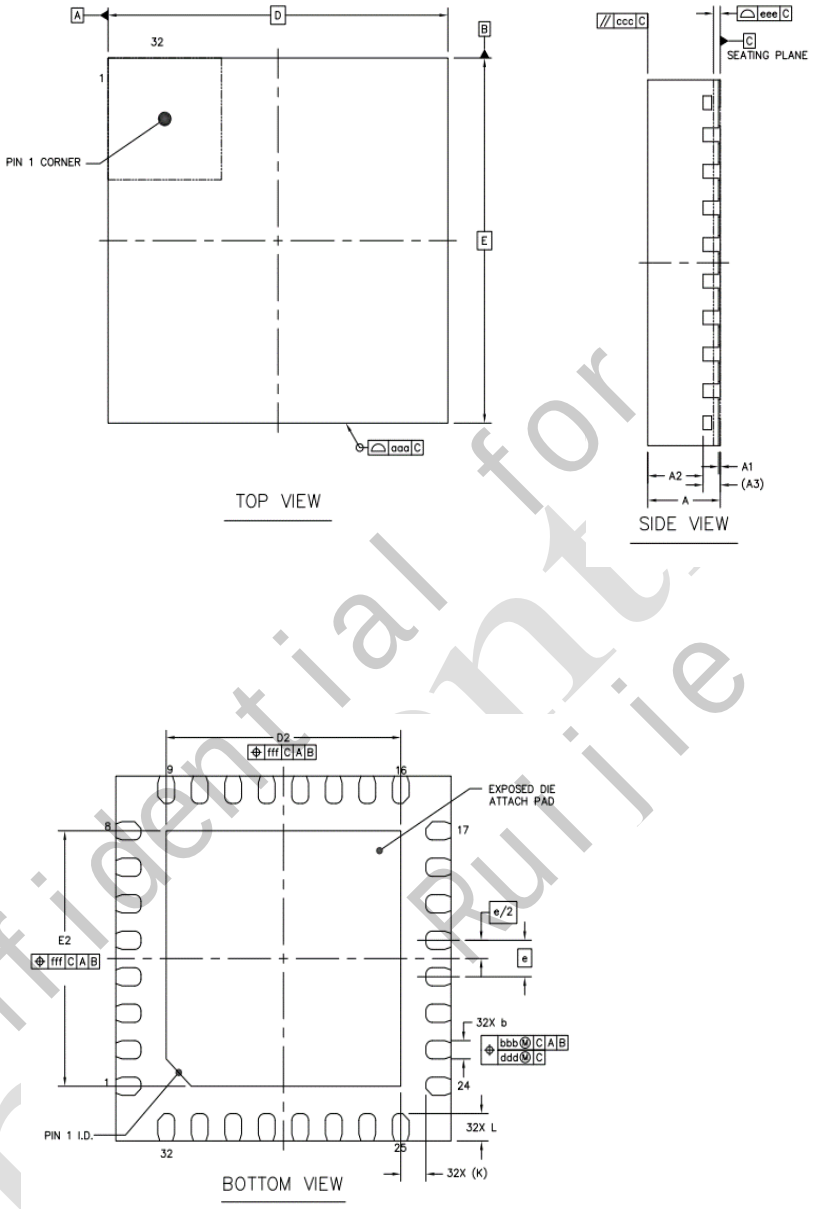


Figure 4. Package Outline Drawing

Table 28. Mechanical Dimensions in mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	4 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	2.6	2.75	2.9
	Y	E2	2.6	2.75	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K	0.3	0.35	0.4

13. Ordering Information

Table 29. Ordering Information

Part number	Grade	Package	Pack	Status	Operation Temp
YT6801S	Consumer	QFN32 EPAD	Tape Reel 3000 ea	Mass Product	0~70℃
YT6801	Consumer	QFN32 EPAD	Tape Reel 3000 ea	Mass Product	0~70℃
YT6801SH	Industrial	QFN32 EPAD	Tape Reel 3000 ea	Engineering Sample	-40~85℃