HARRIS SEMICONDUCTOR

IRFR110, IRFU110

4.7A, 100V, 0.54 Ohm, N-Channel Power MOSFETs

January 1998

Features

- **4.7A, 100V**
- **$r_{DS(ON)} = 0.54\Omega$**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **175°C Operating Temperature**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFU110	TO-251AA	IFU110
IRFR110	TO-252AA	IFR110

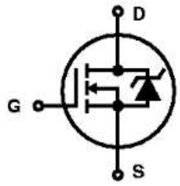
NOTE: When ordering, use the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

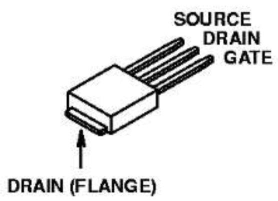
Formerly developmental type TA17441.

Symbol

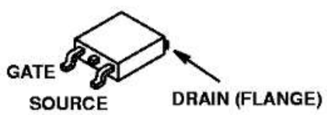


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3275.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFR110, IRFU110	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	4.7	A
$T_C = 100^oC$	I_D	3.3	A
Pulsed Drain Current (Note 4)	I_{DM}	17	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	30	W
Linear Derating Factor		0.2	$W/^oC$
Single Pulse Avalanche Rating (Note 3)	E_{AS}	19	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

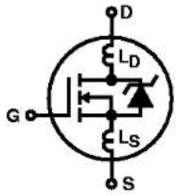
NOTE:

1. $T_J = 25^oC$ to 150^oC.

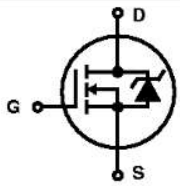
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 10)	100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$	-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, $V_{GS} = 0V$, $T_J = 150^oC$	-	-	250	µA
On-State Drain Current	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10V$	4.7	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm20V$	-	-	±100	nA
Drain to Source On Resistance (Note 4)	$r_{DS(ON)}$	$I_D = 3.3A$, $V_{GS} = 10V$ (Figures 8, 9)	-	0.41	0.54	Ω
Forward Transconductance (Note 4)	g_{fs}	$V_{DS} = 50V$, $I_{DS} = 3.3A$ (Figure 12)	1.3	2.0	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 50V$, $I_D \approx 5.6A$, $R_G = 24\Omega$, $R_L = 9.1\Omega$, $V_{GS} = 10V$ (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	7.6	11	ns
Rise Time	t_r		-	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	21	ns
Fall Time	t_f		-	14	21	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 10V$, $I_D \approx 5.6A$, V_{DS} = 0.8 x Rated BV_{DSS}, $R_L = 14\Omega$, $I_{G(REF)} = 1.5mA$ (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	5.2	7.7	nC
Gate to Source Charge	Q_{gs}		-	1.5	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	2.2	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0MHz (Figure 11)	-	180	-	pF
Output Capacitance	C_{OSS}		-	82	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	15	-	pF

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from The Source Lead, 6mm (0.25in) from Header to Source Bonding Pad		-	7.5	-	nH
Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	110	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 	-	-	4.7	A
Pulse Source to Drain Current (Note 2)	I_{SDM}		-	-	17	A
Source to Drain Diode Voltage (Note 4)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 4.7A$, $V_{GS} = 0V$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 5.6A$, $dI_{SD}/dt = 100A/\mu s$	46	96	200	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 5.6A$, $dI_{SD}/dt = 100A/\mu s$	0.17	0.38	0.83	μC

NOTES:

2. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
3. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 1.3mH, $R_G = 25\Omega$, peak $I_{AS} = 4.7A$.
4. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.

Typical Performance Curves Unless Otherwise Specified

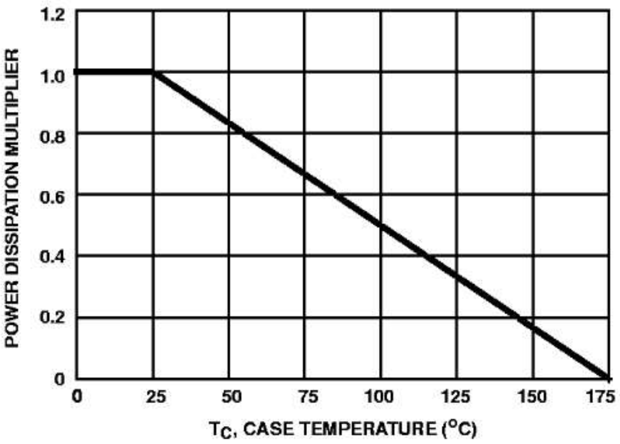


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

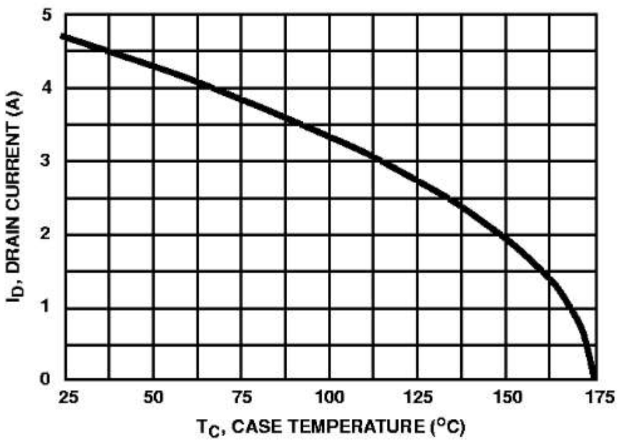


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

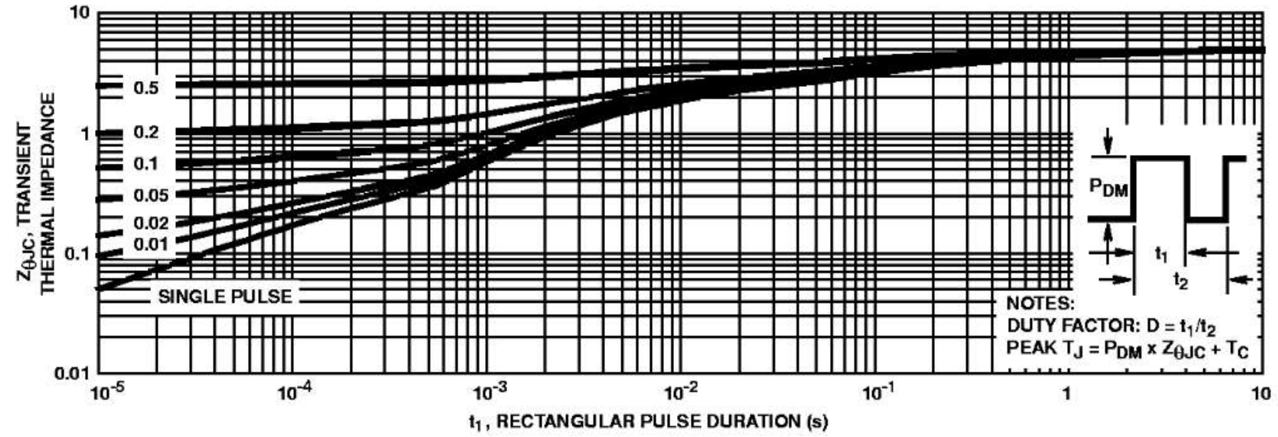


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

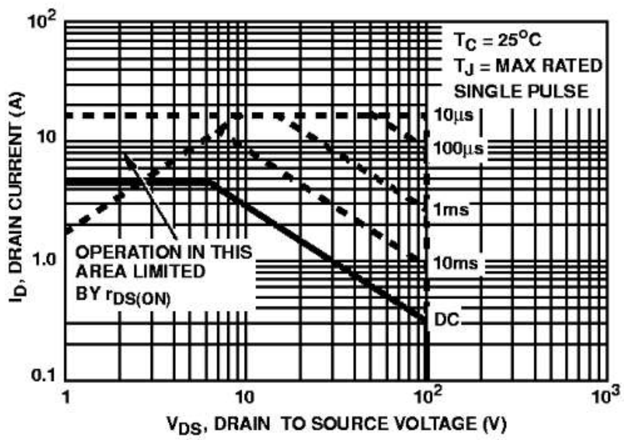


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

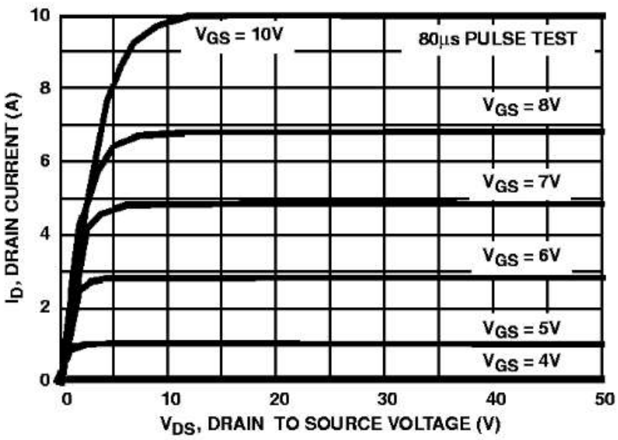


FIGURE 5. OUTPUT CHARACTERISTICS

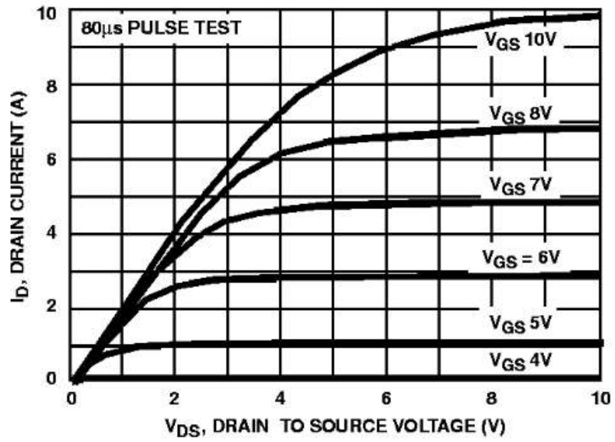


FIGURE 6. SATURATION CHARACTERISTICS

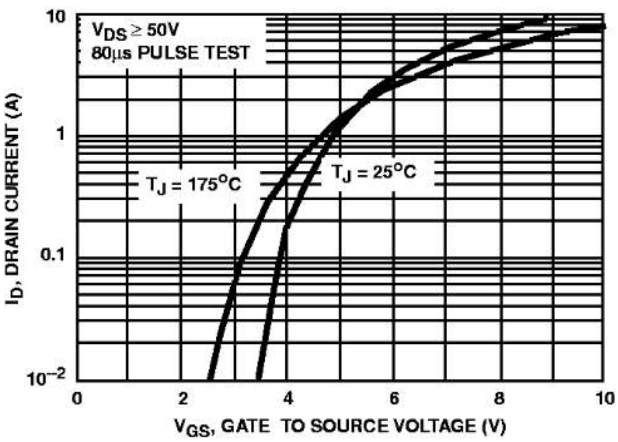


FIGURE 7. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

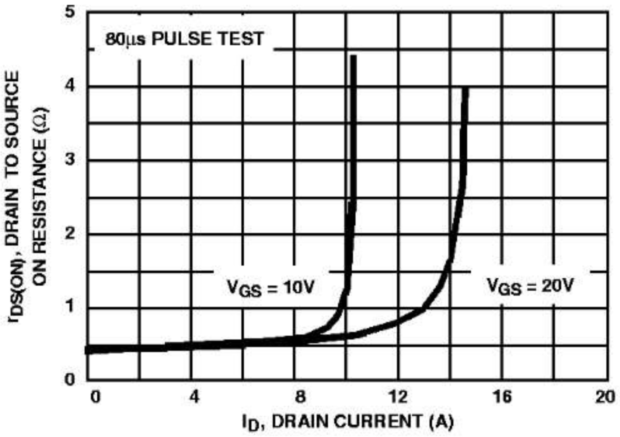


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

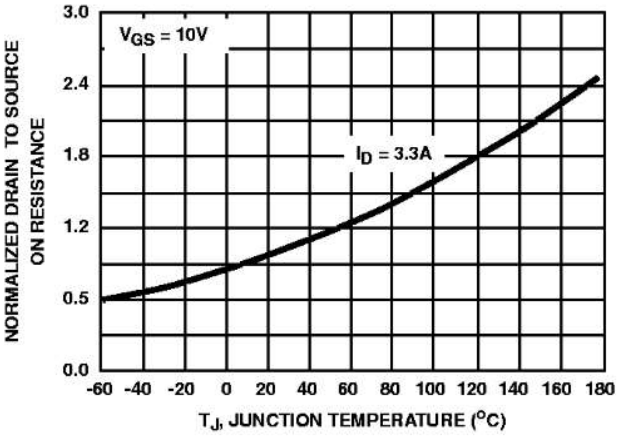


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

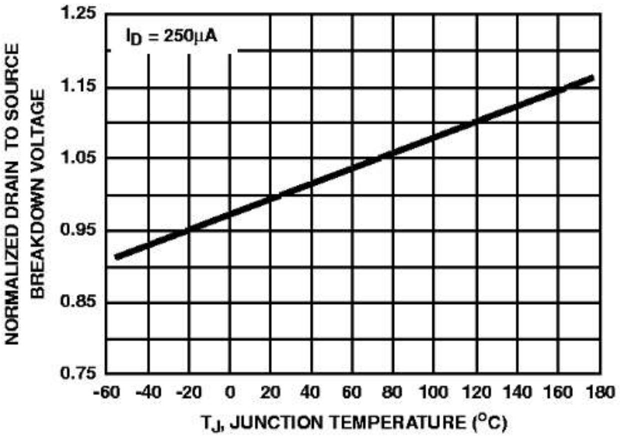


FIGURE 10. DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

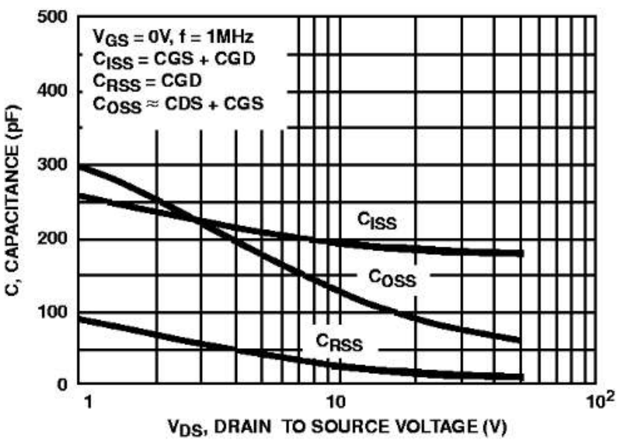


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

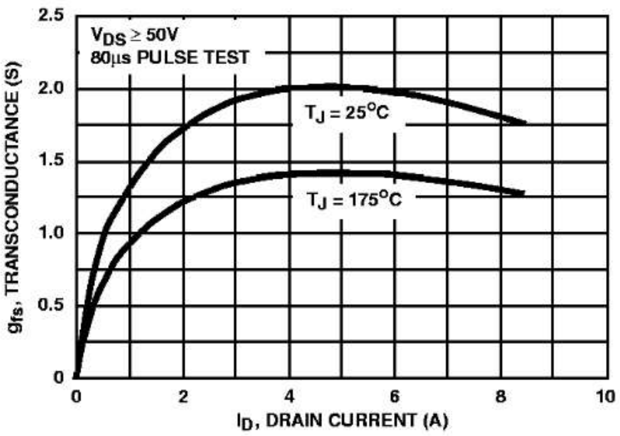


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

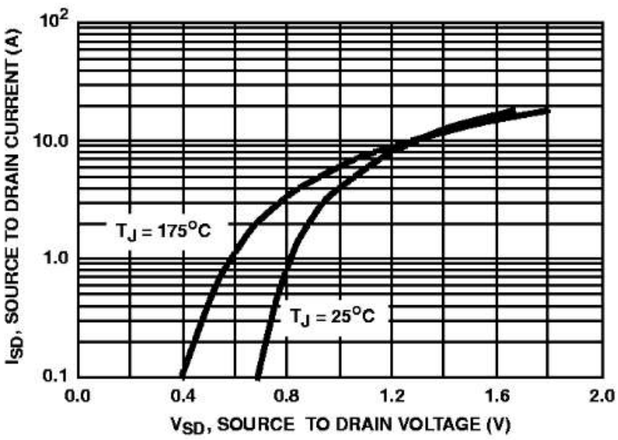


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

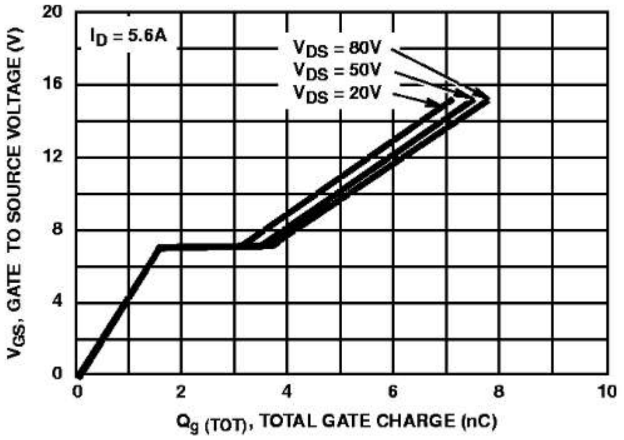


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

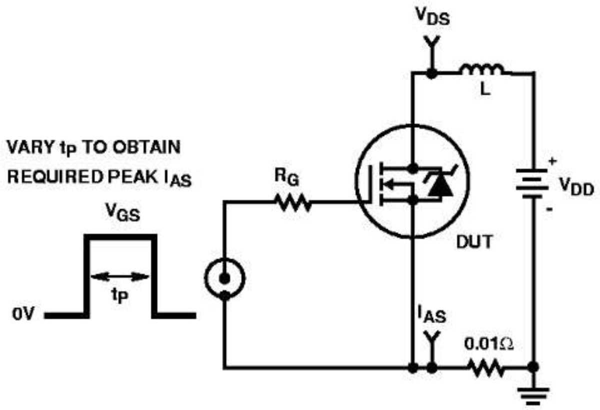


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

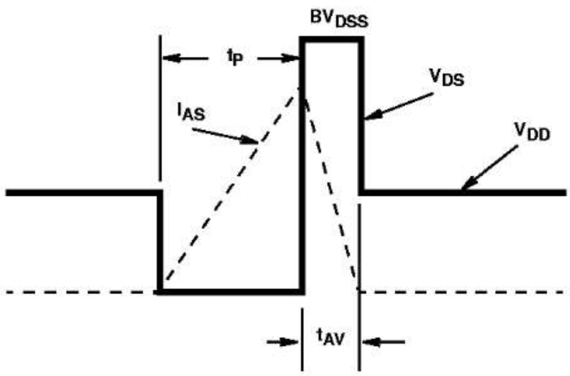


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

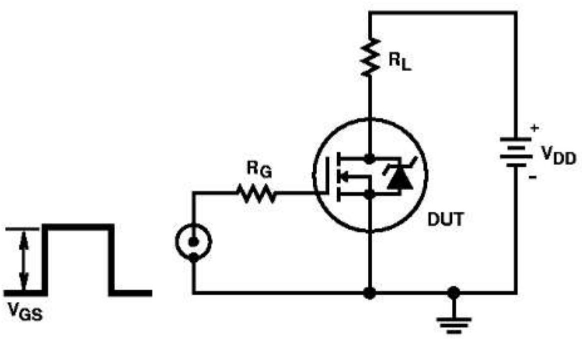


FIGURE 17. SWITCHING TIME TEST CIRCUIT

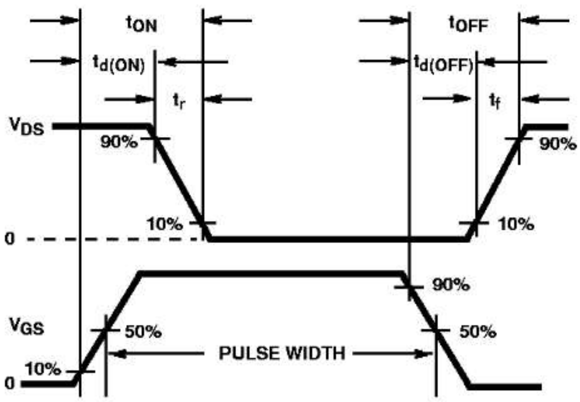


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

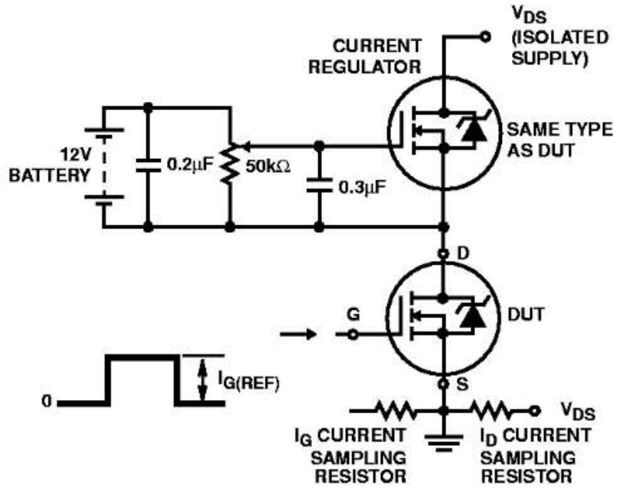


FIGURE 19. GATE CHARGE TEST CIRCUIT

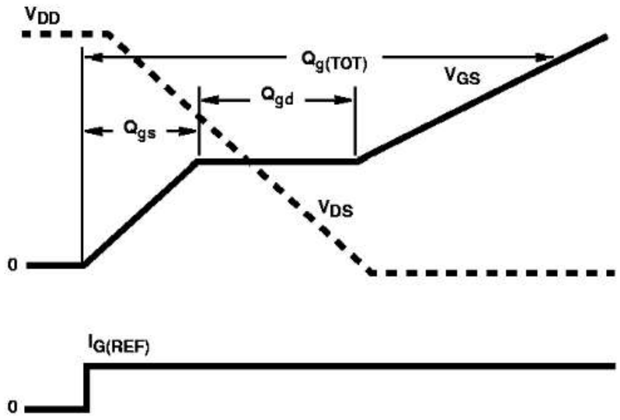


FIGURE 20. GATE CHARGE WAVEFORMS