

# 74ABT16373

## 16-Bit Transparent D-Type Latch with 3-STATE Outputs

### General Description

The ABT16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

### Features

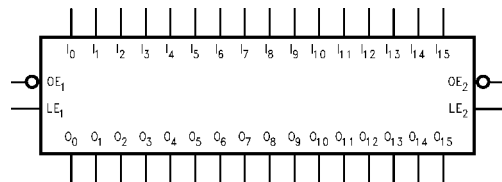
- Separate control logic for each byte
- 16-bit version of the ABT373
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection

### Ordering Code:

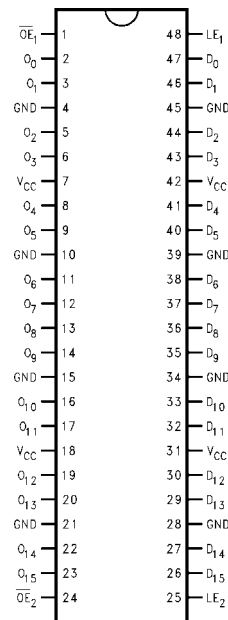
| Order Number   | Package Number | Package Description   |
|----------------|----------------|---|
| 74ABT16373CSSC | MS48A          | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide      |
| 74ABT16373CMTD | MTD48          | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

| Pin Names         | Description                      |
|-------------------|----------------------------------|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $LE_n$            | Latch Enable Input               |
| $D_0$ - $D_{15}$  | Data Inputs                      |
| $O_0$ - $O_{15}$  | Outputs                          |

74ABT16373 16-Bit Transparent D-Type Latch with 3-STATE Outputs

### Functional Description

The ABT16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The 3-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

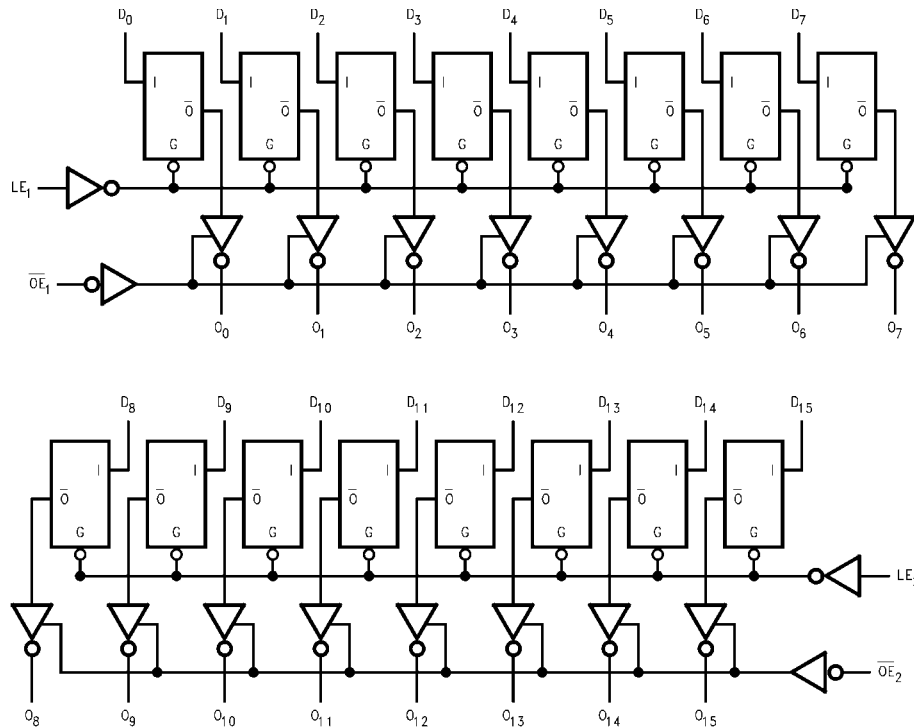
### Truth Tables

| Inputs |                   |           | Outputs    |
|--------|-------------------|-----------|------------|
| $LE_1$ | $\overline{OE}_1$ | $D_0-D_7$ | $O_0-O_7$  |
| X      | H                 | X         | Z          |
| H      | L                 | L         | L          |
| H      | L                 | H         | H          |
| L      | L                 | X         | (Previous) |

| Inputs |                   |              | Outputs      |
|--------|-------------------|--------------|--------------|
| $LE_2$ | $\overline{OE}_2$ | $D_8-D_{15}$ | $O_8-O_{15}$ |
| X      | H                 | X            | Z            |
| H      | L                 | L            | L            |
| H      | L                 | H            | H            |
| L      | L                 | X            | (Previous)   |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 Previous = previous output prior to HIGH-to-LOW transition of LE

### Logic Diagrams



**Absolute Maximum Ratings**(Note 1)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin  | -0.5V to +7.0V                       |
| Input Voltage (Note 2)   | -0.5V to +7.0V                       |
| Input Current (Note 2)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Any Output<br>in the Disabled or<br>Power-Off State                 | -0.5V to +5.5V                       |
| in the HIGH State  | -0.5V to V <sub>CC</sub>             |
| Current Applied to Output<br>in LOW State (Max)  | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current: $\overline{\text{OE}}$ Pin<br>(Across Comm Operating Range) | -350 mA                              |
| Other Pins   | -500 mA                              |
| Over Voltage Latchup (I/O)   | 10V                                  |

**Recommended Operating Conditions**

|   |                |
|---|----------------|
| Free Air Ambient Temperature                    | -40°C to +85°C |
| Supply Voltage                                  | +4.5V to +5.5V |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| Data Input                                      | 50 mV/ns       |
| Enable Input                                    | 20 mV/ns       |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                           | Min  | Typ     | Max  | Units      | V <sub>CC</sub> | Conditions  |
|------------------|-------------------------------------|------|---------|------|------------|-----------------|---|
| V <sub>IH</sub>  | Input HIGH Voltage                  | 2.0  |         |      | V          |                 | Recognized HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                   |      |         | 0.8  | V          |                 | Recognized LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage           |      |         | -1.2 | V          | Min             | I <sub>IN</sub> = -18 mA  |
| V <sub>OH</sub>  | Output HIGH Voltage                 | 2.5  |         |      |            | Min             | I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -32 mA   |
| V <sub>OL</sub>  | Output LOW Voltage                  |      |         | 0.55 | V          | Min             | I <sub>OL</sub> = 64 mA   |
| I <sub>IH</sub>  | Input HIGH Current                  |      | 1       | 1    | μA         | Max             | V <sub>IN</sub> = 2.7V (Note 3)<br>V <sub>IN</sub> = V <sub>CC</sub>  |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test   |      |         | 7    | μA         | Max             | V <sub>IN</sub> = 7.0V  |
| I <sub>IL</sub>  | Input LOW Current                   |      |         | -1   | μA         | Max             | V <sub>IN</sub> = 0.5V (Note 3)<br>V <sub>IN</sub> = 0.0V   |
| V <sub>ID</sub>  | Input Leakage Test                  | 4.75 |         |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded   |
| I <sub>OZH</sub> | Output Leakage Current              |      |         | 10   | μA         | 0 - 5.5V        | V <sub>OUT</sub> = 2.7V; $\overline{\text{OE}}$ = 2.0V  |
| I <sub>OZL</sub> | Output Leakage Current              |      |         | -10  | μA         | 0 - 5.5V        | V <sub>OUT</sub> = 0.5V; $\overline{\text{OE}}$ = 2.0V  |
| I <sub>OS</sub>  | Output Short-Circuit Current        | -100 |         | -275 | mA         | Max             | V <sub>OUT</sub> = 0.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current         |      |         | 50   | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub>  |
| I <sub>ZZ</sub>  | Bus Drainage Test                   |      |         | 100  | μA         | 0.0             | V <sub>OUT</sub> = 5.5V; All Others GND   |
| I <sub>CCH</sub> | Power Supply Current                |      |         | 2.0  | mA         | Max             | All Outputs HIGH  |
| I <sub>CCL</sub> | Power Supply Current                |      |         | 62   | mA         | Max             | All Outputs LOW   |
| I <sub>CCZ</sub> | Power Supply Current                |      |         | 2.0  | mA         | Max             | $\overline{\text{OE}}$ = V <sub>CC</sub><br>All Others at V <sub>CC</sub> or GND  |
| I <sub>CCT</sub> | Additional I <sub>CC</sub> /Input   |      |         | 2.5  | mA         | Max             | V <sub>I</sub> = V <sub>CC</sub> - 2.1V<br>Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V<br>Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V<br>All Others at V <sub>CC</sub> or GND |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub><br>(Note 3) |      | No Load |      | mA/<br>MHz | Max             | Outputs Open, LE = V <sub>CC</sub><br>$\overline{\text{OE}}$ = GND, (Note 4)<br>One Bit Toggling, 50% Duty Cycle  |

**Note 3:** Guaranteed, but not tested.

**Note 4:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

## AC Electrical Characteristics

(SOIC and SSOP Packages)

| Symbol           | Parameter                        | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50 pF |     | Units |
|------------------|----------------------------------|---|-----|-----|---|-----|-------|
|                  |                                  | Min   | Typ | Max | Min   | Max |       |
| t <sub>PLH</sub> | Propagation Delay                | 1.4   |     | 5.6 | 1.4   | 5.6 | ns    |
| t <sub>PHL</sub> | D <sub>n</sub> to O <sub>n</sub> | 1.4   |     | 5.6 | 1.4   | 5.6 |       |
| t <sub>PLH</sub> | Propagation Delay                | 1.7   |     | 6.0 | 1.7   | 6.0 | ns    |
| t <sub>PHL</sub> | LE to O <sub>n</sub>             | 1.7   |     | 5.5 | 1.7   | 5.5 |       |
| t <sub>PZH</sub> | Output Enable Time               | 1.1   |     | 6.1 | 1.1   | 6.1 | ns    |
| t <sub>PZL</sub> |                                  | 1.5   |     | 5.6 | 1.5   | 5.6 |       |
| t <sub>PHZ</sub> | Output Disable Time              | 2.4   |     | 7.1 | 2.4   | 7.1 | ns    |
| t <sub>PLZ</sub> |                                  | 1.6   |     | 6.5 | 1.6   | 6.5 |       |

## AC Operating Requirements

(SOIC and SSOP Packages)

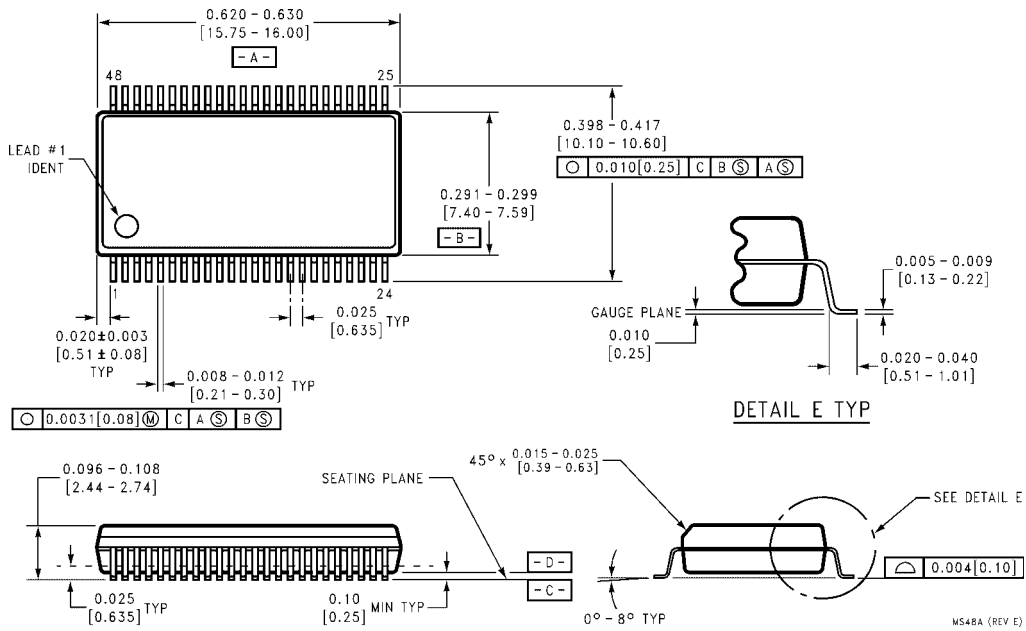
| Symbol              | Parameter                   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50 pF |     | Units |
|---------------------|-----------------------------|---|-----|-----|---|-----|-------|
|                     |                             | Min   | Typ | Max | Min   | Max |       |
| f <sub>TOGGLE</sub> | Maximum Toggle Frequency    |   | 100 |     |   |     | MHz   |
| t <sub>S(H)</sub>   | Setup Time, HIGH            | 1.5   |     |     | 1.5   |     | ns    |
| t <sub>S(L)</sub>   | or LOW D <sub>n</sub> to LE | 1.5   |     |     | 1.5   |     |       |
| t <sub>H(H)</sub>   | Hold Time, HIGH             | 1.0   |     |     | 1.0   |     | ns    |
| t <sub>H(L)</sub>   | or LOW D <sub>n</sub> to LE | 1.0   |     |     | 1.0   |     |       |
| t <sub>W(H)</sub>   | Pulse Width,<br>LE HIGH     | 3.0   |     |     | 3.0   |     | ns    |

## Capacitance

| Symbol                    | Parameter          | Typ | Units | Conditions<br>(T <sub>A</sub> = 25°C) |
|---------------------------|--------------------|-----|-------|---------------------------------------|
| C <sub>IN</sub>           | Input Capacitance  | 5   | pF    | V <sub>CC</sub> = 0V                  |
| C <sub>OUT</sub> (Note 5) | Output Capacitance | 11  | pF    | V <sub>CC</sub> = 5.0V                |

**Note 5:** C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

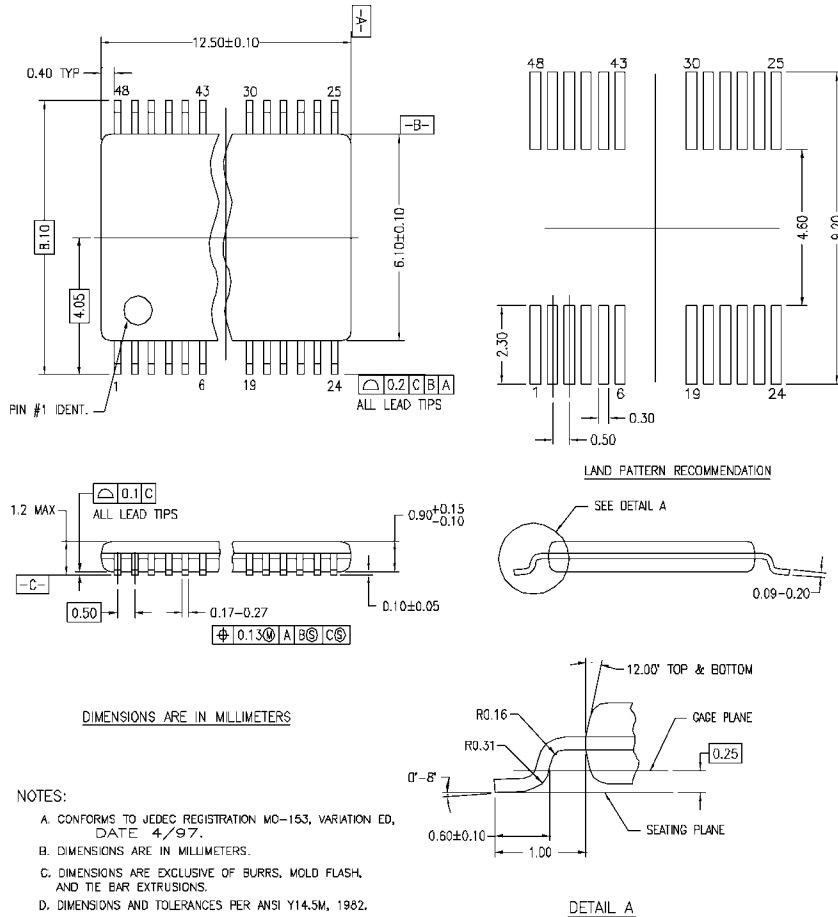
**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

MS48A (REV E)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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