JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

12V Input Single Channel Full Bridge Motor Driver

CJDR9110T Motor Driver

1 Introduction

CJDR9110T is a 12V DC motor driver. The device is internally integrated with a full bridge composed of four MOS, which can support a power supply voltage range of 3.8V to 12V, and can provide a continuous output current of up to 1.5A or a peak output current of 2.5A. CJDR9110T has an input interface IN / IN compatible with industry standard devices, which can support pulse width modulation (PWM) mode control. When the input interfaces are all low level, the device will enter sleep mode, and the power consumption current in sleep mode is less than 1μA. Since the device has built-in LDO, it can be compatible with common input voltage (such as 3.3V or 5.0V) without logic power supply.

CJDR9110T is an upgraded version of CJDR9110, with functions such as thermal shutdown, undervoltage protection, short circuit protection, overcurrent protection, automatic fault recovery, etc. One CJDR9110T can be used to drive a DC motor or two CJDR9110Ts can be used to drive a stepping motor. Therefore, CJDR9110T is very suitable for applications, providing an integrated motor drive solution for consumer products such as cameras, toys, or other battery powered motion control applications.

2 Applications

- Video Camera
- Digital Single Lens Reflective (DSLR)
- Lens
- Toys
- Robotics
- Shared Bicycle Lock
- Water Meter Switch
- Medical Equipment

3 Features

- Power supply input voltage: 3.8V~12V
- Output current:
  - 1.5A for continuous operation
  - 2.5A for peak current
- Low $R_{DS\ ON}$: 350mΩ (HS + LS)
- Pulse width modulation (PWM) input, compatible with common logic input levels of 3.3V and 5.0V
- Sleep mode low current consumption: nA level
- Comprehensive protection:
  - Thermal shutdown
  - Undervoltage protection
  - Built-in current limit
  - Short circuit protection
  - Automatic fault recovery

4 Available Package

PART NUMBER	PACKAGE
CJDR9110T	ESOP8

Note: For more detailed packaging information, see the part *Pin Configuration and Function* and the part *Mechanical Information*.

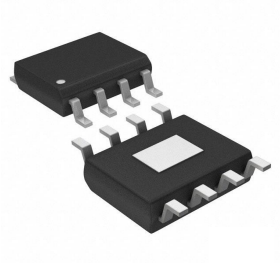


Figure 4-1. ESP8 Package

5 Pin Configuration and Function

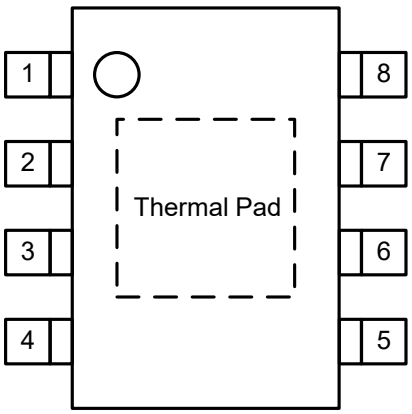


Figure 5-1. Package Top View

PIN NAME	CJDR9110T ESOP8	I / O	DESCRIPTION
VM	2 & 3	Power	Logic power supply.
OUT 1	1	O	H-bridge output 1.
OUT 2	4	O	H-bridge output 2.
GND	5 & 8	-	Device ground. Connect to system ground.
IN 2	6	I	H-bridge control input 2.
IN 1	7	I	H-bridge control input 1.
-	Thermal Pad	-	Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

(over operating free-air temperature range, unless otherwise specified)(1)

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Power supply input voltage range(2)	V_M	0 ~ 17	V
Logic input voltage range(2)	$V_{IN\ x}$	-0.5 ~ 7.0	
Continuous output current	I_{OUT}	±1.5	A
Peak output current	$I_{OUT\ Max}$	±2.5	
Maximum junction temperature	T_J	150	°C
Storage temperature	T_{stg}	-60 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 Recommended Operating Conditions

PARAMETER(3)	SYMBOL	MIN.	NOM.	MAX.	UNIT
Load power input voltage range	V_M	3.8	-	12	V
Logic input voltage (IN x)	$V_{IN\ x}$	0	-	5.0	V
Continuous output current	I_{OUT}	0	-	1.5	A
PWM frequency	f_{PWM}	0	-	250	kHz
Operating junction temperature	T_J	-40	-	150	°C
Operating ambient temperature	T_A	-40	-	100(4)	°C

(3) JSCJ recommends that users should not exceed the rated value in the *Recommended Operating Conditions* for the application conditions of the device, so as to ensure the stability of normal operation and reliability of long-term operation. Operation beyond the recommended rated conditions does not mean that the product will fail. The consumers need to evaluate the risks that may be caused by the operation of the product beyond the recommended rated conditions.
(4) It is necessary to ensure that the operating junction temperature of the device does not exceed the rated value of the recommended operating conditions when using the device for design.

6 Specifications

6.3 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge(5)	Human body model	$V_{ESD-HBM}$	4000	V

(5) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body mode (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ.

6.4 Thermal Information

THERMAL METRIC(6)	SYMBOL	CJDR9110T	UNIT
		ESOP8	
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	104.0	°C/W
Maximum heat dissipation power for continuous operation	$P_{D\ Ref}$	1.20	W

(6) T_A = 25°C, all numbers are typical, and apply for packages soldered directly onto a PCB board in still air.

6 Specifications

6.5 Electrical Characteristics

CJDR9110T (V_{CC} = 5.0V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(7)	MAX.	UNIT
Power Supply						
V_M working current	I_{VM}	No PWM input	-	0.8	1.2	mA
V_M standby current	$I_{VM\ Q}$	nSleep = 0	-	0.01	1	μA
Output H-bridge						
High side + low side bridge conduction resistance	$R_{DS\ ON}$	I_{OUT} = 500mA, T_J = 25°C	-	350	450	mΩ
		I_{OUT} = 500mA, T_J = 125°C	-	530	700	
Off-state leakage current	I_{OFF}	V_{OUT} = 0V	-10	-	10	μA
Logic Input Pin (IN 1, IN 2, nSleep)						
Logic input low voltage	V_{IL}	High level to low level	-	-	1.20	V
Logic input high voltage	V_{IH}	Low level to high level	1.60	-	-	V
Logic input hysteresis	V_{IHY}	V_{IN} = 3.3V	-	0.3	-	V
Logic input low current	I_{IL}	V_{IN} = 0V	-5	-	5	μA
Logic input high current	I_{IH}	V_{IN} = 3.3V	-	50	70	μA
Pull down resistance	R_{PD}	IN x pins and nSleep pin	-	100	-	kΩ
Protection Circuits						
Thermal shutdown temperature	T_{SD}	-	155	170	180	°C
Thermal shutdown hysteresis	ΔT_{SD}	-	-	20	-	°C
Undervoltage protection voltage	V_{UVLO}	V_{CC} power supply	-	3.00	-	V
Undervoltage protection hysteresis	ΔV_{UVLO}	V_{CC} power supply	-	0.20	-	V
Output current limit	$I_{OUT\ Limit}$	High side	-	3.0	-	A
		Low side	-	3.0	-	
OCP delay time	t_D	-	-	2.3	-	μs
OCP retry time	t_R	-	-	1.5		ms

Note:

(7) Typical numbers are at 25°C and represent the most likely norm.

6 Specifications

6.6 Time Series Parameters

CJDR9110T (V_{CC} = 5.0V, T_A = 25°C, R_L = 20Ω, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(7)	MAX.	UNIT
Start-up time	T1	-	-	-	10	μs
Shutdown time	T2	-	-	180	220	ns
Input high to output high delay	T3	-	-	160	200	ns
Input low to output low delay	T4	-	-	160	200	ns
Output rising edge time	T5	-	-	40	200	ns
Output drop edge time	T6	-	-	2	3	ms

Note:

(7) Typical numbers are at 25°C and represent the most likely norm.

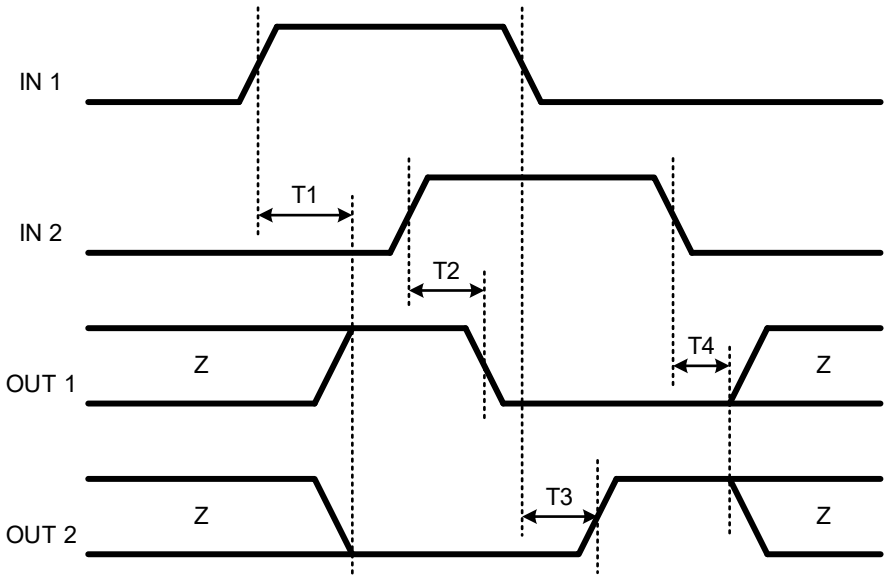


Figure 6-1. Input and Output Time Parameter 1

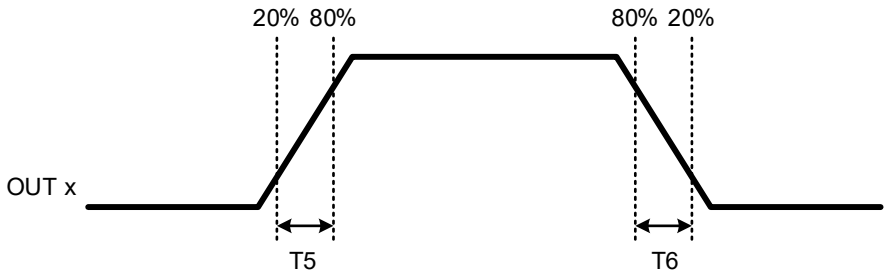


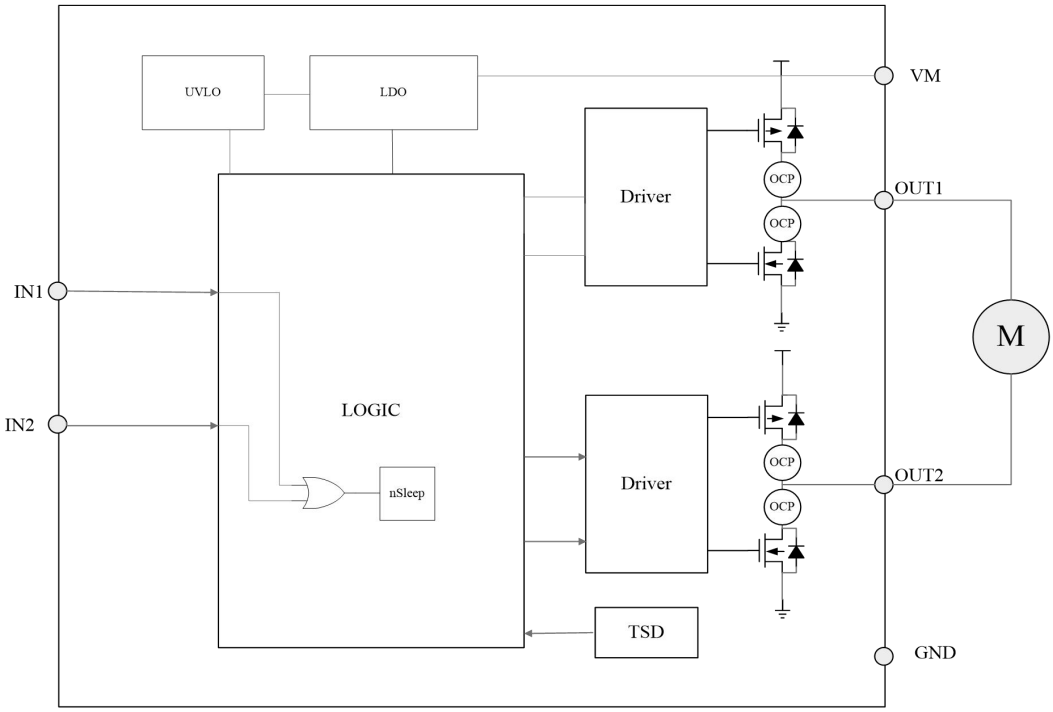
Figure 6-2. Input and Output Time Parameter 2

7 Detailed Description

7.1 Description

CJDR9110T is a 12V, single channel, full bridge motor drive integrated circuit. It supports 12V power input supply voltage and can provide up to 1.5A continuous output current. CJDR9110T has a PWM (IN / IN) input interface and is compatible with industry standard devices.

7.2 Functional Block Diagram



7 Detailed Description

7.3 Feature Description

PWM Control Mode

CJDR9110T is controlled by PWM input interface, also known as IN / IN input mode, the PWM interface (IN 1 / IN 2) controls the OUT x pins according to the logic table in Table 7-1.

Table 7-1. PWM Control Mode with Automatic Sleep

IN 1	IN 2	OUT 1	OUT 2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Coast (H-bridge Hi-Z) / low-power automatic sleep mode
0	1	L	H	Reverse (OUT 2 → OUT 1)
1	0	H	L	Forward (OUT 1 → OUT 2)
1	1	L	L	Brake (low-side slow decay)

Sleep Mode

When IN 1 and IN 2 are at low level, the device will enter sleep mode. At this time, the internal circuit of the device will stop working, and the current power consumption will be less than 1μA.
When one of IN 1 and IN 2 is at high level and the other is at low level, the device will resume normal operation.
The recovery time from sleep mode to normal operation shall not exceed 10μs.
If the control logic of IN 1= IN 2= 0 needs to be used when using the control mode of pulse width modulation for adjustment, ensure that keep the input low level within the range of 0.9V ~ 1.2V.

Input Pin

IN 1 and IN 2 input pins have 100kΩ resistance pull-down, and the default is low level.

Thermal Shutdown

When the junction temperature T_J exceeds 170°C (Typ.), the thermal shutdown circuit is activated and all outputs of the device will be turned off. When the T_J decreases by a hysteresis temperature of 20°C (Typ.), the device will return to normal operation.
Although the internal protection circuit of the device is designed to prevent overall thermal conditions, it is not intended to replace appropriate power consumption. Continuous operation of the equipment until thermal shutdown or higher than the recommended T_J will reduce long-term reliability.

Undervoltage Locking

When the power supply voltage is lower than V_{UVLO}, the device will enter the undervoltage protection mode, and the internal detection circuit will turn off the H-bridge output. At this time, if the power supply voltage rises within a certain range of ΔV_{UVLO}, the device will release the undervoltage protection mode and resume normal operation.

7 Detailed Description

7.3 Feature Description (continued)

Built-in Current Limit

Each drive MOS of the H-bridge in CJDR9110T has a built-in current limiting mechanism. When it is detected that the current of any drive MOS exceeds the output current limit $I_{OUT\ Limit}$ in the data sheet and the duration exceeds the delay time T_D, all drive MOS will be turned off. After the retry time T_R, the drive tube will automatically attempt to resume normal operation. At this time, if the output current still exceeds the rated range, the device will enter the current limit state again and turn off the output. Therefore, when the device enters the output current limit state because the output current exceeds the rated range, the device will continue the process of "Detection - Shutdown - Release - Detection" until the output current no longer exceeds its rated range. Typical values of output current limit $I_{OUT\ Limit}$, delay time T_D and retry time T_R can be found in *Electrical Characteristics*.

Short Circuit Protection

CJDR9110T has short circuit protection mechanism. When OUT x is short circuited to GND (for example, when the high side of OUT 1 is conductive, OUT 1 is abnormally short circuited to GND), or when OUT x is short circuited to VM (for example, when the lower side of OUT 1 is conductive, OUT 1 is abnormally short circuited to VM), the device will turn off the output of all drive MOS to protect the device from being burnt due to large current. The action mechanism of short-circuit protection is the same as that of current limit. See *Build-in Current Limit* for more details.

Operation Mode

CJDR9110T enters the sleep mode when both IN 1 and IN 2 are low. In the sleep mode, all h-bridges are turned off and output high resistance state. Most circuits of chip circuits are turned off and enter the power saving mode.
When IN 1 and IN 2 are not low at the same time, they will automatically resume normal operation.
When the over temperature protection detects failure, it will also close the H-bridge.

Table 7-2. Operation Mode

MODE	CONDITION	H-BRIDGE
Work	0 when IN 1 is different from IN 2	Normal Operation
Sleep mode	IN 1 = IN 2 = 0	Shutdown
Failure detection	IN x = X	Shutdown

8 Application and Implementation

8.1 Typical Application Circuit

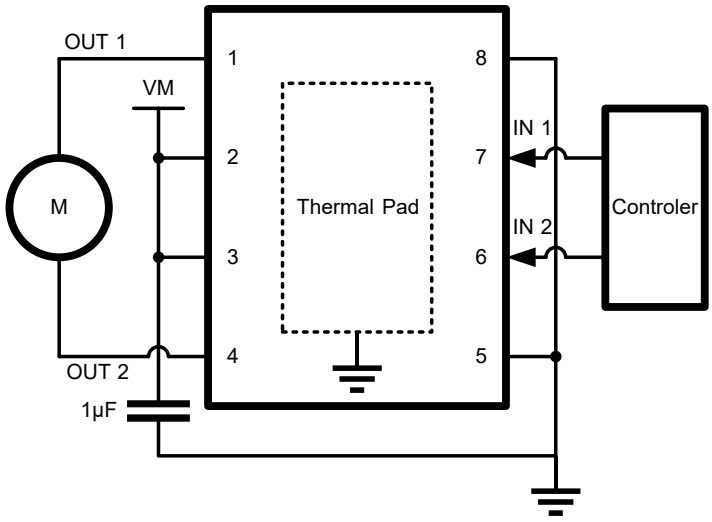


Figure 8-1. Typical Application Circuit

8.2 Application Information

The absolute parameters of the device cannot be exceeded in any environment.

The bypass capacitor of V_{CC}, especially the connection of ceramic capacitor, should be as close to the V_{CC} pin of the device as possible.

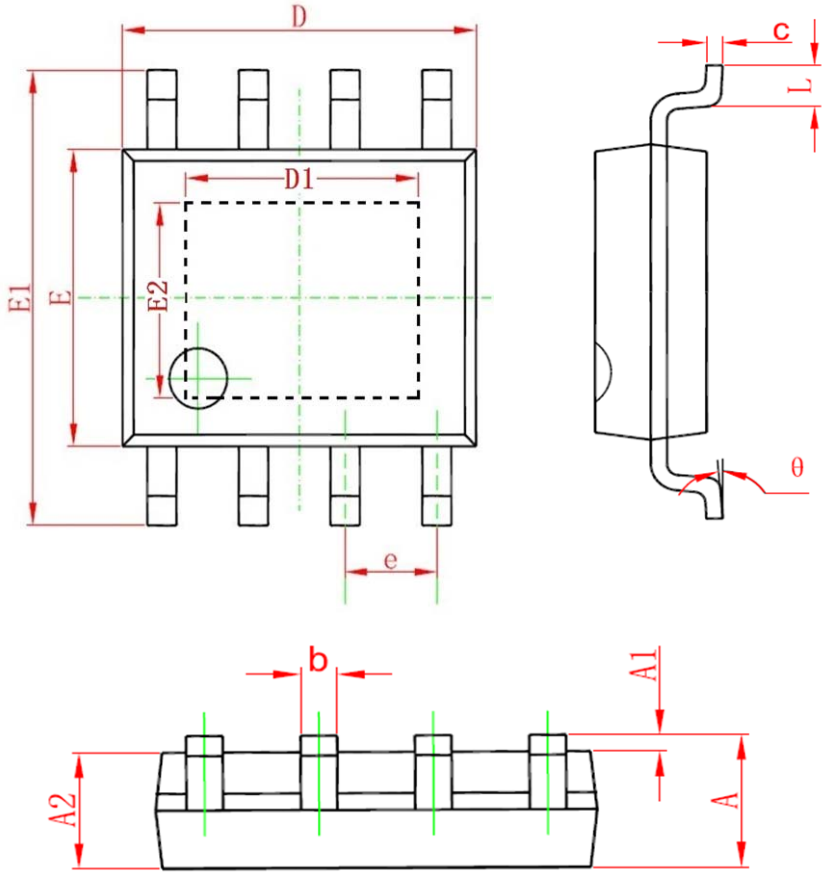
The ground wire connecting the motor needs to be isolated in layout design.

NOTE

The application information in this section is not part of the data sheet component specification, and JSCJ makes no commitment or statement to guarantee its accuracy or completeness. Customers are responsible for determining the rationality of corresponding components in their circuit design and making tests and verifications to ensure the normal realization of their circuit design.

9 Mechanical Information

ESOP8 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0. 250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- https: ***www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

August, 2022: released CJDR9110T rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

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