

AMIS-30600

LIN Transceiver

General Description

The single-wire transceiver AMIS-30600 is a monolithic integrated circuit in a SOIC-8 package. It works as an interface between the protocol controller and the physical bus.

The AMIS-30600 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the AMIS-30600 offers a stand-by mode. A wake-up caused by a message on the bus pulls the INH-output high until the device is switched to normal operation mode.

The transceiver is implemented in I2T100 technology enabling both high-voltage analog circuitry and digital functionality to co-exist on the same chip.

The AMIS-30600 provides an ultra-safe solution to today's automotive in-vehicle networking (IVN) requirements by providing unlimited short circuit protection in the event of a fault condition.

Features

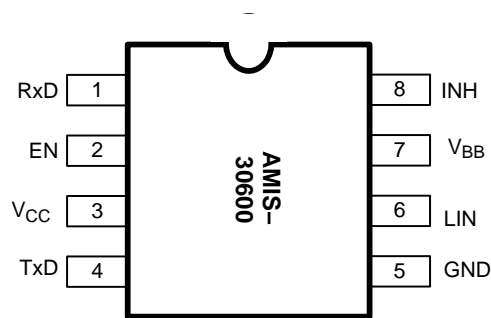
- LIN-Bus Transceiver
 - ♦ LIN compliant to specification rev. 1.3 and rev. 2.0
 - ♦ I2T high-voltage technology
 - ♦ Bus voltage ± 40 V
 - ♦ Transmission rate up to 20kbaud
 - ♦ SOIC-150-8 package
- Protection
 - ♦ Thermal shutdown
 - ♦ Indefinite short circuit protection to supply and ground
- Load dump protection (45 V)
- Power Saving
 - ♦ Operating voltage = 4.75 to 5.25 V
 - ♦ Power down supply current < 50 μ A
- EMS Compatibility
 - ♦ Integrated filter and hysteresis for receiver
- EMI Compatibility
 - ♦ Integrated slope control for transmitter
 - ♦ Slope control dependant from Vbat to enable maximum capacitive load
- These are Pb-Free Devices



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PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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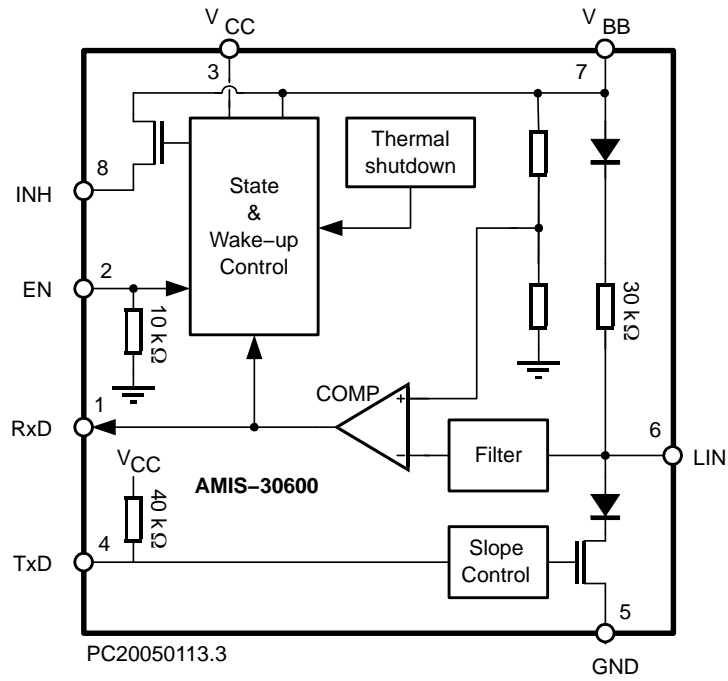


Figure 1. Block Diagram

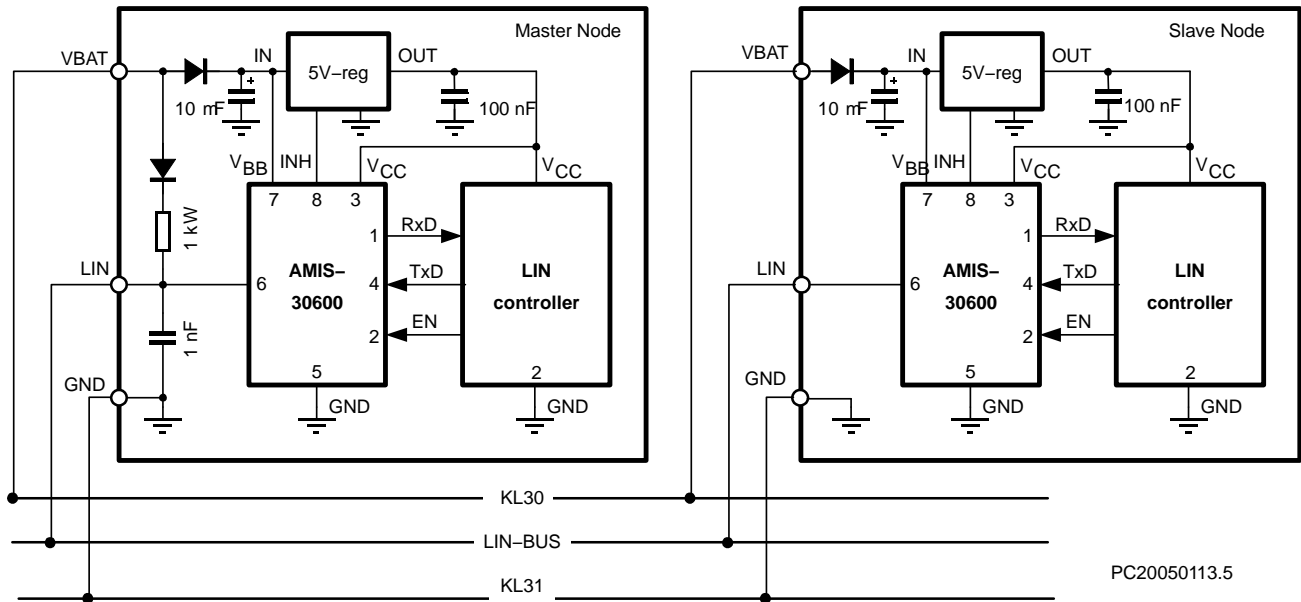


Figure 2. Application Diagram

Table 1. PIN LIST AND DESCRIPTIONS

| Pin | Name | Description |
|-----|------|--|
| 1 | RxD | Receive data output; low in dominant state |
| 2 | EN | Enable input; transceiver in normal operation mode when high |
| 3 | VCC | 5V supply input |
| 4 | TxD | Transmit data input; low in dominant state; internal 40 kΩ pullup |
| 5 | GND | Ground |
| 6 | LIN | LIN bus output/input; low in dominant state; internal 30 kΩ pullup |
| 7 | VBB | Battery supply input |
| 8 | INH | Inhibit output; to control a voltage regulator; becomes high when wake-up via LIN bus occurs |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|---|------------------------------|------|-----------------------|------|
| V _{CC} | Supply Voltage | | -0.3 | +7 | V |
| V _{BB} | Battery Supply Voltage | | -0.3 | +40 | V |
| V _{LIN} | DC Voltage at Pin LIN | 0 < V _{CC} < 5.50 V | -40 | +40 | V |
| V _{INH} | DC Voltage at Pin INH | 0 < V _{CC} < 5.50 V | -0.3 | V _{BB} + 0.3 | V |
| V _{TxD} | DC Voltage at Pin TxD | 0 < V _{CC} < 5.50 V | -0.3 | V _{CC} + 0.3 | V |
| V _{RxD} | DC Voltage at Pin RxD | 0 < V _{CC} < 5.50 V | -0.3 | V _{CC} + 0.3 | V |
| V _{EN} | DC Voltage at Pin EN | 0 < V _{CC} < 5.50 V | -0.3 | V _{CC} + 0.3 | V |
| V _{esd(LIN)} | Electrostatic Discharge Voltage at LIN Pin | (Note 1) | -4 | +4 | kV |
| V _{esd} | Electrostatic Discharge Voltage at All Other Pins | (Note 1) | -4 | +4 | kV |
| V _{tran(LIN)} | Transient Voltage at Pin LIN | (Note 2) | -150 | +150 | V |
| V _{tran(VBB)} | Transient Voltage at Pin V _{BB} | (Note 3) | -150 | +150 | V |
| T _{amb} | Ambient Temperature | | -40 | +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Standardized Human Body Model system ESD pulses in accordance with IEC 1000.4.2.
2. Applied transient waveforms in accordance with "ISO 7637 parts 1 & 3", capacitive coupled test pulses 1 (-100 V), 2 (+100 V), 3a (-150 V), and 3b (+150 V). See Figure 8.
3. Applied transient waveforms in accordance with "ISO 7637 parts 1 & 3", direct coupled test pulses 1 (-100 V), 2 (+75 V), 3a (-150 V), 3b (+150 V), and 5 (+80 V). See Figure 8.

Table 3. OPERATING RANGE

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|--|------|------|-------|------|
| V _{CC} | Supply Voltage | 4.75 | | +5.25 | V |
| V _{BB} | Battery Supply Voltage | 7.3 | | +18 | V |
| T _J | Maximum Junction Temperature | -40 | | +150 | °C |
| T _{jsd} | Thermal Shutdown Temperature | +150 | +170 | +190 | °C |
| R _{thj-a} | Thermal Resistance Junction-to-Ambient | | 185 | | °C/W |

APPLICATION INFORMATION

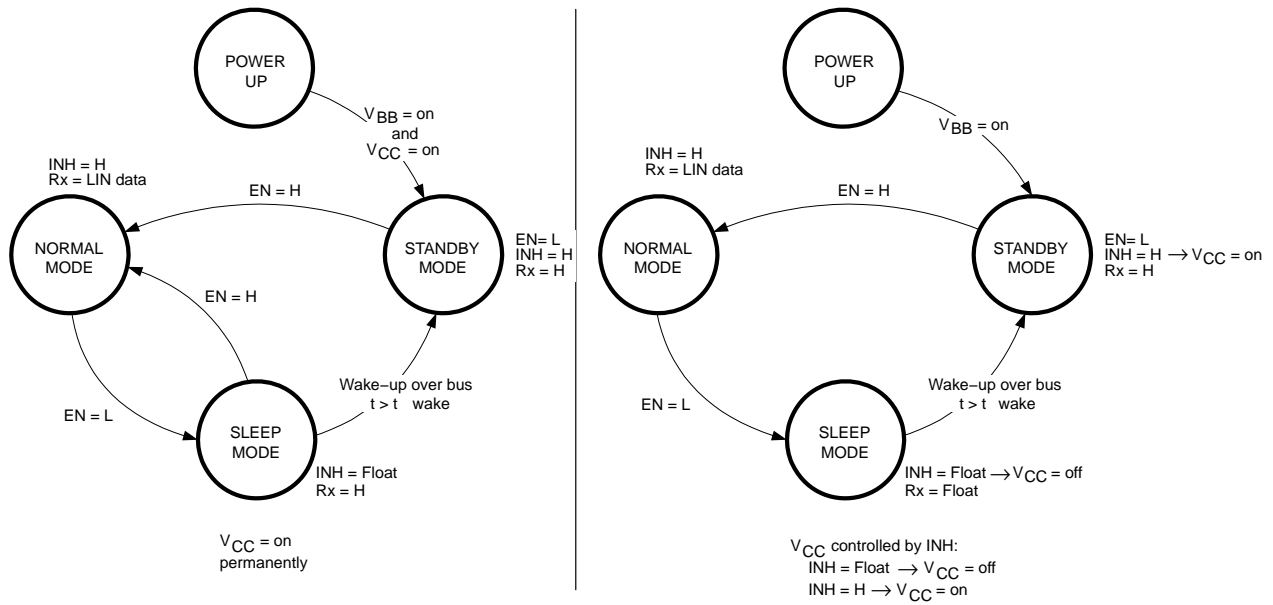


Figure 3. State Diagrams

The AMIS-30600 has a slope which depends of the supply V_{bat} . This implementation guarantees biggest slope-time under all load conditions. The rising slope has to be slower then the external RC-time-constant, otherwise the slope will be terminated by the RC-time-constant and no longer by the internal slope-control. This would affect the symmetry of the bus-signal and would limit the maximum allowed bus-speed.

A capacitor of 10 μF at the supply voltage input VB buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

In order to reduce the current consumption, the AMIS-30600 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see Figure 4).

An external voltage regulator can be controlled via the INH output in order to minimize the current consumption of the whole application in sleep mode (see Figure 2). A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INH output high (see Figure 3). In case the voltage regulator control input is not connected to the INH output, or the microcontroller is active respectively, the AMIS-30600 can be set in normal operation mode by EN = H (see Figure 3).

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Table 4. DC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $V_{BB} = 7.3 \text{ V to } 18 \text{ V}$, $V_{EN} < V_{ENon}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$; $R_L = 500 \Omega$ unless specified otherwise. All voltages with respect to ground, positive current flowing into pin, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|----------------------|----------------------|-----------------------|------------------------------|
| SUPPLY (Pin V_{CC} and Pin V_{BB}) | | | | | | |
| I_{CC} | 5 V Supply Current | Dominant; $V_{TxD} = 0 \text{ V}$ Recessive; $V_{TxD} = V_{CC}$ | | 400 250 | 700 500 | μA |
| I_{BB} | Battery Supply Current | Dominant; $V_{TxD} = 0 \text{ V}$ Recessive; $V_{TxD} = V_{CC}$ | | 1 100 | 1.5 200 | mA μA |
| I_{BB} | Battery Supply Current | Sleep Mode; $V_{EN} = 0 \text{ V}$ | | 35 | 55 | μA |
| I_{CC} | 5 V Supply Current | Sleep Mode; $V_{EN} = 0 \text{ V}$ | | 0.25 | 1 | μA |
| TRANSMITTER DATA INPUT (Pin TxD) | | | | | | |
| V_{IH} | High-Level Input Voltage | Output Recessive | $0.7 \times V_{CC}$ | – | V_{CC} | V |
| V_{IL} | Low-Level Input Voltage | Output Dominant | 0 | – | $0.3 \times V_{CC}$ | V |
| $R_{TxD,pu}$ | Pullup Resistor to V_{CC} | | 24 | | 60 | k |
| RECEIVER DATA OUTPUT (Pin RxD) | | | | | | |
| V_{OH} | High-Level Output Voltage | $I_{RxD} = -10 \text{ mA}$ | $0.8 \times V_{CC}$ | | V_{CC} | V |
| V_{OL} | Low-Level Output Voltage | $I_{RxD} = 5 \text{ mA}$ | 0 | | $0.2 \times V_{CC}$ | V |
| ENABLE INPUT (Pin EN) | | | | | | |
| $V_{EN,on}$ | High-Level Input Voltage | Normal Mode | $0.7 \times V_{CC}$ | – | V_{CC} | V |
| $V_{EN,off}$ | Low-Level Input Voltage | Low Power Mode | 0 | – | $0.3 \times V_{CC}$ | V |
| $R_{EN,pd}$ | Pulldown Resistor-to-GND | | 6 | 10 | 15 | k |
| INHIBIT OUTPUT (Pin INH) | | | | | | |
| $V_{INH,d}$ | High-Level Voltage Drop: $V_{INH,d} = V_{BB} - V_{INH}$ | $I_{INH} = -0.15 \text{ mA}$ | | 0.5 | 1.0 | V |
| $I_{INH,lk}$ | Leakage Current | Sleep Mode; $V_{INH} = 0 \text{ V}$ | -5.0 | – | 5.0 | μA |
| BUS LINE (Pin LIN) | | | | | | |
| $V_{bus,rec}$ | Recessive Bus Voltage at Pin LIN | $V_{TxD} = V_{CC}$ | $0.9 \times V_{BB}$ | – | V_{BB} | V |
| $V_{bus,dom}$ | Dominant Output Voltage at Pin LIN | $V_{TxD} = 0 \text{ V}$; $V_{BB} = 7.3 \text{ V}$ $V_{TxD} = 0 \text{ V}$; $V_{BB} = 18 \text{ V}$; $R_L = 500 \Omega$ | 0 | – | 1.2 2.0 | V |
| $I_{bus,sc}$ | Bus Short-Circuit Current | $V_{bus,short} = 18 \text{ V}$ | 40 | 85 | 130 | mA |
| $I_{bus,lk}$ | Bus Leakage Current | $V_{CC} = V_{BB} = 0 \text{ V}$; $V_{bus} = -8 \text{ V}$ $V_{CC} = V_{BB} = 0 \text{ V}$; $V_{bus} = 20 \text{ V}$ | -400 | -200 5 | 20 | μA |
| R_{bus} | Bus Pullup Resistance; Note 4 | $V_{TxD} = 0 \text{ V}$ | 20 | 30 | 47 | $\text{k}\Omega$ |
| $V_{bus,rd}$ | Receiver Threshold: Recessive-to-Dominant | | $0.4 \times V_{BB}$ | $0.48 \times V_{BB}$ | $0.6 \times V_{BB}$ | V |
| $V_{bus,dr}$ | Receiver Threshold: Dominant-to-Recessive | | $0.4 \times V_{BB}$ | $0.52 \times V_{BB}$ | $0.6 \times V_{BB}$ | V |
| V_q | Receiver Hysteresis | $V_{bus,hys} = V_{bus,rec} - V_{bus,dom}$ | $0.05 \times V_{BB}$ | $0.08 \times V_{BB}$ | $0.175 \times V_{BB}$ | V |
| V_{WAKE} | Wake-up Threshold Voltage | | $0.4 \times V_{BB}$ | | $0.6 \times V_{BB}$ | V |

4. Guaranteed by design. The total resistance of the pullup resistor and the serial diode is measured on ATE.

Table 5. AC ELECTRICAL CHARACTERISTICS ACCORDING TO LIN V13 $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BB} = 7.3\text{ V to }18\text{ V}$; $V_{EN} < V_{ENon}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$; $R_L = 500\ \Omega$ unless otherwise specified. Load for slope definitions (typical loads) = [L1] 1 nF 1 k Ω / [L2] 6.8 nF 600 Ω / [L3] 10 nF 500 Ω .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|---|-----------------------|-----|-----|-----|---------------|
| t_slope_F | Slope Time Falling Edge; (Note 5) | See Figure 5 | 4 | – | 24 | μs |
| t_slope_R | Slope Time Rising Edge; (Note 5) | See Figure 5 | 4 | – | 24 | μs |
| t_slope_Sym | Slope Time Symmetry; (Note 5) | t_slope_F – t_slope_R | –8 | – | +8 | μs |
| T_rec_F | Propagation Delay Bus Dominant to RxD = Low; (Note 6) | See Figures 4 and 5 | | 2 | 6 | μs |
| T_rec_R | Propagation Delay Bus Recessive to RxD = High; (Note 6) | See Figures 4 and 5 | | 6 | 6 | μs |
| t_WAKE | Wake-up Delay Time | | 30 | 100 | 200 | μs |

5. Guaranteed by design; not measured for all supply/load combinations on ATE.

6. Not measured on ATE.

Table 6. AC ELECTRICAL CHARACTERISTICS ACCORDING TO LIN v2.0 $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BB} = 7.3\text{ V to }18\text{ V}$; $V_{EN} < V_{ENon}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$; $R_L = 500\ \Omega$ unless otherwise specified. Load for slope definitions (typical loads) = [L1] 1 nF 1 k Ω / [L2] 6.8 nF 600 Ω / [L3] 10 nF 500 Ω .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|-------------------|-----|-----|-----|---------------|
| DYNAMIC RECEIVER CHARACTERISTICS ACCORDING TO LIN v2.0 | | | | | | |
| trx_pdr | Propagation Delay Bus Dominant to RxD = Low; (Note 7) | See Figure 6 | | | 6 | μs |
| trx_pdf | Propagation Delay Bus Recessive to RxD = High; (Note 7) | See Figure 6 | | | 6 | μs |
| trx_sym | Symmetry of Receiver Propagation Delay | trx_pdr – trx_pdf | –2 | – | +2 | μs |

DYNAMIC TRANSMITTER CHARACTERISTICS ACCORDING TO LIN v2.0

| | | | | | | |
|----|--|--|-------|--|-------|--|
| D1 | Duty Cycle 1 = $t_{Bus_rec(min)}/(2 \times t_{Bit})$; See Figure | | 0.396 | | 0.5 | |
| D1 | Duty Cycle 1 = $t_{Bus_rec(min)}/(2 \times t_{Bit})$; See Figure 6 | THRec(max) = $0.744 \times V_{bat}$; THDom(max) = $0.581 \times V_{bat}$; $V_{bat} = 7.0\text{ V to }18\text{ V}$; $t_{Bit} = 50\ \mu\text{s}$ THRec(max) = $0.744 \times V_{bat}$; THDom(max) = $0.581 \times V_{bat}$; $V_{bat} = 7.0\text{ V}$; $t_{Bit} = 50\ \mu\text{s}$; $t_{amb} = -40^\circ\text{C}$ | 0.366 | | 0.5 | |
| D2 | Duty Cycle 2 = $t_{Bus_rec(max)}/(2 \times t_{Bit})$; See Figure 6 | THRec(min) = $0.284 \times V_{bat}$; THDom(min) = $0.422 \times V_{bat}$; $V_{bat} = 7.6\text{ V to }18\text{ V}$; $t_{Bit} = 50\ \mu\text{s}$; | 0.5 | | 0.581 | |

7. Not measured on ATE.

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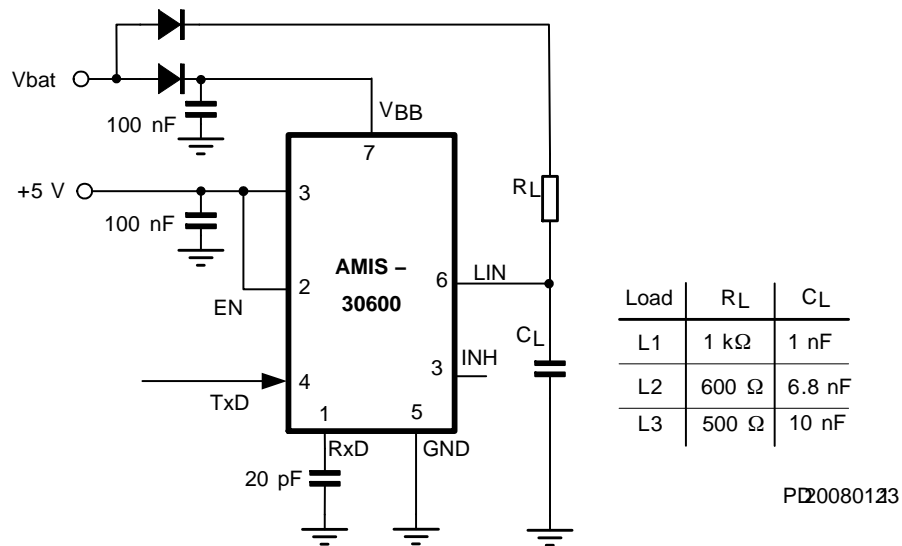


Figure 4. Test Circuit for Timing Characteristics

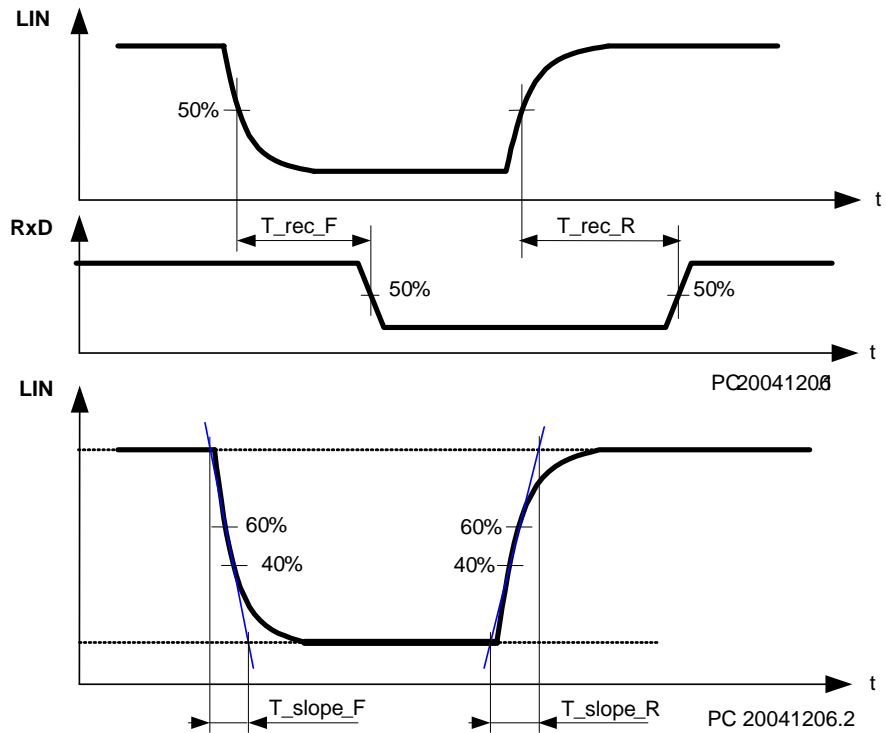


Figure 5. Timing Diagram for AC Characteristics According to LIN 1.3

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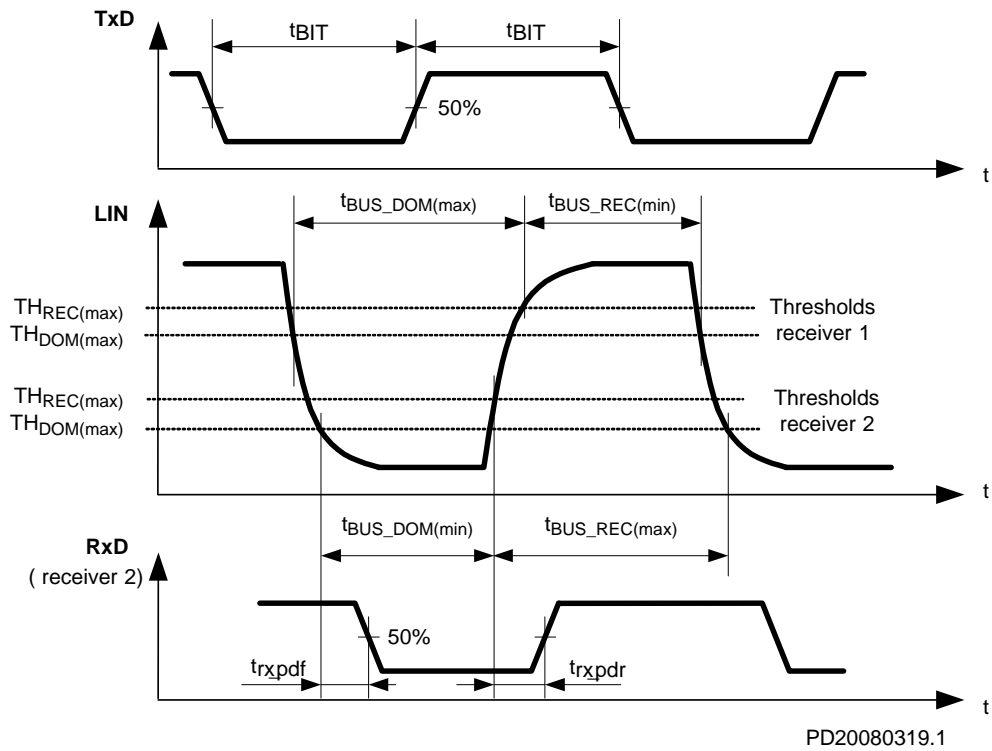


Figure 6. Timing Diagram for AC Characteristics According to LIN 2.0

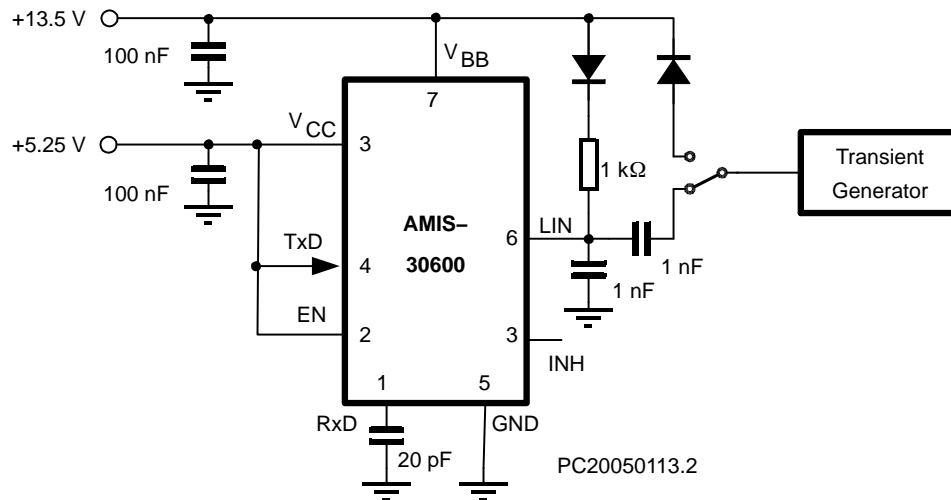


Figure 7. Test Circuit for Transient Measurements

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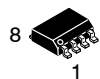
DEVICE ORDERING INFORMATION

| Part Number | Temperature Range | Package Type | Shipping [†] |
|------------------|-------------------|---------------------|-----------------------|
| AMIS30600LINI1G | –40°C – 125°C | SOIC–8 (Pb–Free) | 96 Tube / Tray |
| AMIS30600LINI1RG | –40°C – 125°C | SOIC–8 (Pb–Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

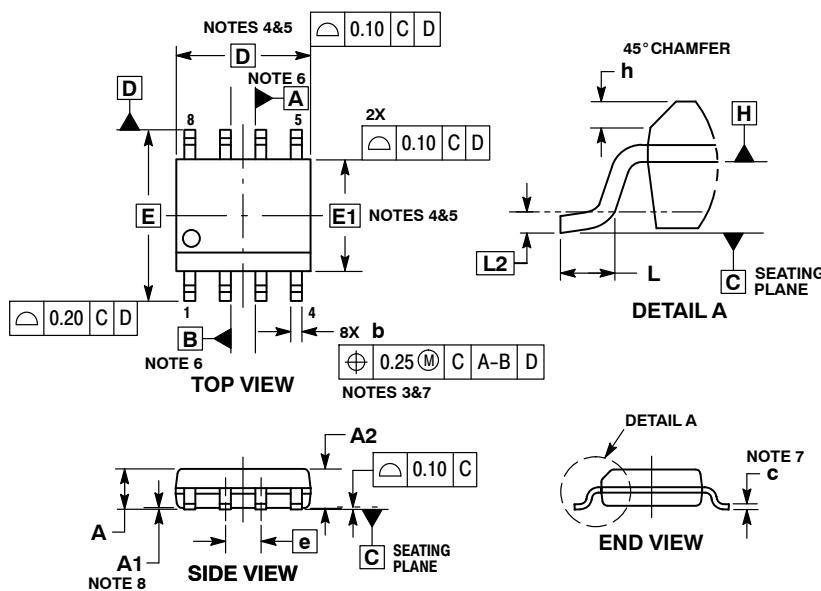
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SCALE 1:1

SOIC-8 CASE 751AZ ISSUE B

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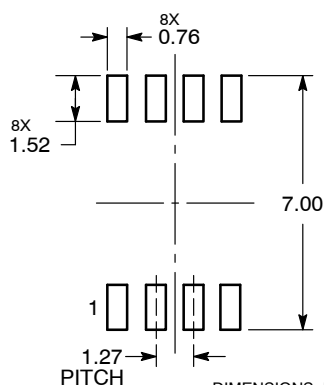


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

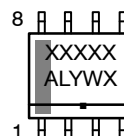
| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | --- |
| b | 0.31 | 0.51 |
| c | 0.10 | 0.25 |
| D | 4.90 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| h | 0.25 | 0.41 |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

| | | |
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