

FDS6900S

Dual N-Ch PowerTrench[®] SyncFet[™]

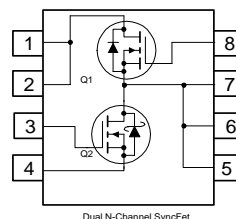
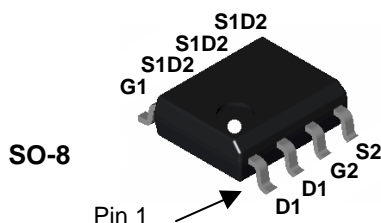
General Description

The FDS6900S is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6900S contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

Features

- Q2:** Optimized to minimize conduction losses
 Includes SyncFET Schottky body diode
 8.2A, 30V $R_{DS(on)} = 22m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 29m\Omega @ V_{GS} = 4.5V$
- Q1:** Optimized for low switching losses
 Low Gate Charge (8 nC typical)
 6.9A, 30V $R_{DS(on)} = 30m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 37m\Omega @ V_{GS} = 4.5V$



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q2	Q1	Units
V_{DSS}	Drain-Source Voltage	30	30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	8.2	6.9	A
	- Pulsed	30	20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6900S	FDS6900S	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

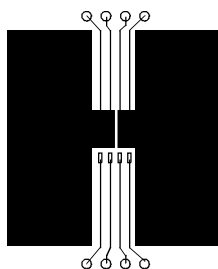
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C $I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	Q2 Q1		20 24		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	Q2 Q1			500 1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	Q2 Q1			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	Q2 Q1			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$ $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Q2 Q1	1 1	2.3 1.4	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C $I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	Q2 Q1		-5.5 -5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.2\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8.2\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 7.6\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.9\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.9\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 6.2\text{ A}$	Q2 Q1		13 20 20 25 38 30	22 36 29 30 49 37	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 8.2\text{ A}$ $V_{DS} = 5\text{ V}, I_D = 6.9\text{ A}$	Q2 Q1		69 18		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q2 Q1		1238 771		pF
C_{oss}	Output Capacitance		Q2 Q1		351 180		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		116 72		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	Q2 Q1		1.2 1.7		Ω
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q2 Q1		13 9	23 18	ns
t_r	Turn-On Rise Time		Q2 Q1		14 5	25 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		29 26	46 42	ns
t_f	Turn-Off Fall Time		Q2 Q1		11 4	20 8	ns
Q_g	Total Gate Charge	Q2: $V_{DS} = 15\text{ V}, I_D = 8.2\text{ A}, V_{GS} = 5\text{ V}$	Q2 Q1		12 8	17 11	nC
Q_{gs}	Gate-Source Charge	Q1: $V_{DS} = 15\text{ V}, I_D = 6.9\text{ A}, V_{GS} = 5\text{ V}$	Q2 Q1		4 2		nC
Q_{gd}	Gate-Drain Charge		Q2 Q1		4.3 2.5		nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

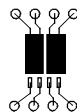
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			2.3 1.3	A
T_{rr}	Reverse Recovery Time	$I_F = 8.2\text{ A}$, $dI_F/dt = 300\text{ A}/\mu\text{s}$ (Note 3)	Q2		17		ns
Q_{rr}	Reverse Recovery Charge				24		nC
T_{rr}	Reverse Recovery Time	$I_F = 6.9\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 3)	Q1		18		ns
Q_{rr}	Reverse Recovery Charge				15		nC
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.3\text{ A}$ (Note 2)	Q2		0.4	0.7	V
		$V_{GS} = 0\text{ V}$, $I_S = 5\text{ A}$ (Note 2)	Q2		0.6	1.0	
		$V_{GS} = 0\text{ V}$, $I_S = 1.3\text{ A}$ (Note 2)	Q1		0.7	1.2	

Notes:

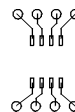
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 0.5in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a 0.02in^2 pad of 2 oz copper



c) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

3. See "SyncFET Schottky body diode characteristics" below.

Typical Characteristics: Q2

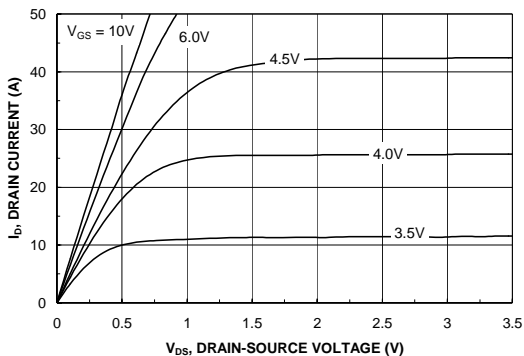


Figure 1. On-Region Characteristics.

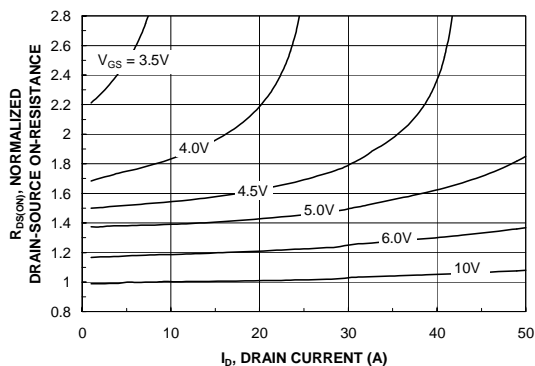


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

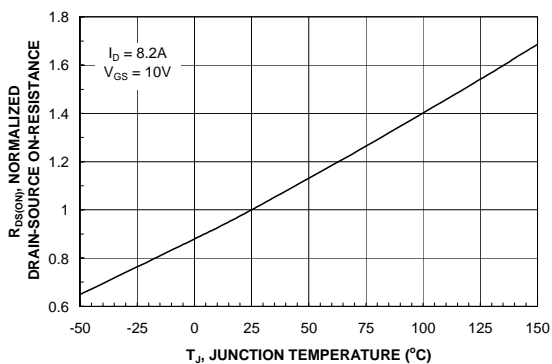


Figure 3. On-Resistance Variation with Temperature.

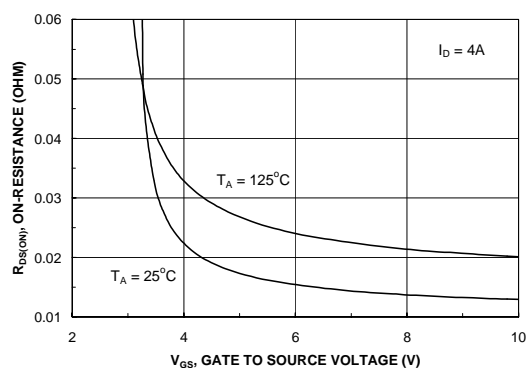


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

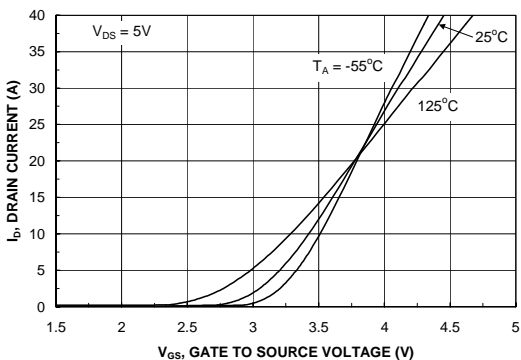


Figure 5. Transfer Characteristics.

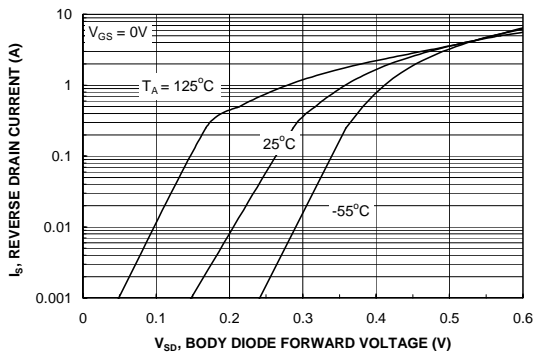


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

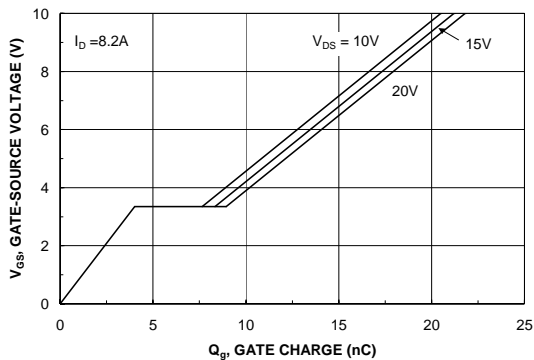


Figure 7. Gate Charge Characteristics.

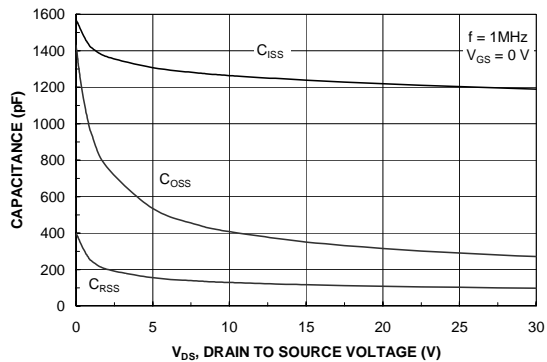


Figure 8. Capacitance Characteristics.

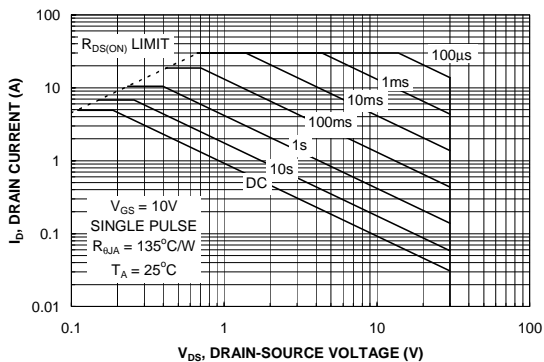


Figure 9. Maximum Safe Operating Area.

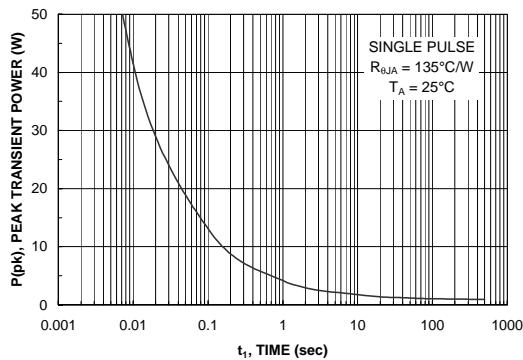


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics Q1

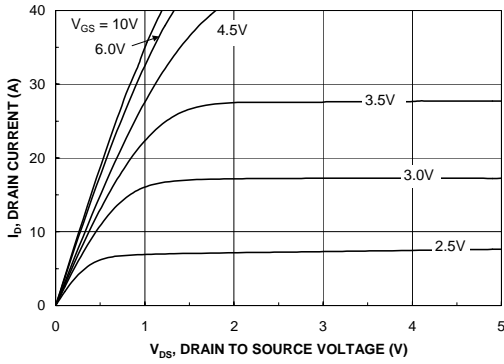


Figure 11. On-Region Characteristics.

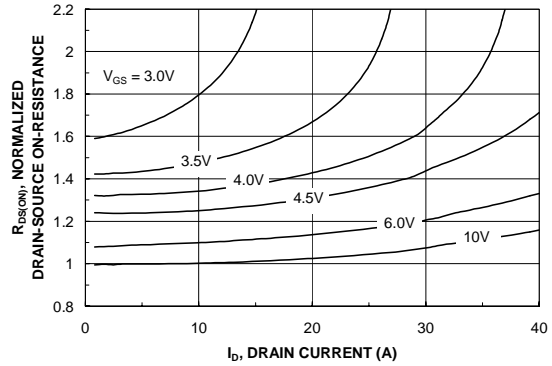


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

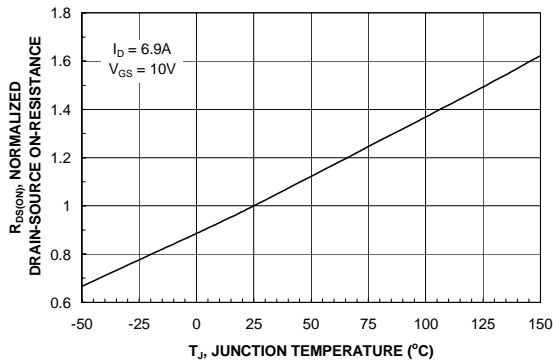


Figure 13. On-Resistance Variation with Temperature.

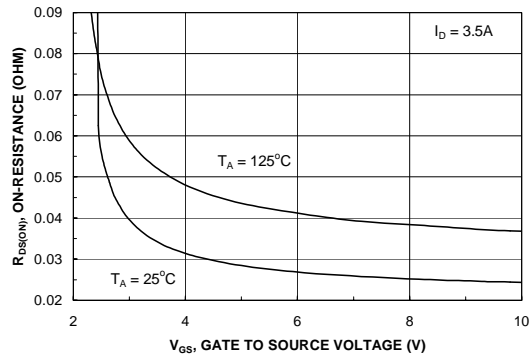


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

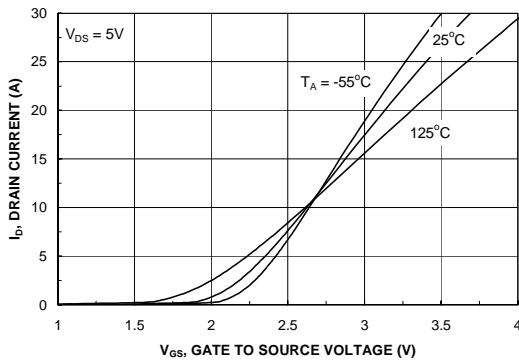


Figure 15. Transfer Characteristics.

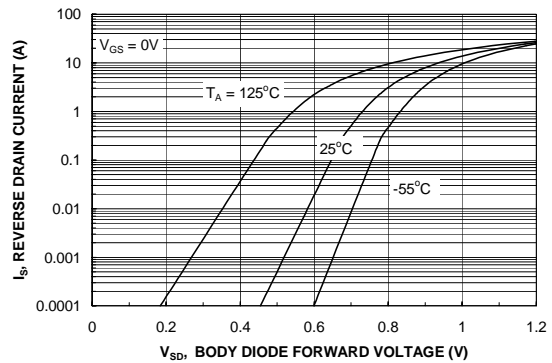


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

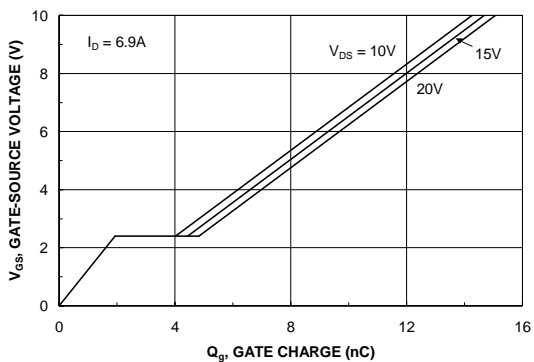


Figure 17. Gate Charge Characteristics.

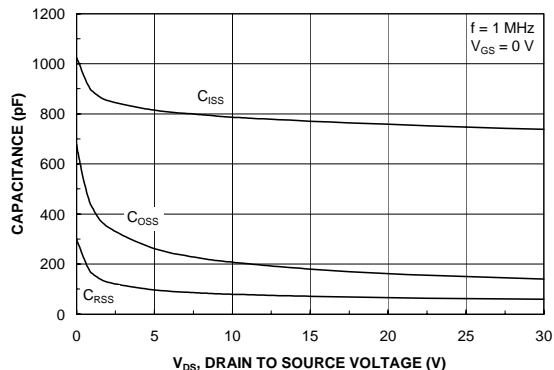


Figure 18. Capacitance Characteristics.

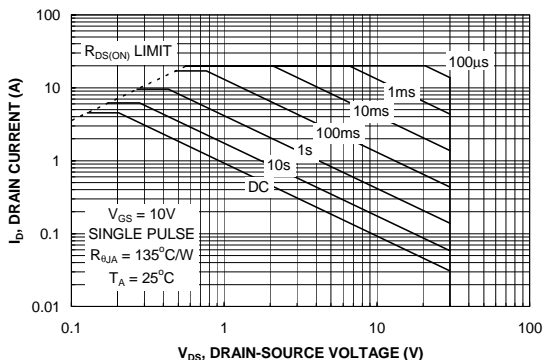


Figure 19. Maximum Safe Operating Area.

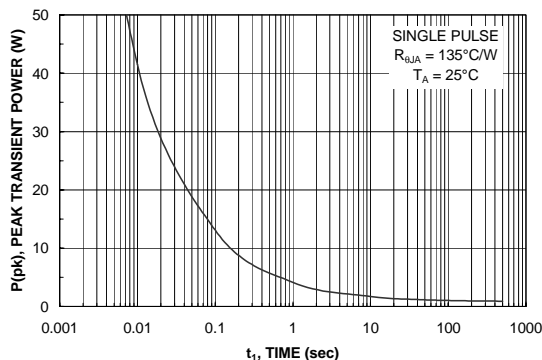


Figure 20. Single Pulse Maximum Power Dissipation.

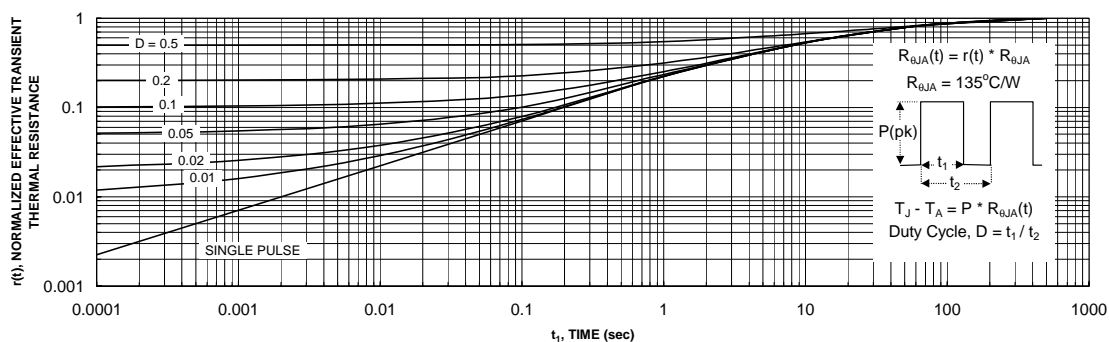


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued) This section copied from FDS6984S datasheet

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. **Figure 22** shows the reverse recovery characteristic of the FDS6900S.

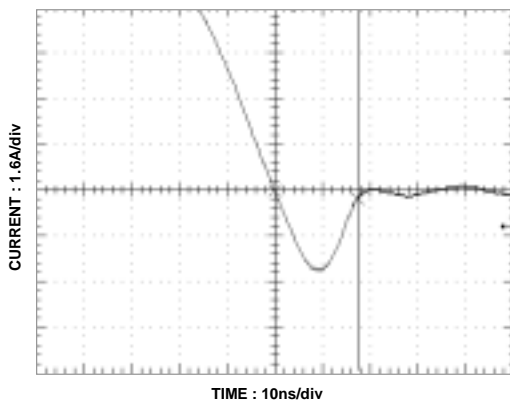


Figure 22. FDS6900S SyncFET body diode reverse recovery characteristic.

For comparison purposes, **Figure 23** shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690).

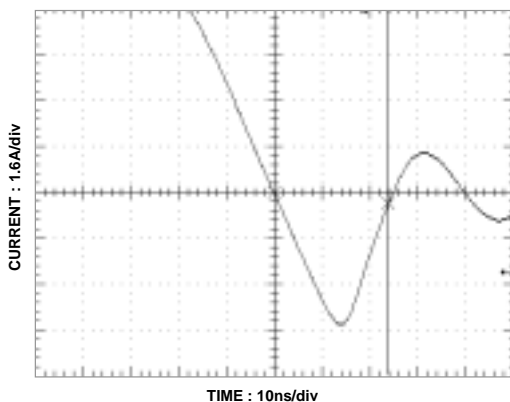


Figure 23. Non-SyncFET (FDS6690) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

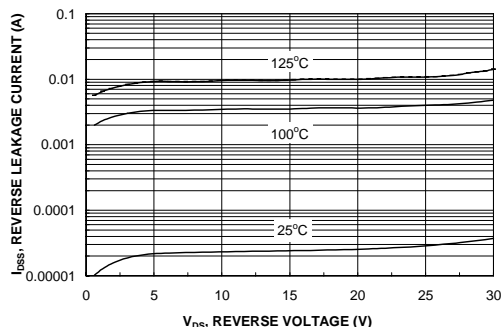


Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E ² CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	ꞆC™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.