

FDS7082N3

30V N-Channel PowerTrench® MOSFET

General Description

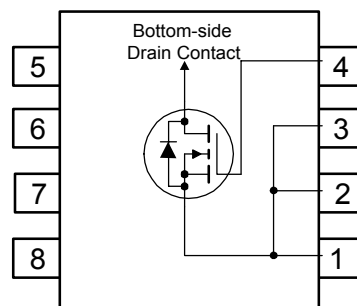
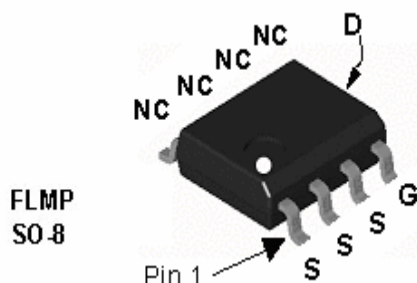
This N-Channel MOSFET in the thermally enhanced SO8 FLMP package has been designed specifically to improve the overall efficiency of DC/DC converters. Providing a balance of low $R_{DS(ON)}$ and Q_g it is ideal for synchronous rectifier applications in both isolated and non-isolated topologies. It is also well suited for both high and low side switch applications in Point of Load converters.

Applications

- Secondary side Synchronous rectifier
- Synchronous Buck VRM and POL Converters

Features

- 17.5 A, 30 V $R_{DS(ON)} = 6 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 8 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low Q_g and R_g for fast switching
- FLMP SO-8 package for enhanced thermal performance in an industry-standard package outline.



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	17.5	A
	– Pulsed	60	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	3.0	W
		1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7082N3	FDS7082N3	13"	12mm	2500 units

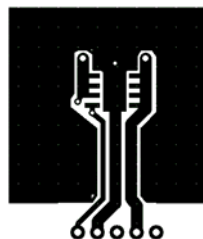
Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			10	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		–4.3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 17.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 15.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 17.5\text{ A}, T_J = 125^\circ\text{C}$		4.9 6.5 5.0	6.0 8.0 8.0	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 17.5\text{ A}$		116		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2271		pF
C_{oss}	Output Capacitance			554		pF
C_{rss}	Reverse Transfer Capacitance			213		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		14	20	ns
t_r	Turn–On Rise Time			12	37	ns
$t_{d(off)}$	Turn–Off Delay Time			38	64	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}$		43	53	nC
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 5\text{ V}$		22	31	nC
Q_{gs}	Gate–Source Charge			6.8		nC
Q_{gd}	Gate–Drain Charge			6.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.5\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 17.5\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		31		nS
Q_{rr}	Diode Reverse Recovery Charge			21		nC

Electrical Characteristics

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1in² pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics

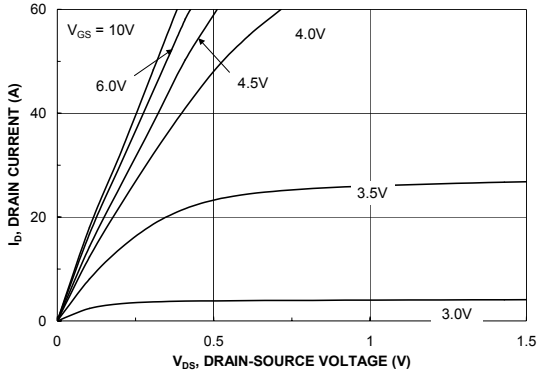


Figure 1. On-Region Characteristics.

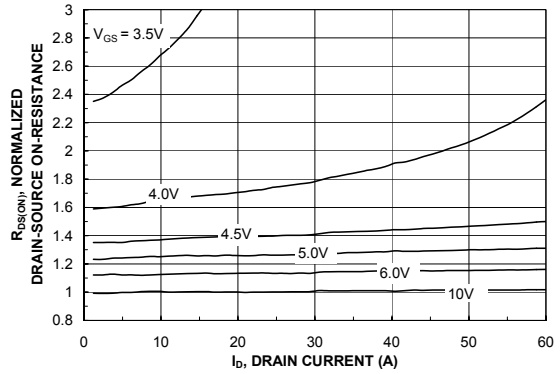


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

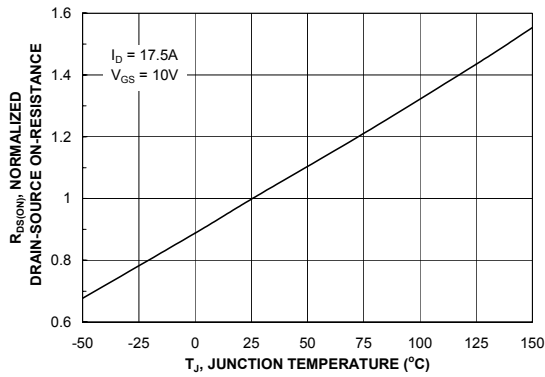


Figure 3. On-Resistance Variation with Temperature.

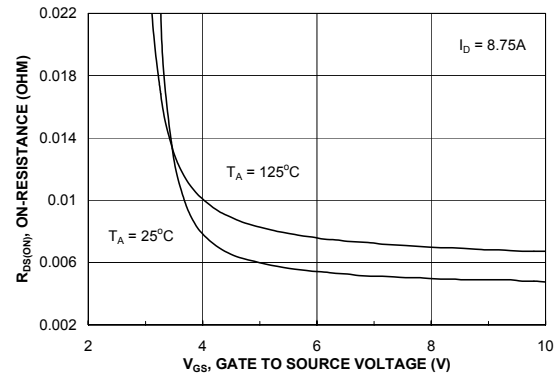


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

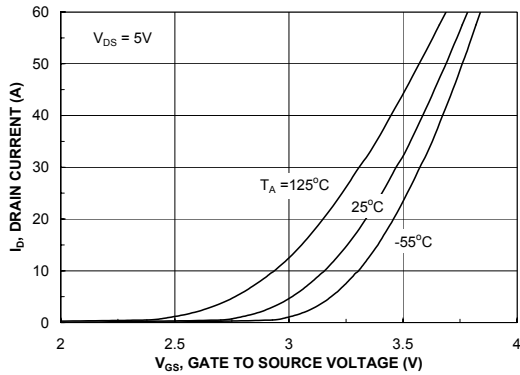


Figure 5. Transfer Characteristics.

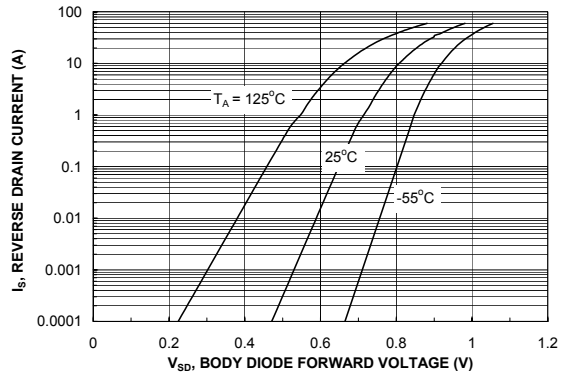


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

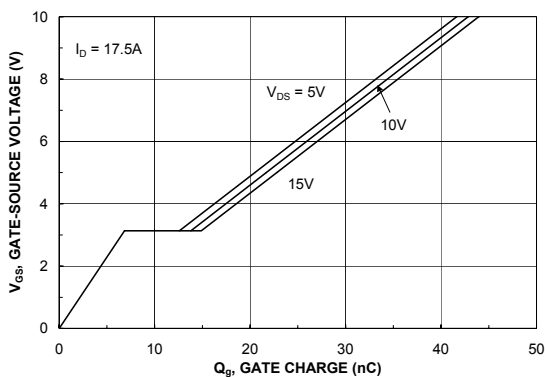


Figure 7. Gate Charge Characteristics.

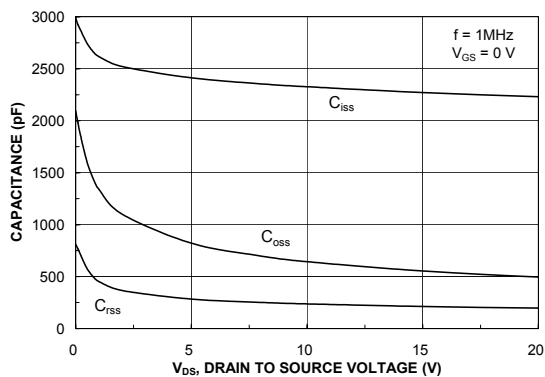


Figure 8. Capacitance Characteristics.

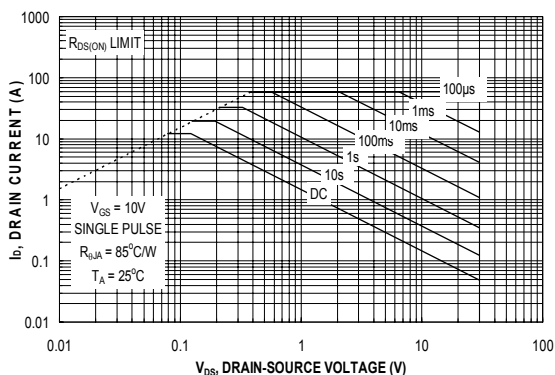


Figure 9. Maximum Safe Operating Area.

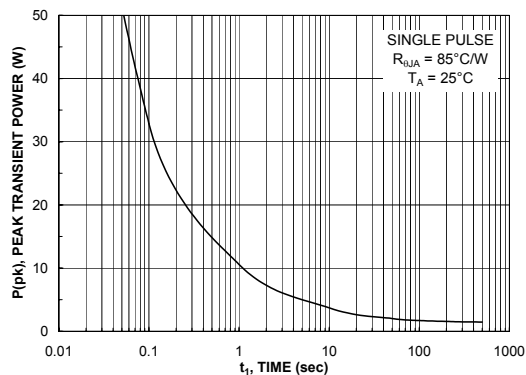


Figure 10. Single Pulse Maximum Power Dissipation.

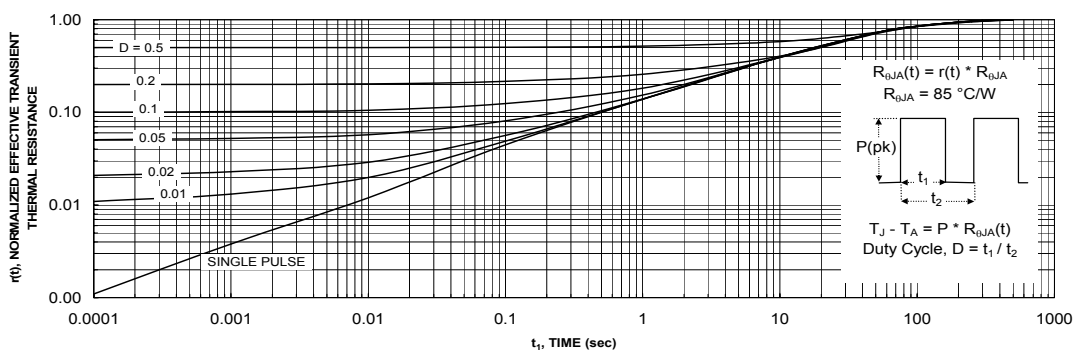
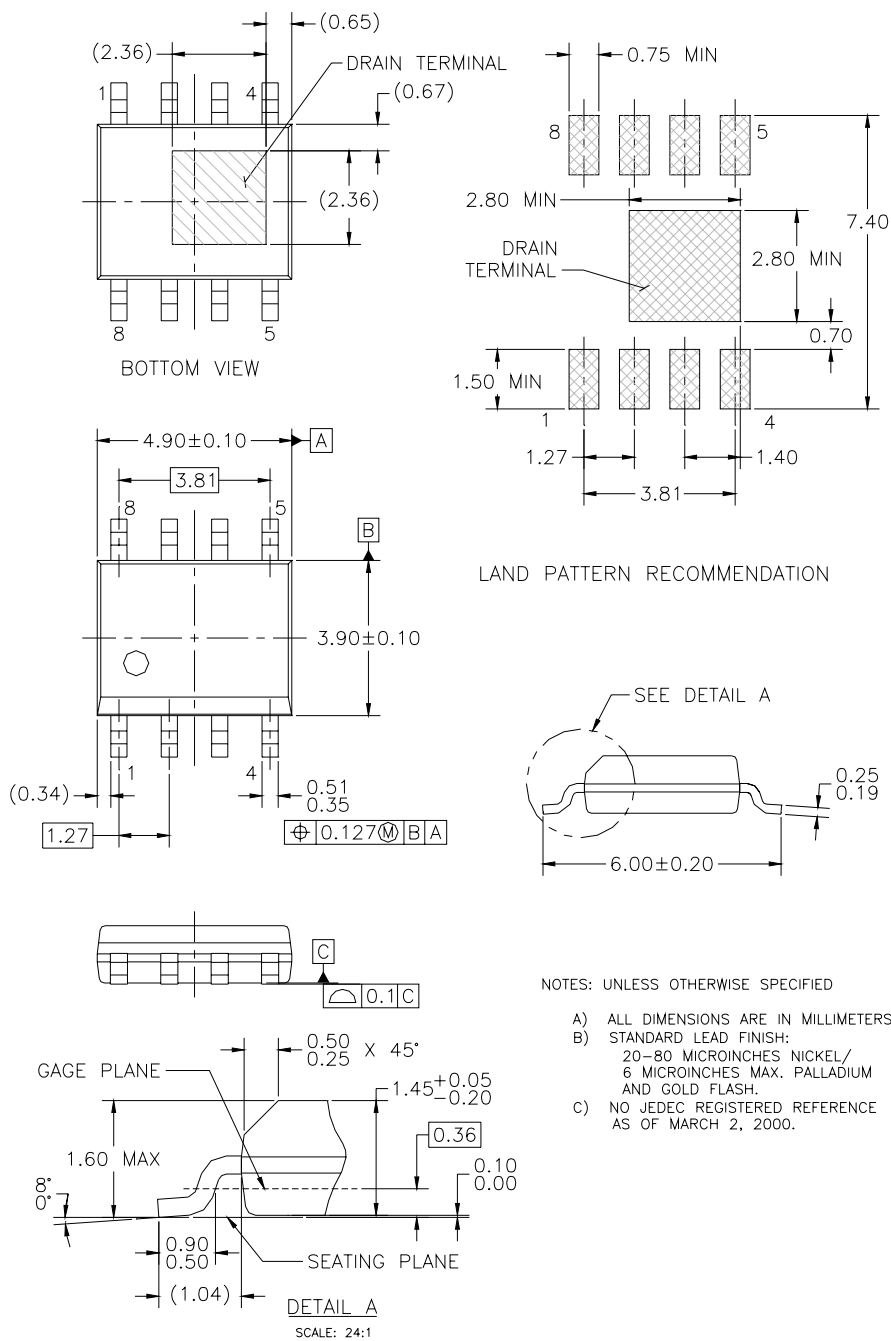


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) STANDARD LEAD FINISH:
20-80 MICROINCHES NICKEL/
6 MICROINCHES MAX. PALLADIUM
AND GOLD FLASH.
 - C) NO JEDEC REGISTERED REFERENCE
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