June 2007

DM74AS245
Octal Bus Transceiver with 3-STATE Outputs

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Non-inverting logic output
- 3-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

General Description

This advanced Schottky device contains 8 pairs of 3-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Ordering Information

Order Number	Package Number	Package Description
DM74AS245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74AS245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagram
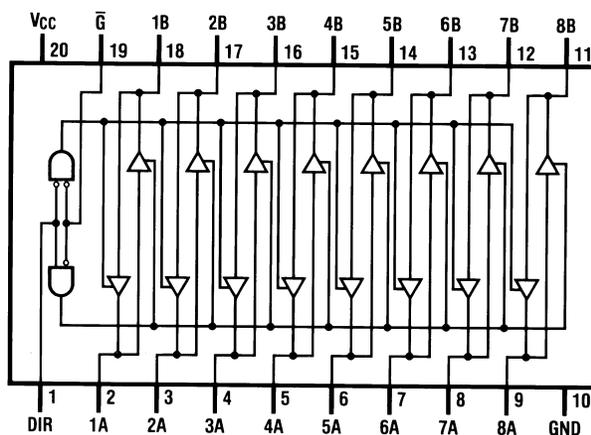
Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	
	Control Inputs	7V
	I/O Ports	5.5V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	−65°C to +150°C
θ_{JA}	Typical Thermal Resistance	76.0°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$				−1.2	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3mA$		2.4	3.2		V
		$V_{CC} = 4.5V$, $I_{OH} = -15mA$		2	2.3		
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to $5.5V$		$V_{CC} - 2$			
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} =$ Max.			0.35	0.55	V
I_I	Input Current at Max. Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$, ($V_{IN} = 5.5V$ for A or B Ports)				0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−50		−150	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Output HIGH		62	97	mA
			Output LOW		95	149	
			3-STATE		79	123	

Switching Characteristics

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min.	Max.	Units
t_{PLH}	Propagation Delay Time, HIGH-to-LOW Level Output	V_{CC} = 4.5V to 5.5V, R_1 = R_2 = 500Ω, C_L = 50pF	A or B	B or A	2	7.5	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		A or B	B or A	2	7	ns
t_{PZL}	Output Enable Time to LOW Level		G	A or B	2	8.5	ns
t_{PZH}	Output Enable Time to HIGH Level		G	A or B	2	9	ns
t_{PLZ}	Output Disable Time from LOW Level		G	A or B	2	9.5	ns
t_{PHZ}	Output Disable Time from HIGH Level		G	A or B	2	5.5	ns

Physical Dimensions

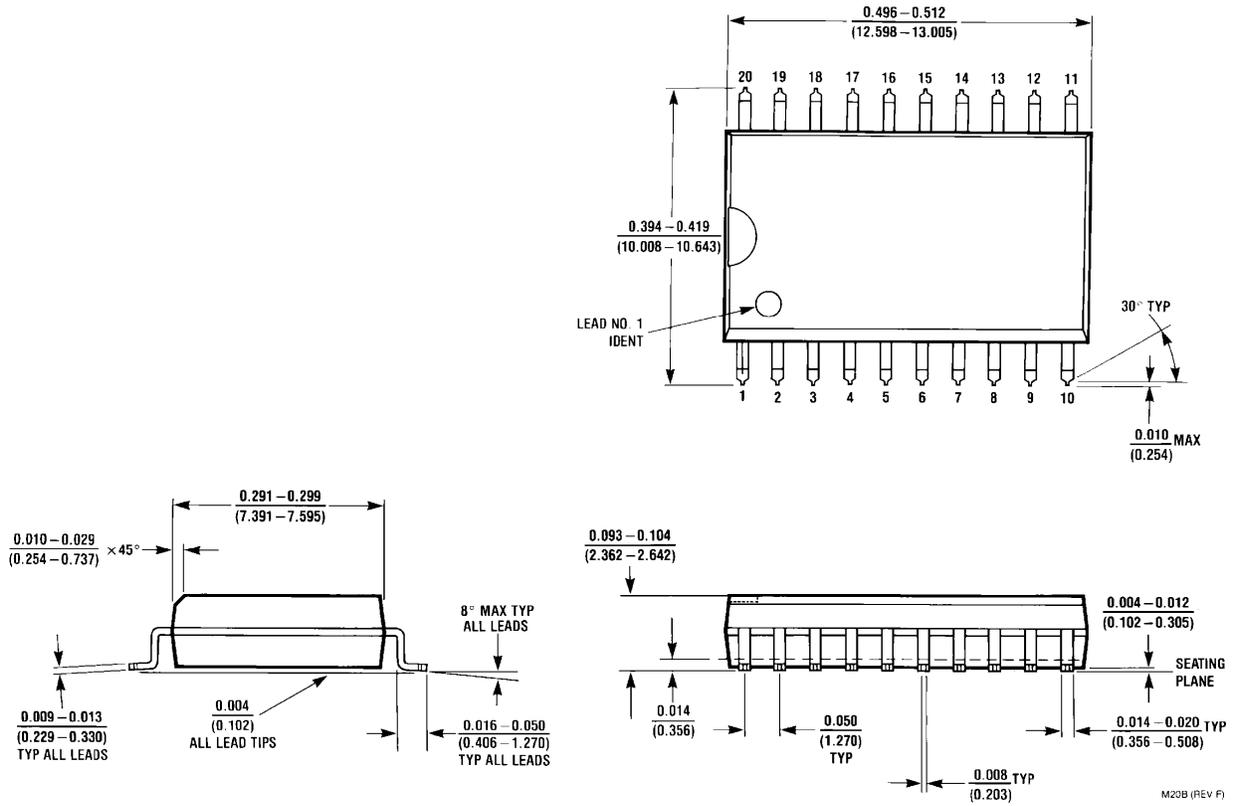Dimensions are in inches (millimeters) unless otherwise noted.

0.496 − 0.512
(12.598 − 13.005)

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) ×45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
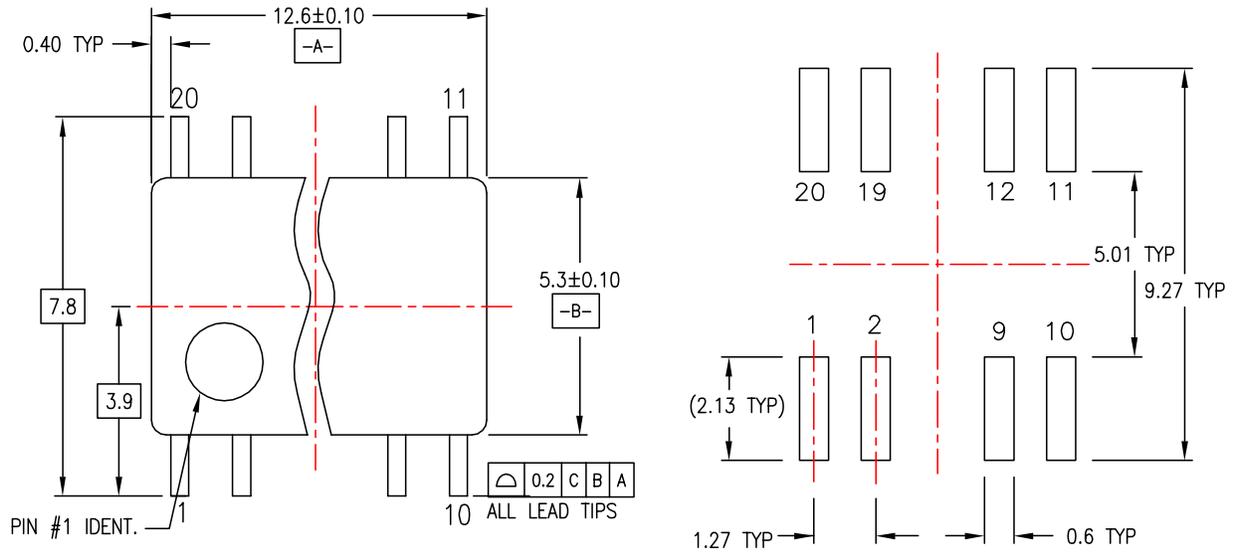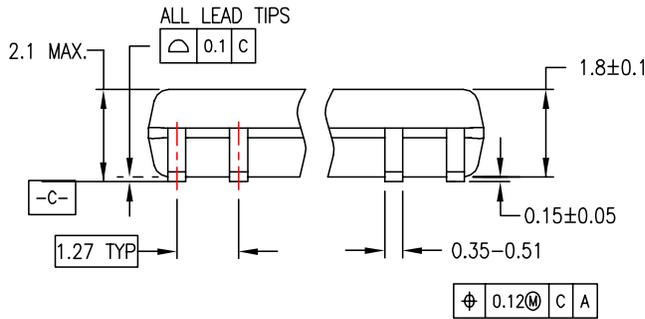(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M20B (REV F)

Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)
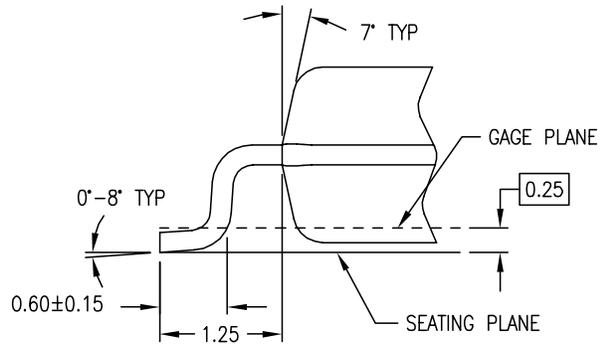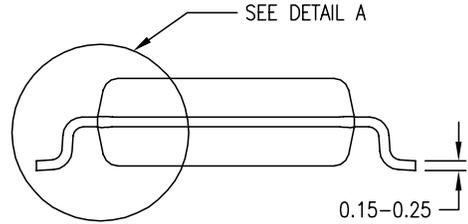Dimensions are in millimeters unless otherwise noted.

12.6±0.10
-A-

0.40 TYP

20   11

7.8

3.9

5.3±0.10
-B-

0.2 C B A

PIN #1 IDENT.   1   10   ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

20 19   12 11

5.01 TYP
9.27 TYP

1 2   9 10

(2.13 TYP)

1.27 TYP   0.6 TYP

ALL LEAD TIPS
0.1 C

2.1 MAX.

-C-

1.27 TYP

1.8±0.1

0.15±0.05

0.35−0.51

0.12 M C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0.25

0°−8° TYP

0.60±0.15

1.25

SEATING PLANE

DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

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FPS™	PDP-SPM™	SuperFET™	UHC®
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Global Power Resource℠	Power247®	SuperSOT™-6	VCX™
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Rev. I28