3.3 V Differential 1:21 Differential Fanout Clock Driver with HCSL level Output

NB4N121K

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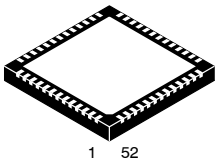


QFN−52
MN SUFFIX
CASE 485M

Description

The NB4N121K is a Clock differential input fanout distribution 1 to 21 HCSL level differential outputs, optimized for ultra low propagation delay variation. The NB4N121K is designed with HCSL clock distribution for FBDIMM applications in mind.

Inputs can accept differential LVPECL, CML, or LVDS levels. Single−ended LVPECL, CML, LVCMOS or LVTTL levels are accepted with the proper V_{REFAC} supply (see Figures 5, 10, 11, 12, and 13). Clock input pins incorporate an internal 50 Ω on die termination resistors.

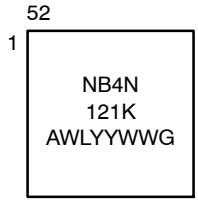
Output drive current at I_{REF} (Pin 1) for 1X load is selected by connecting to GND. To drive a 2X load, connect I_{REF} to V_{CC}. See Figure 9.

The NB4N121K specifically guarantees low output−to−output skews. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB4N121K's performance to distribute low skew clocks across the backplane or the motherboard.

Features

- Typical Input Clock Frequency 100, 133, 166, 200, 266, 333 and 400 MHz
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- Δtpd 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- Additive Phase RMS Jitter: 1 ps Max
- Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- Differential HCSL Output Level (700 mV Peak−to−Peak)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM*



A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

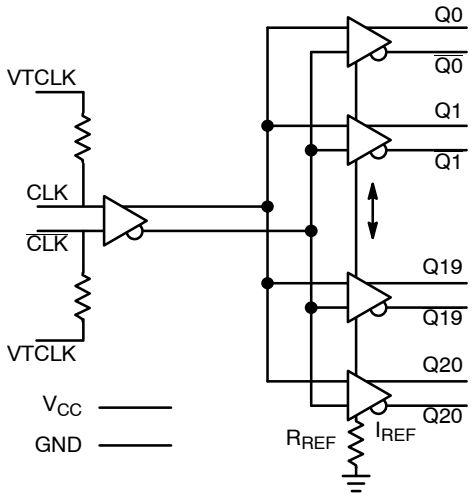


Figure 1. Pin Configuration (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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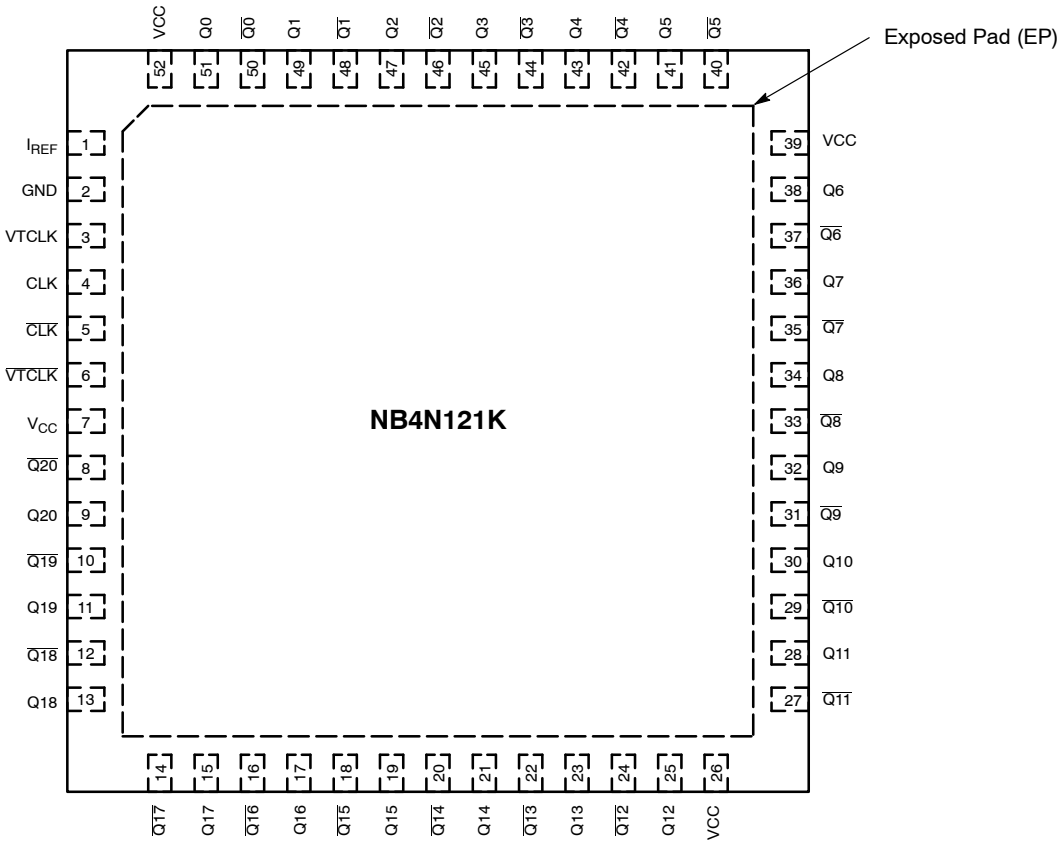


Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	I_{REF}	Output	Output current programming pin to select load drive. For 1X configuration, connect I_{REF} to GND, or for 2X configuration, connect I_{REF} to V_{CC} (See Figure 9).
2	GND	–	Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation.
3, 6	VTCLK, $\overline{VTCLK}$	–	Internal 50 Ω Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self−oscillation.
4	CLK	LVPECL Input	CLOCK Input (TRUE)
5	$\overline{CLK}$	LVPECL Input	CLOCK Input (INVERT)
7, 26, 39, 52	V_{CC}	–	Positive Supply pins. V_{CC} pins must be externally connected to a power supply to guarantee proper operation.
8, 10, 12, 14, 16, 18, 20, 22, 24, 27, 29, 31, 33, 35, 37, 40, 42, 44, 46, 48, 50	$\overline{Q[20-0]}$	HCSL Output	Output (INVERT)
9, 11, 13, 15, 17, 19, 21, 23, 25, 28, 30, 32, 34, 36, 38, 41, 43, 45, 47, 49, 51	Q[20−0]	HCSL Output	Output (TRUE)
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat−sinking conduit for proper thermal operation. (Note 1)

1. The exposed pad must be connected to the circuit board ground.

Table 2. ATTRIBUTES

Characteristic	Value
Input Default State Resistors	None
ESD Protection Human Body Model Machine Model	 >2 kV 400 V
Moisture Sensitivity (Note 2) QFN−52	 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	622
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Positive Input	GND = 0 V		GND − 0.3 ≤ V_I ≤ V_{CC}	V
V_{INPP}	Differential Input Voltage |CLK − CLKb|			V_{CC}	V
I_{OUT}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range	QFN−52		−40 to +70	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−52 QFN−52	25 19.6	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 4)	QFN−52	21	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS (V_{CC} = 3.0 V to 3.6 V, T_A = −40°C to +70°C Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
I_{GND}	GND Supply Current (All Outputs Loaded)		70	98	120	mA
I_{CC}	Power Supply Current (All Outputs Loaded)	1X 2X		420 780		mA
I_{IH}	Input HIGH Current CLKx, $\overline{CLKx}$			2.0	150	μA
I_{IL}	Input LOW Current CLKx, $\overline{CLKx}$		−150	−2.0		μA
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 5 and 7)						
V_{th}	Input Threshold Reference Voltage Range (Note 6)		1050		V_{CC} − 150	mV
V_{IH}	Single−Ended Input HIGH Voltage		V_{th} + 150		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage		GND		V_{th} − 150	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8)						
V_{IHD}	Differential Input HIGH Voltage		1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V_{CC} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})		75		2400	mV
V_{CMR}	Input Common Mode Range		1163		V_{CC} − 75	
HCSL OUTPUTS (Figure 4)						
V_{OH}	Output HIGH Voltage		600	740	900	mV
V_{OL}	Output LOW Voltage		−150	0	150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input parameters vary 1:1 with V_{CC}. Measurements taken with outputs in either 1X (all outputs loaded 50 Ω to GND) or 2X (all outputs loaded 25 Ω to GND) configuration, see Figure 9. For 1X configuration, connect $_{IREF}$ to GND, or for 2X configuration, connect $_{IREF}$ to V_{CC}.
6. V_{th} is applied to the complementary input when operating in single ended mode.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V; −40°C to +70°C (Note 7)

Symbol	Characteristic		Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$)	f_{in} = 133 MHz f_{in} = 166 MHz f_{in} = 200 MHz		725 725 725	900 900 900	mV
t_{PLH}, t_{PHL}	Propagation Delay to (See Figure 3)	CLK/$\overline{CLK}$ to Qx/$\overline{Qx}$	550	800	950	ps
Δt_{PLH}, Δt_{PHL}	Propagation Delay Variations Variation Per Each Diff Pair CLK/$\overline{CLK}$ to Qx/$\overline{Qx}$ (Note 8) (See Figure 3)				100	ps
t_{SKEW}	Duty Cycle Skew (Note 9) Within−Device Skew, 1X Mode Only (Note 10) Within−Device Skew, 2X Mode (Note 10) Device−to−Device Skew (Note 10)				20 50 80 150	ps ps ps ps
$t_{jit(\phi)}$	Additive RMS Phase RMS (Note 11) f_{in} =133 MHz to 200 MHz				1	ps
V_{cross}	Absolute Crossing Magnitude Voltage		250		550	mV
ΔV_{cross}	Variation in Magnitude of V_{cross}				150	mV
t_r, t_f	Absolute Magnitude in Output Risetime and Falltime (From 175 mV to 525 mV)	Qx, $\overline{Qx}$	175	340	700	ps
Δt_r, Δt_f	Variation in Magnitude of Risetime and Falltime (Single−Ended) (See Figure 4)	Qx, $\overline{Qx}$ 1X 2X			 125 150	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. Measurements taken with outputs in either 1X (all outputs loaded 50 Ω to GND) or 2X (all outputs loaded 25 Ω to GND) configuration, see Figure 9. For 1X configuration, connect I_{REF} to GND, or for 2X configuration, connect I_{REF} to V_{CC}. Typical gain is 20 dB.
8. Measured from the input pair crosspoint to each single output pair crosspoint across temp and voltage ranges.
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+.
10. Skew is measured between outputs under identical transition @ 133 MHz.
11. Additive RMS jitter with 50% duty cycle clock signal using phase noise integrated from 12 KHz to 33 MHz

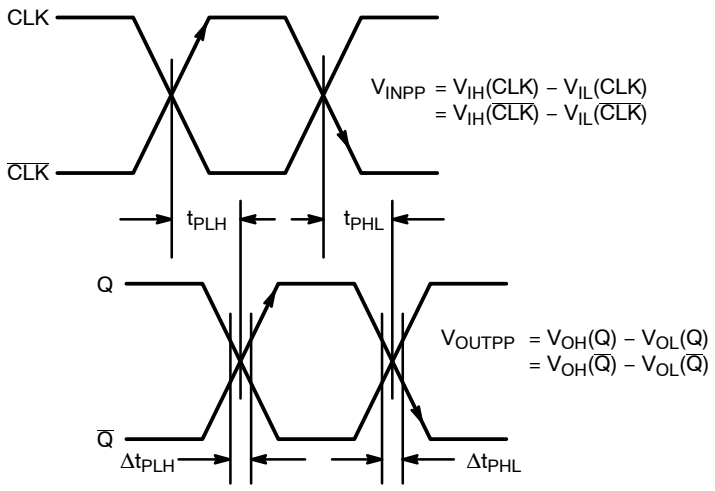


Figure 3. AC Reference Measurement

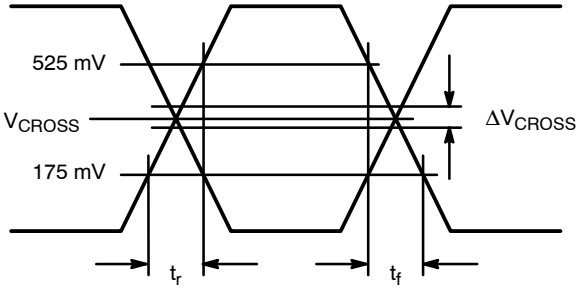


Figure 4. HCSL Output Parameter Characteristics

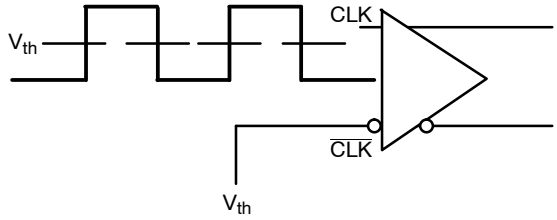


Figure 5. Differential Input Driven Single−Ended (V_{th} = V_{REFAC})

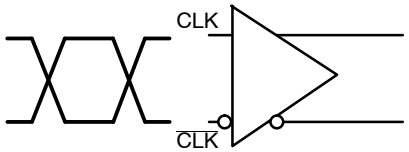


Figure 6. Differential Inputs Driven Differentially

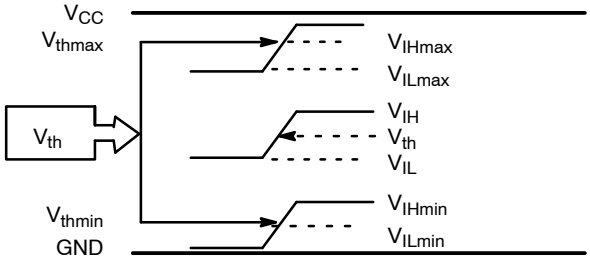


Figure 7. V_{th} Diagram

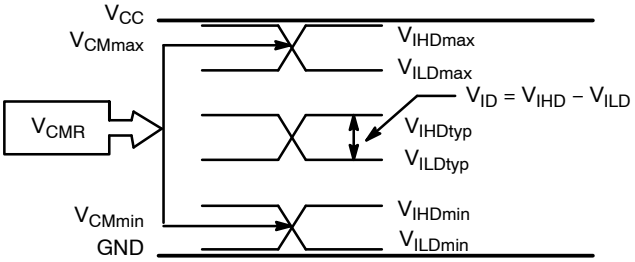
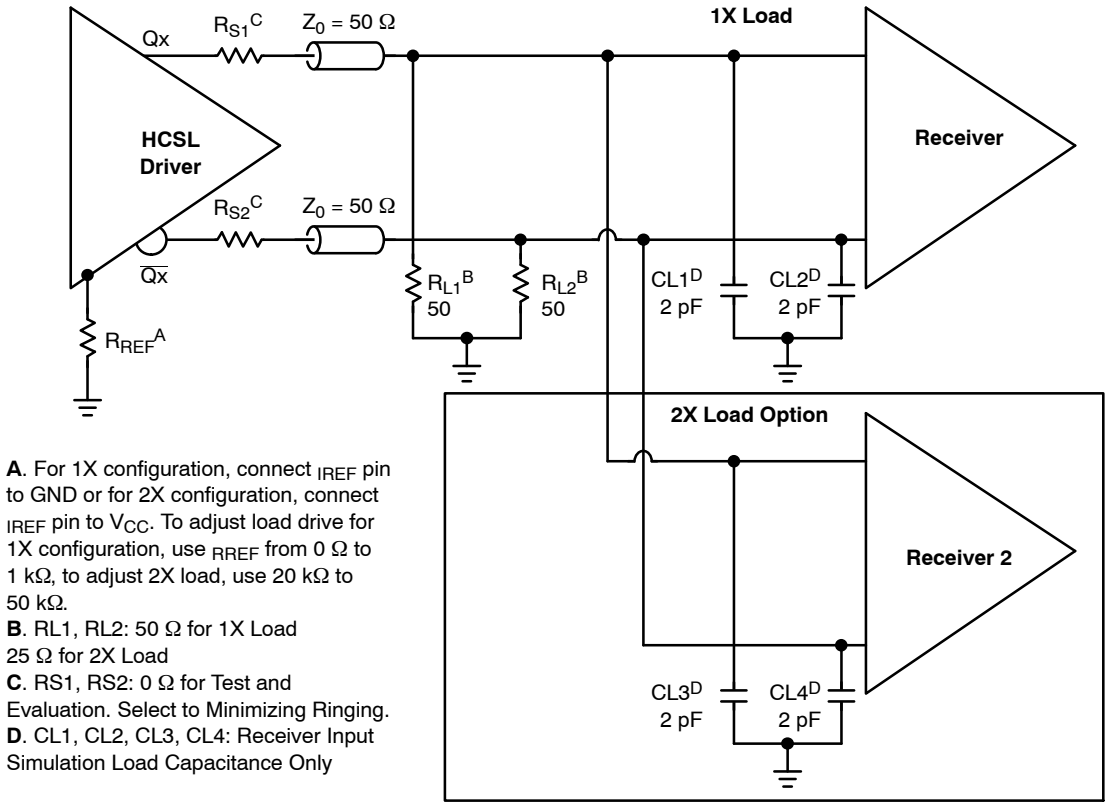
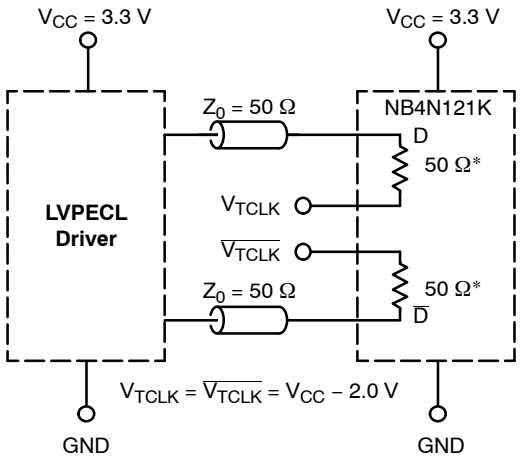


Figure 8. V_{CMR} Diagram



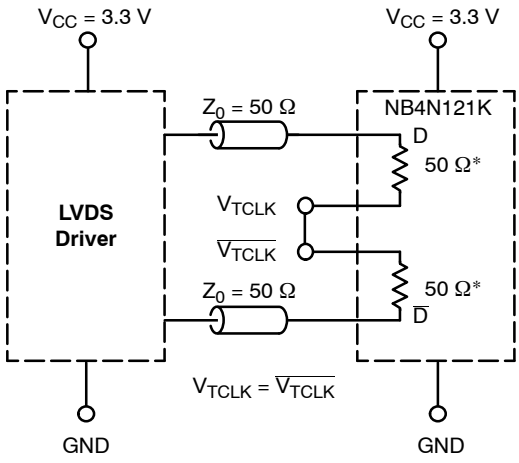
A. For 1X configuration, connect $_{IREF}$ pin to GND or for 2X configuration, connect $_{IREF}$ pin to V_{CC}. To adjust load drive for 1X configuration, use $_{RREF}$ from 0 Ω to 1 kΩ, to adjust 2X load, use 20 kΩ to 50 kΩ.
B. RL1, RL2: 50 Ω for 1X Load
25 Ω for 2X Load
C. RS1, RS2: 0 Ω for Test and Evaluation. Select to Minimizing Ringing.
D. CL1, CL2, CL3, CL4: Receiver Input Simulation Load Capacitance Only

Figure 9. Typical Termination Configuration for Output Driver and Device Evaluation C_{Lx} for Test Only (Representing Receiver Input Loading); Not Added to Application



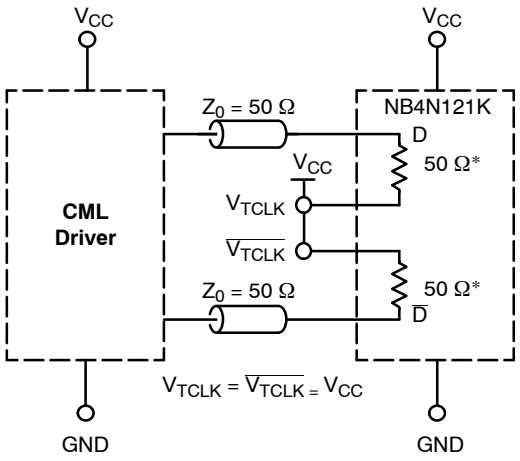
*RTIN, Internal Input Termination Resistor

Figure 10. LVPECL Interface



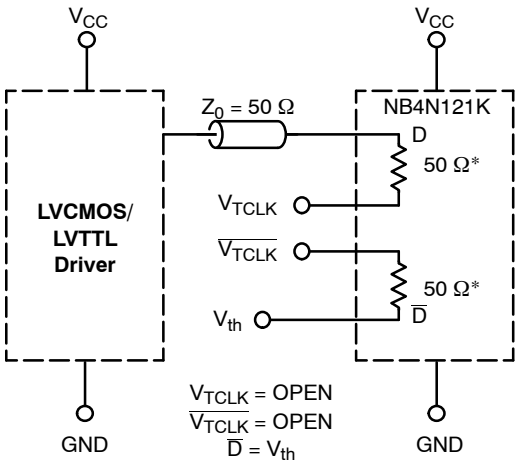
*RTIN, Internal Input Termination Resistor

Figure 11. LVDS Interface



*RTIN, Internal Input Termination Resistor

Figure 12. Standard 50 Ω Load CML Interface



*RTIN, Internal Input Termination Resistor

Figure 13. LVCMOS/LVTTL Interface

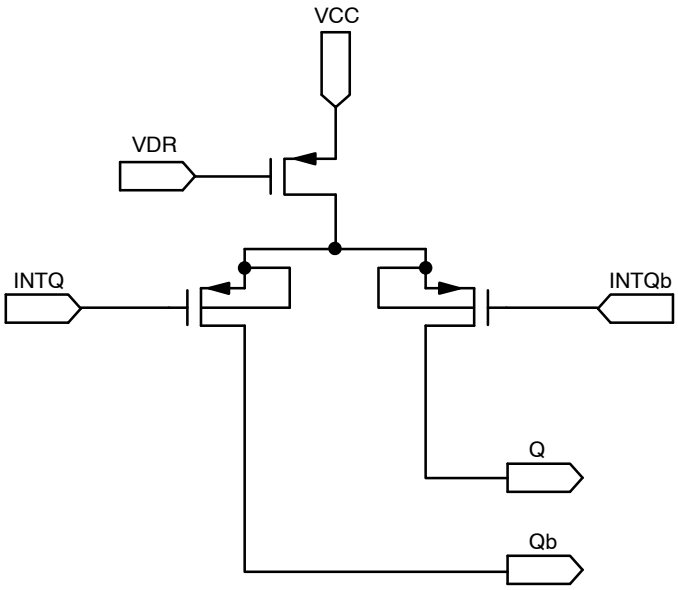


Figure 14. HCSL Output Structure

ORDERING INFORMATION

Device	Package	Shipping†
NB4N121KMNR2G	QFN−52 (Pb−Free)	2000 / Tape & Reel

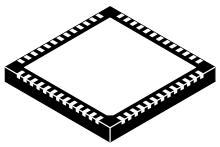
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

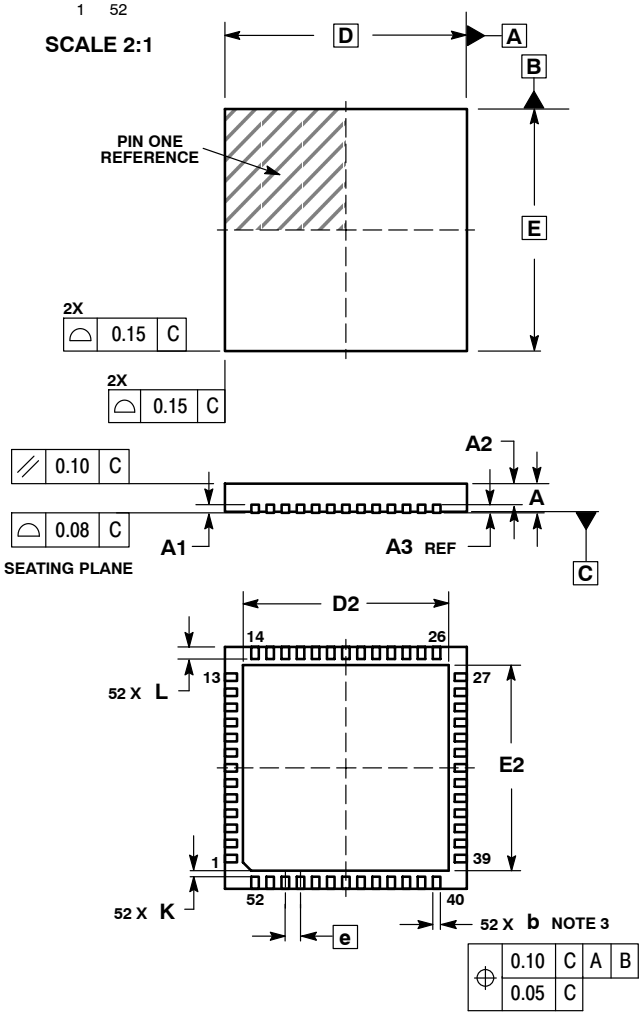
ON Semiconductor®

QFN52 8x8, 0.5P
CASE 485M−01
ISSUE C

DATE 16 FEB 2010



SCALE 2:1



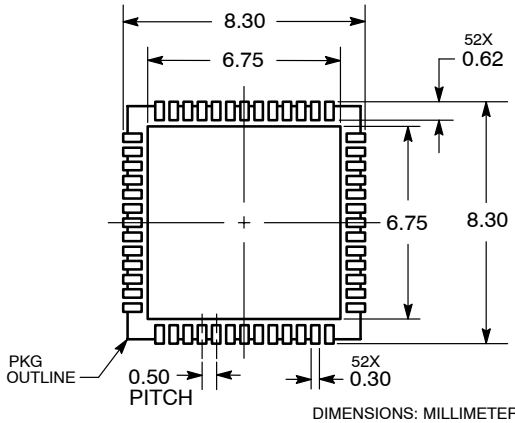
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

GENERIC MARKING DIAGRAM

XXXXXXXXX	= Device Code
A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**52 PIN QFN, 8X8, 0.5P**	**PAGE 1 OF 1**

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