FAIRCHILD SEMICONDUCTOR®

November 2008

FAN7390
High-Current, High and Low-Side, Gate-Drive IC

Features

- Floating Channels for Bootstrap Operation to +600V
- Typically 4.5A/4.5A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- Logic (V_{SS}) and Power (COM) Ground +/- 7V Offset
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input

Applications

- PDP Sustain Driver
- HID Lamp Ballast
- SMPS
- Motor Driver

Description

The FAN7390 is a monolithic high- and low-side gate-drive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to V_S=-9.8V (typical) for V_{BS}=15V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop feature make this device suitable for the PDP sustain pulse driver, motor driver, switching power supply, and high-power DC-DC converter applications.

8-SOP **8-DIP** **14-SOP**

Ordering Information

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN7390N	8-DIP	-40°C ~ 125°C	RoHS	Tube
FAN7390M	8-SOP			Tube
FAN7390MX				Tape & Reel
FAN7390M1	14-SOIC			Tube
FAN7390M1X				Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Circuit

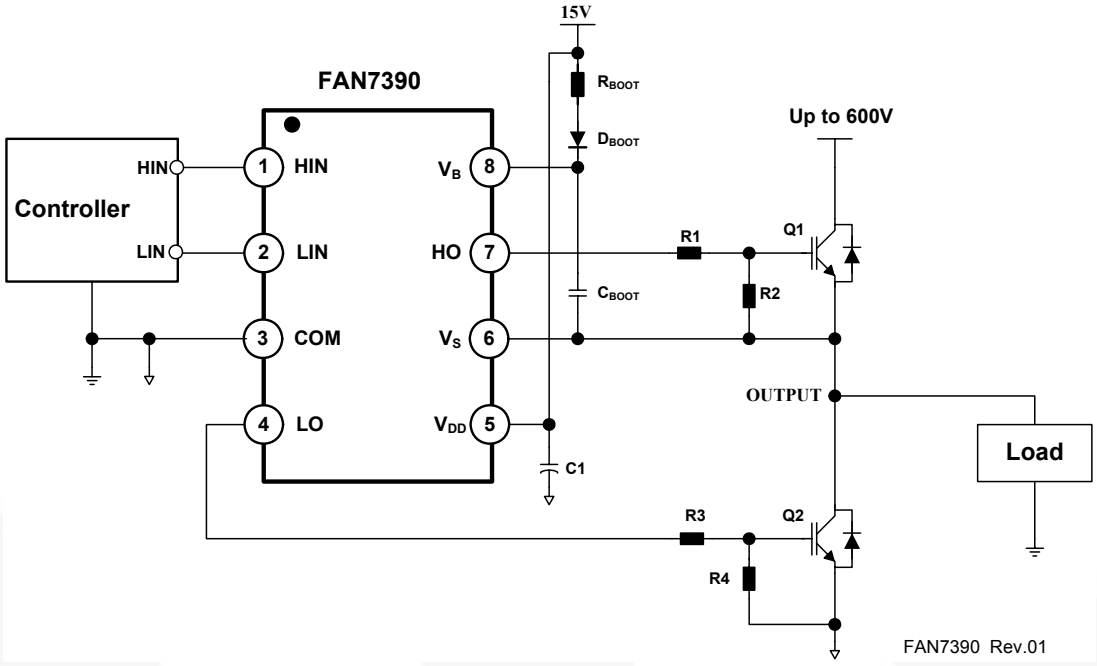

Figure 1. Application Circuit for Half-Bridge (Referenced 8-SOP/DIP)

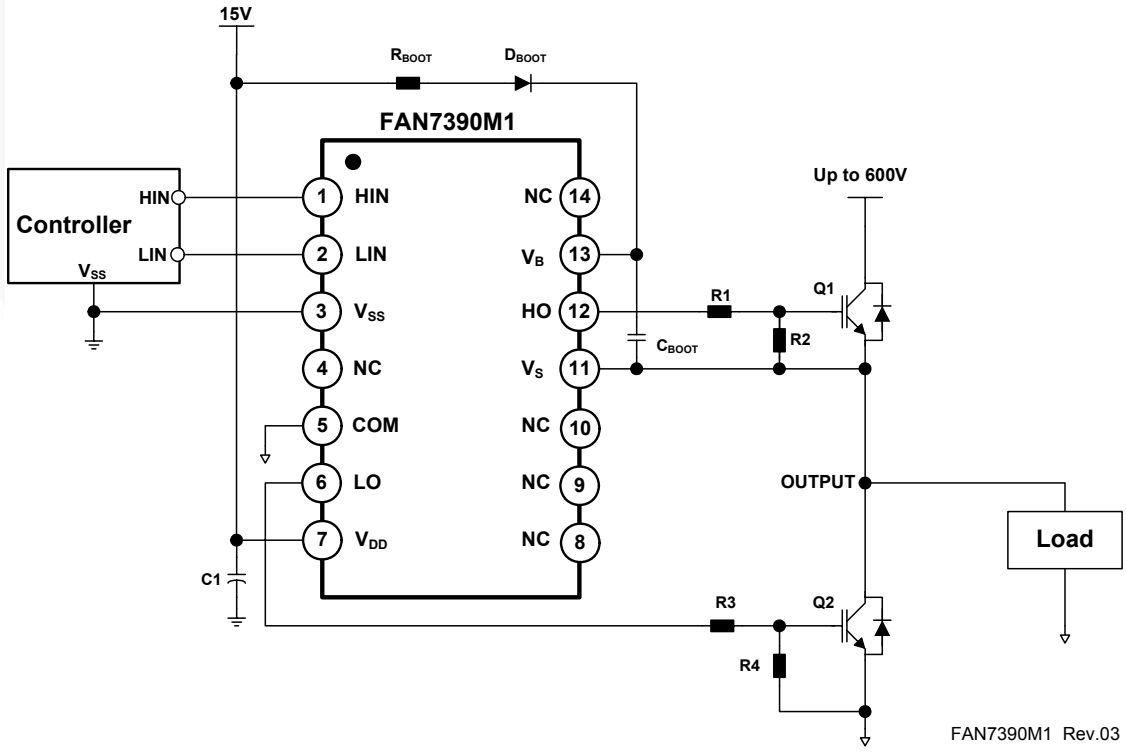

Figure 2. Application Circuit for Half-Bridge (Referenced 14-SOIC)

Internal Block Diagram

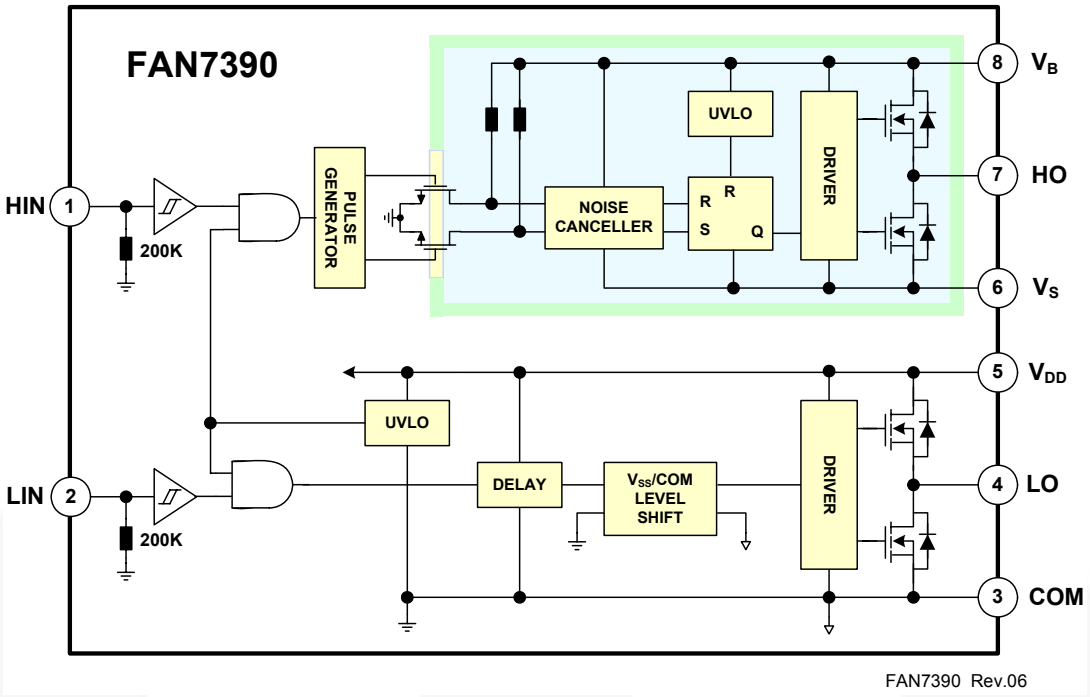

Figure 3. Functional Block Diagram (Referenced 8-SOP/DIP)

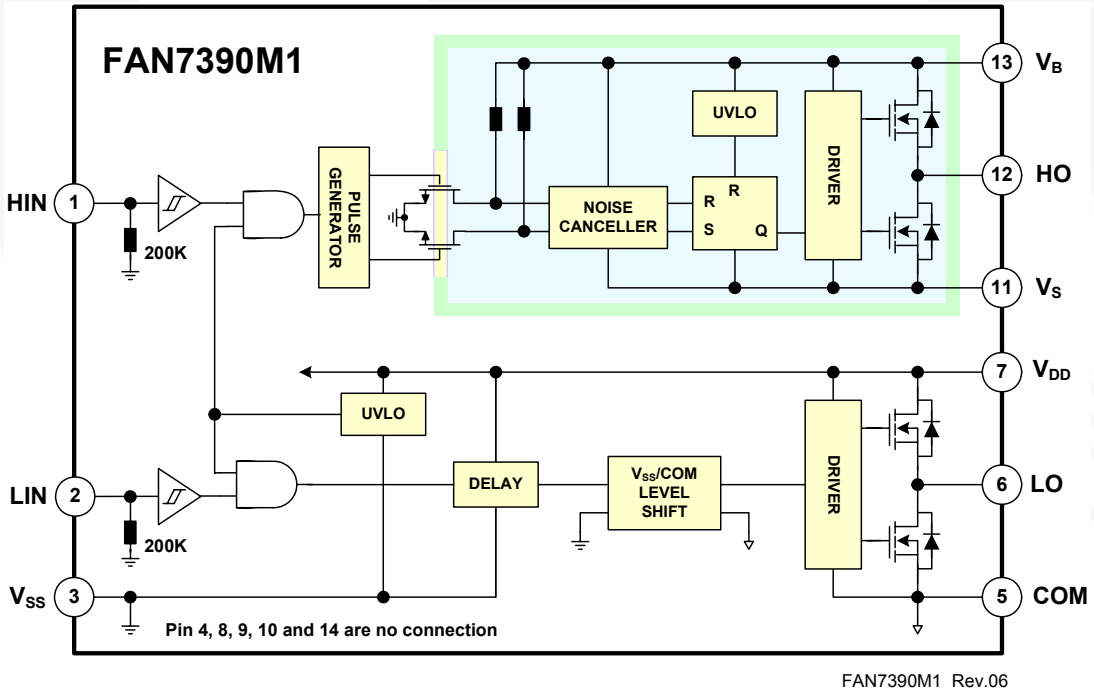

Figure 4. Functional Block Diagram (Referenced 14-SOIC)

Pin Configurations

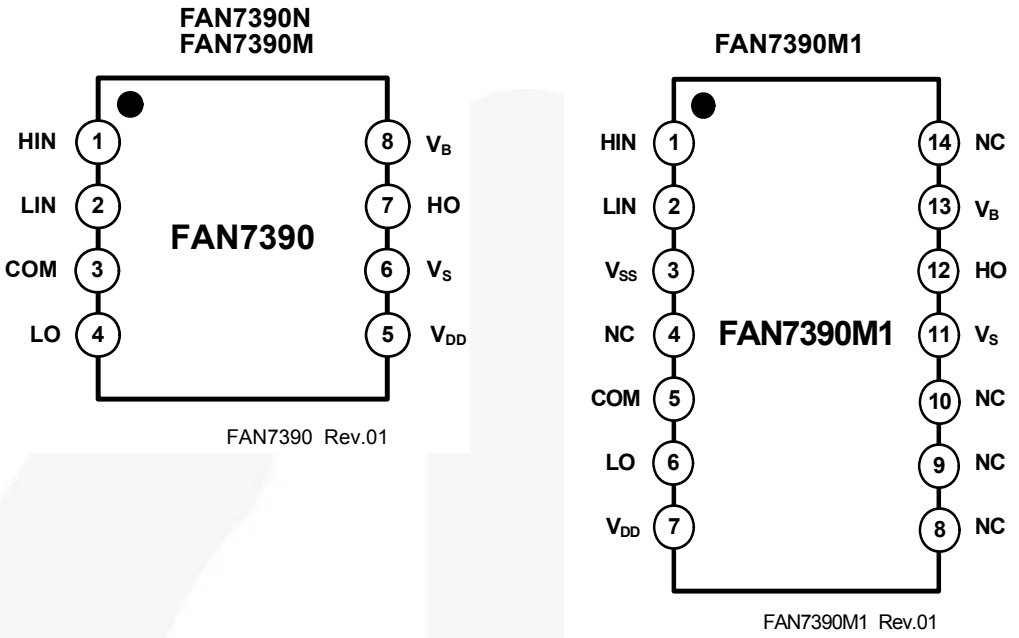

Figure 5. Pin Assignments (Top View)

Pin Definitions

8-Pin	14-Pin	Name	Description
1	1	HIN	Logic Input for High-Side Gate Driver Output
2	2	LIN	Logic Input for Low-Side Gate Driver Output
	3	V_{SS}	Logic Ground (FAN7390M1 only)
3	5	COM	Low-Side Driver Return
4	6	LO	Low-Side Driver Output
5	7	V_{DD}	Low-Side and Logic Part Supply Voltage
6	11	V_S	High-Voltage Floating Supply Return
7	12	HO	High-Side Driver Output
8	13	V_B	High-Side Floating Supply
	4, 8, 9, 10, 14	NC	No Connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-Side Floating Supply Offset Voltage	V_B-25.0	V_B+0.3	V
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_{HO}	High-Side Floating Output Voltage HO	V_S-0.3	V_B+0.3	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
V_{LO}	Low-Side Output Voltage LO	-0.3	V_{DD}+0.3	V
V_{IN}	Logic Input Voltage (HIN and LIN)	V_{SS}-0.3	V_{DD}+0.3	V
V_{SS}	Logic Ground (FAN7390M1 only)	V_{DD}-25	V_{DD}+0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate		50	V/ns
P_D(1, 2, 3)	Power Dissipation	8-DIP	1.25	W
		8-SOP	0.625	
		14-SOIC	1.0	
θ_{JA}	Thermal Resistance, Junction-to-Ambient	8-DIP	100	°C/W
		8-SOP	200	
		14-SOIC	110	
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature		+150	°C

Notes:

1. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+22	V
V_S	High-Side Floating Supply Offset Voltage	6-V_{DD}	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{DD}	Low-Side and Logic Supply Voltage	10	22	V
V_{LO}	Low-Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (HIN and LIN)	V_{SS}	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	°C

Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS})=15.0V, V_S=V_{SS}=COM, T_A=25°C, unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM and V_S is applicable to the respective output signals HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION (V_{DD} AND V_{BS})						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive-going Threshold		8.0	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative-going Threshold		7.4	8.3	9.0	
V_{DDUVH} V_{BSUVH}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage			0.5		
I_{LK}	Offset Supply Leakage Current	V_B=V_S=600V			50	µA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN}=0V or 5V		45	80	
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN}=0V or 5V		75	110	
I_{PBS}	Operating V_{BS} Supply Current	f_{IN}=20kHz, rms value		530	640	µA
I_{PDD}	Operating V_{DD} Supply Current	f_{IN}=20kHz, rms value		530	640	
LOGIC INPUT SECTION (HIN, LIN)						
V_{IH}	Logic "1" Input Voltage		2.5			V
V_{IL}	Logic "0" Input Voltage				1.2	
I_{IN+}	Logic "1" Input Bias Current	V_{IN}=5V		25	50	µA
I_{IN-}	Logic "0" Input Bias Current	V_{IN}=0V		1.0	2.0	
R_{IN}	Input Pull-down Resistance		100	200		KΩ
GATE DRIVER OUTPUT SECTION (HO, LO)						
V_{OH}	High-level Output Voltage, V_{BIAS}-V_O	No Load			1.0	V
V_{OL}	Low-level Output Voltage, V_O	No Load			35	mV
I_{O+}	Output High, Short-circuit Pulsed Current[4]	V_O=0V, V_{IN}=5V with PW<10µs	3.5	4.5		A
I_{O-}	Output Low, Short-circuit Pulsed Current[4]	V_O=15V, V_{IN}=0V with PW<10µs	3.5	4.5		
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V
V_{SS}-COM	V_{SS}-COM/COM-V_{SS} Voltage Educability		-7.0		7.0	V

Note:

4. This parameter guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS})=15.0V, V_S=V_{SS}=COM=0V, C_L=1000pF and T_A=25°C unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Propagation Delay	V_S=0V		140	200	ns
t_{off}	Turn-off Propagation Delay	V_S=0V		140	200	
MT	Delay Matching, HS & LS Turn-on/off			0	50	
t_r	Turn-on Rise Time			25	50	
t_f	Turn-off Fall Time			20	45	

Typical Characteristics

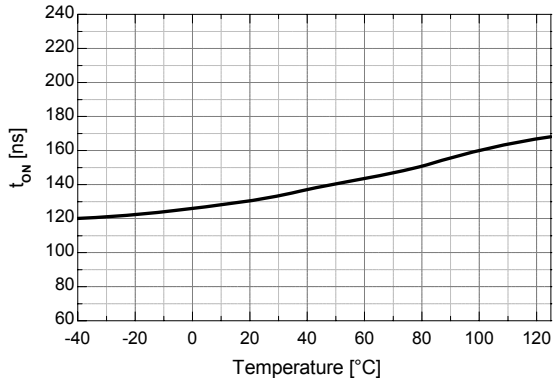

Figure 6. Turn-on Propagation Delay vs. Temperature

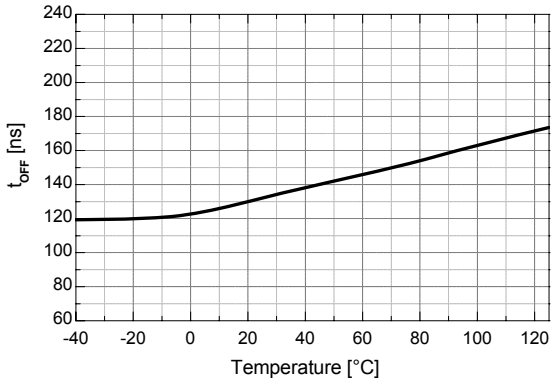

Figure 7. Turn-off Propagation Delay vs. Temperature

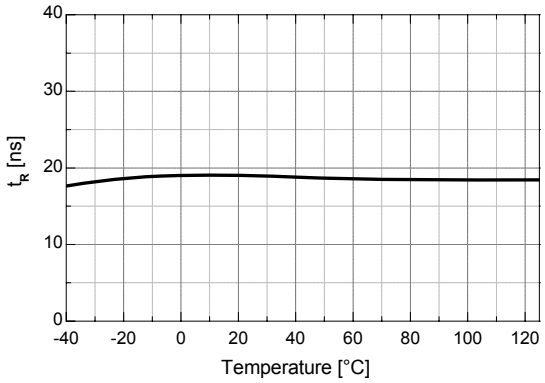

Figure 8. Turn-on Rise Time vs. Temperature

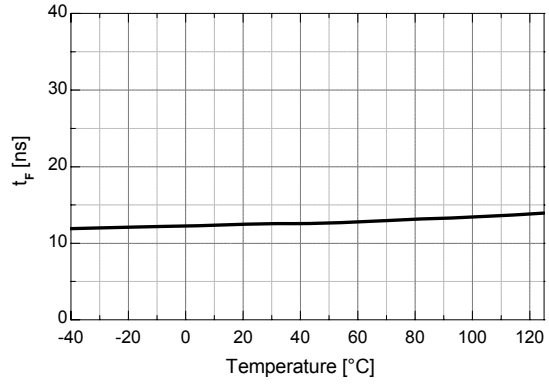

Figure 9. Turn-off Fall Time vs. Temperature

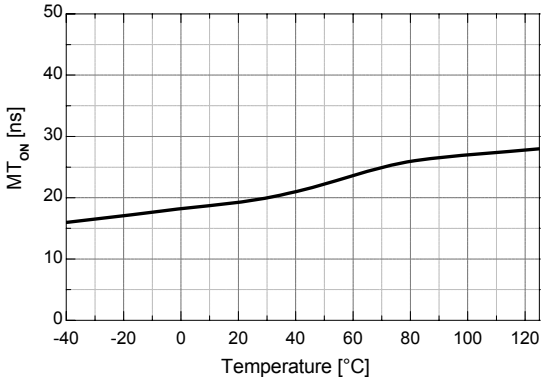

Figure 10. Turn-on Delay Matching vs. Temperature

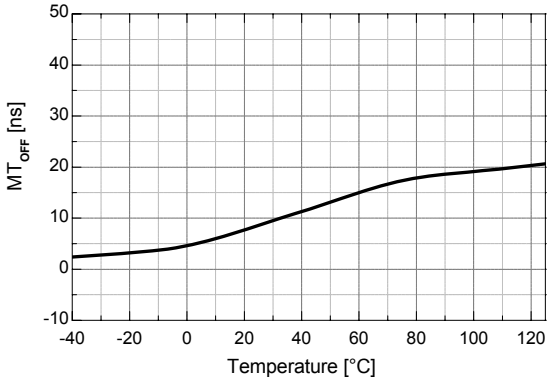

Figure 11. Turn-off Delay Matching vs. Temperature

Typical Characteristics (Continued)

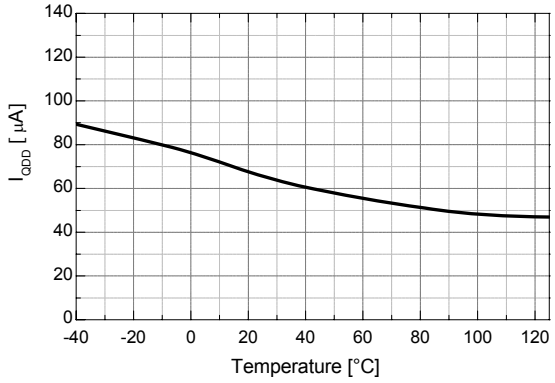

Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

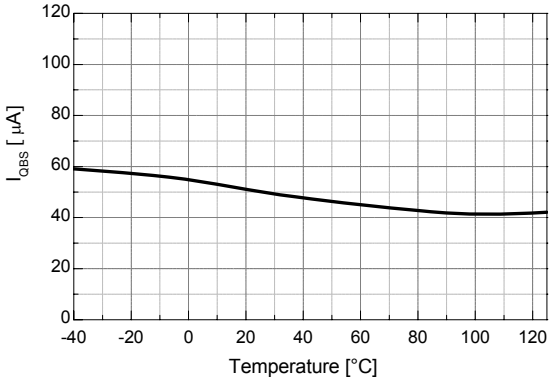

Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

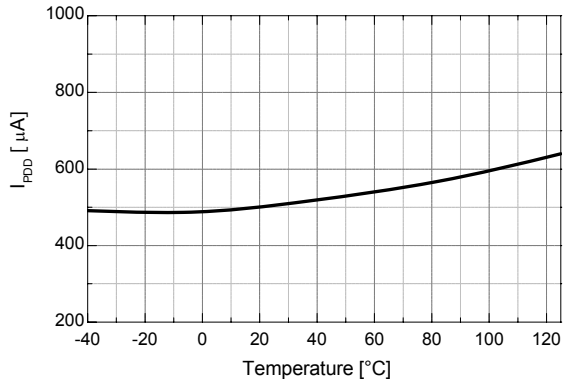

Figure 14. Operating V_{DD} Supply Current vs. Temperature

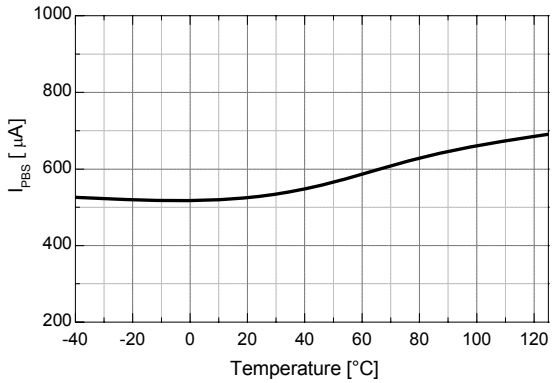

Figure 15. Operating V_{BS} Supply Current vs. Temperature.

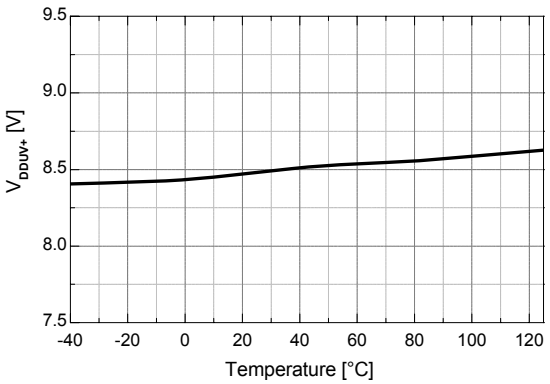

Figure 16. V_{DD} UVLO+ vs. Temperature

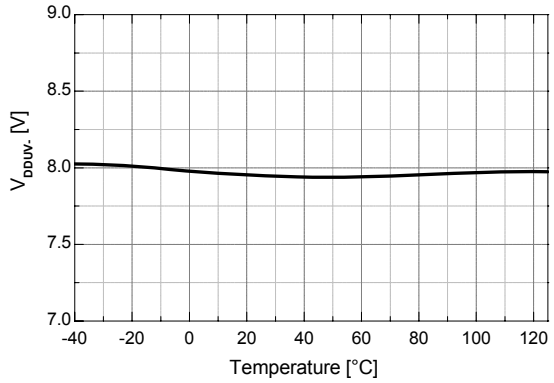

Figure 17. V_{DD} UVLO- vs. Temperature

Typical Characteristics (Continued)

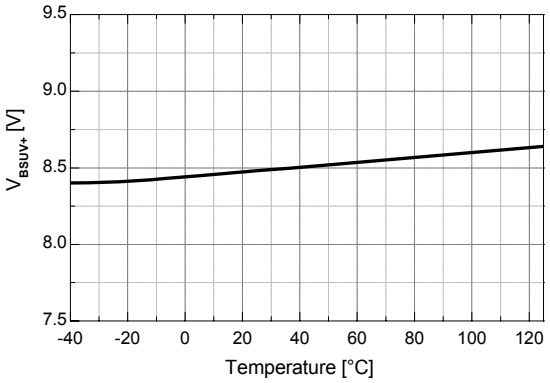

Figure 18. V_{BS} UVLO+ vs. Temperature

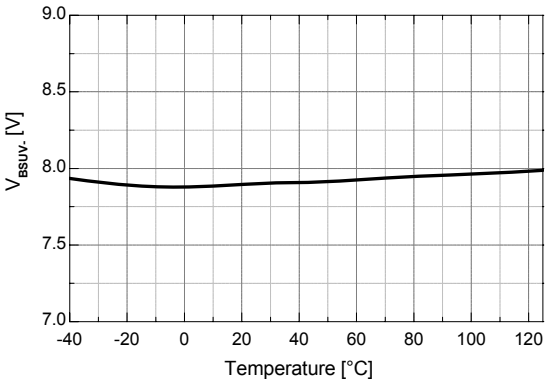

Figure 19. V_{BS} UVLO- vs. Temperature

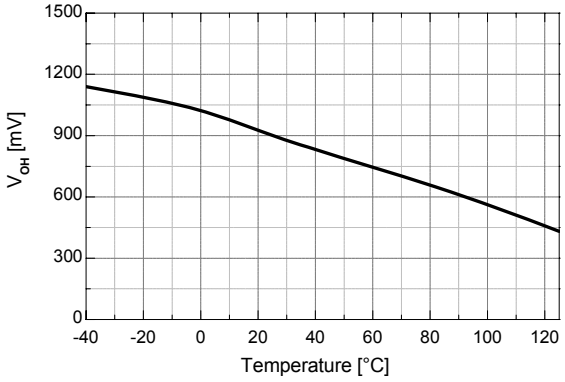

Figure 20. High-Level Output Voltage vs. Temperature

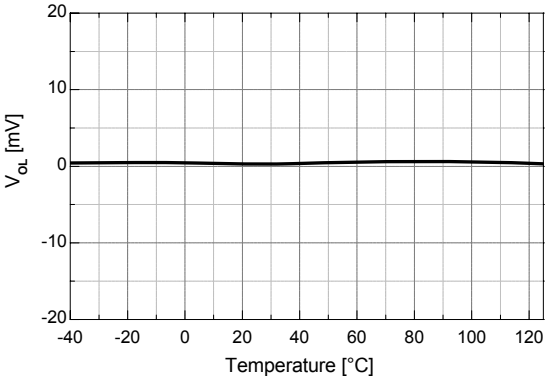

Figure 21. Low-Level Output Voltage vs. Temperature

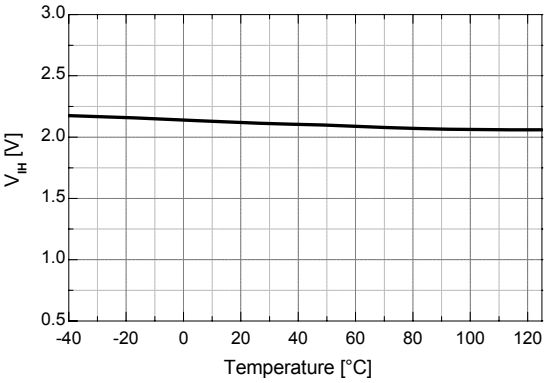

Figure 22. Logic High Input Voltage vs. Temperature

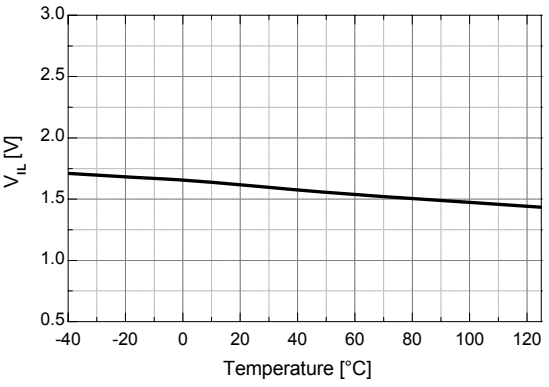

Figure 23. Low Input Voltage vs. Temperature

Typical Characteristics (Continued)

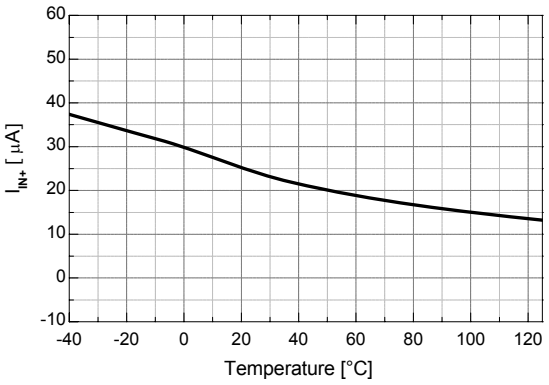

Figure 24. Logic Input High Bias Current vs. Temperature

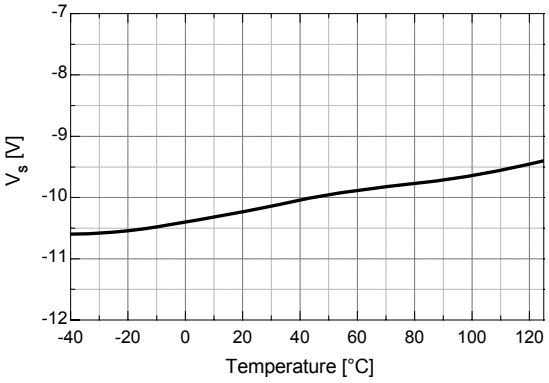

Figure 25. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

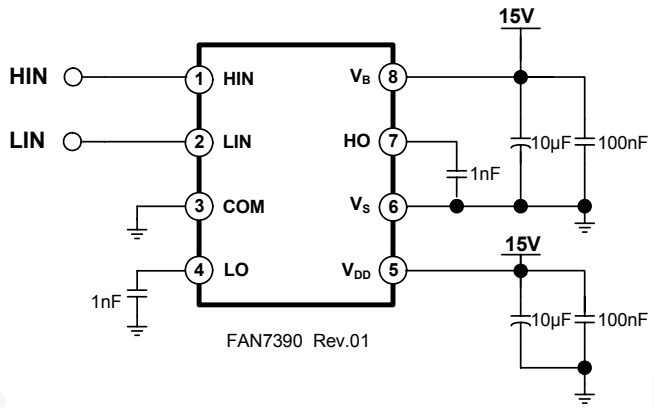

Figure 26. Switching Time Test Circuit (Referenced 8-SOP)

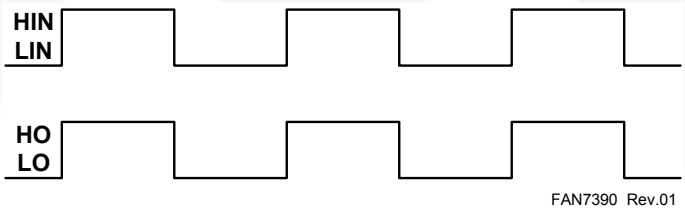

Figure 27. Input/Output Timing Diagram

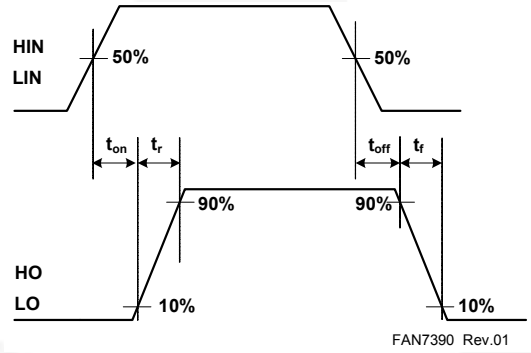

Figure 28. Switching Time Waveform Definitions

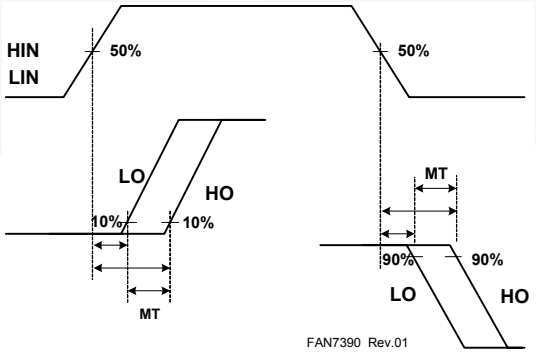

Figure 29. Delay Matching Waveform Definitions

Physical Dimensions

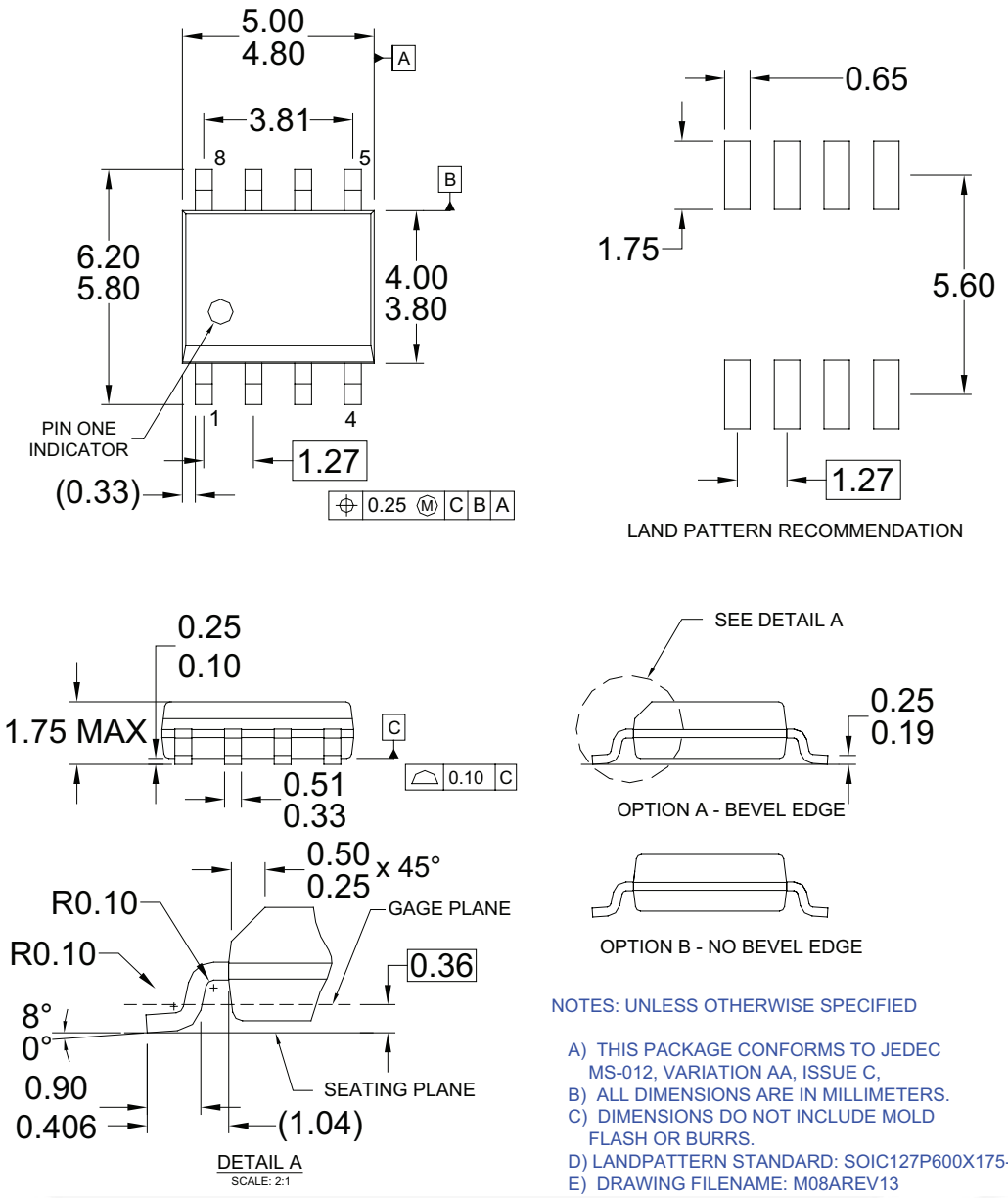

Figure 30. 8-Lead Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

Physical Dimensions (Continued)

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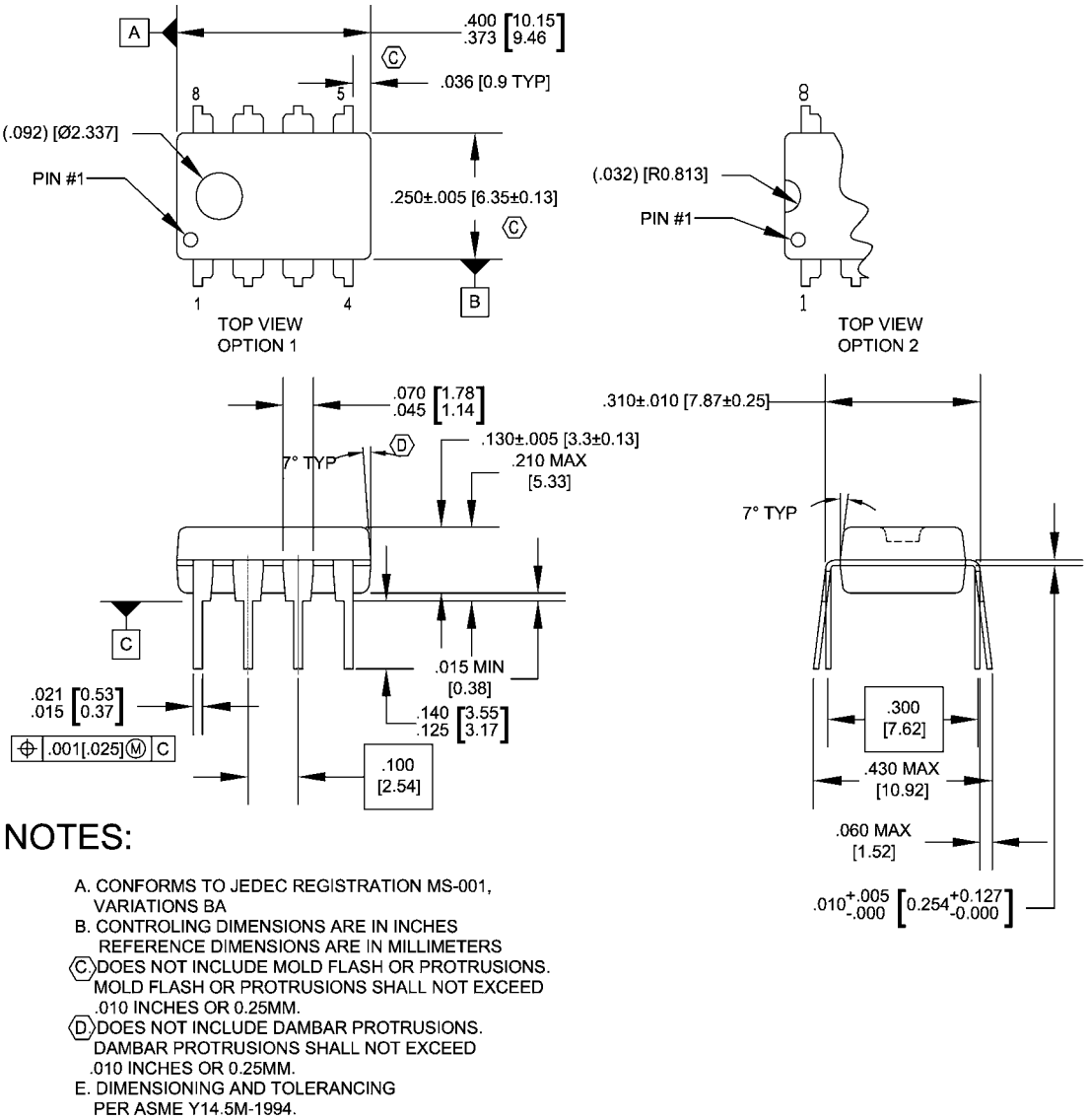

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
B. CONTROLING DIMENSIONS ARE IN INCHES
REFERENCE DIMENSIONS ARE IN MILLIMETERS
C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

Figure 31. 8-Lead Dual In-Line Package (DIP)

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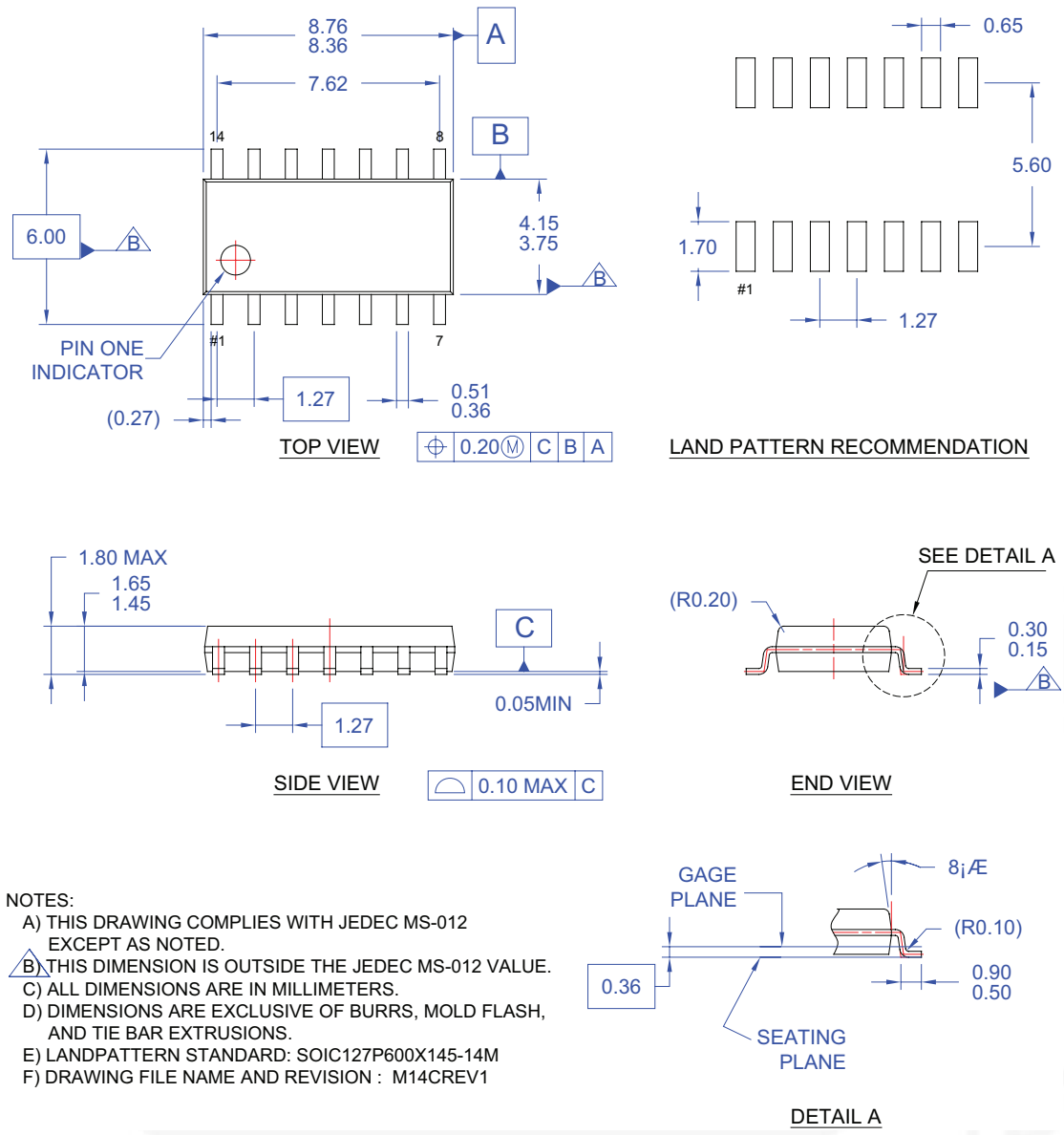
http://www.fairchildsemi.com/packaging/.

Physical Dimensions (Continued)



NOTES:

A) THIS DRAWING COMPLIES WITH JEDEC MS-012 EXCEPT AS NOTED.

B) THIS DIMENSION IS OUTSIDE THE JEDEC MS-012 VALUE.

C) ALL DIMENSIONS ARE IN MILLIMETERS.

D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

E) LANDPATTERN STANDARD: SOIC127P600X145-14M

F) DRAWING FILE NAME AND REVISION : M14CREV1

Figure 32. 14-Lead Small Outline Integrated Circuit Package (SOIC)

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