National Semiconductor

July 1998

54ABT573
Octal D-Type Latch with TRI-STATE® Outputs

General Description

The 'ABT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'ABT373 but has different pinouts.

Features

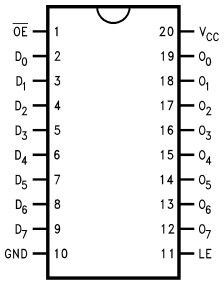
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ABT373
- TRI-STATE outputs for bus interfacing
- Output sink capability of 48 mA, source capability of 24 mA
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9321901

Ordering Code

Military	Package Number	Package Description
54ABT573J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT573W-QML	W20A	20-Lead Cerpack
54ABT573E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

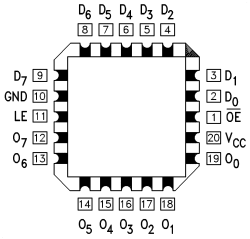
Connection Diagram

Pin Assignment for DIP and Cerpack



DS100219-1

Pin Assignment for LCC



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

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Functional Description

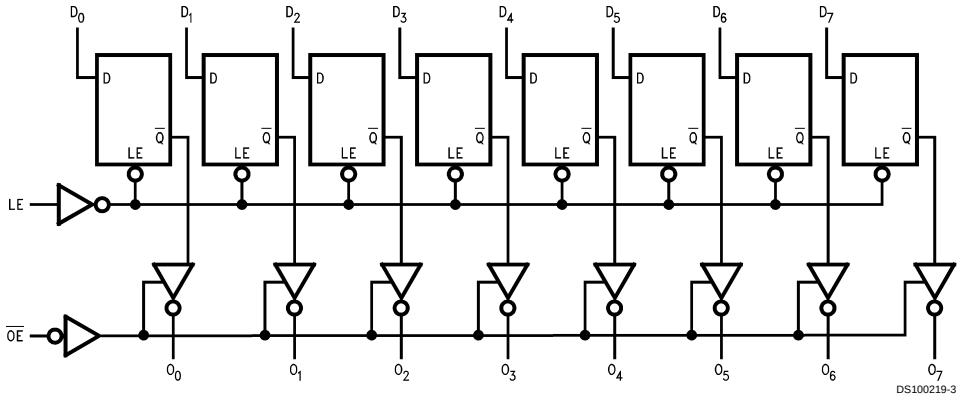
The 'ABT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT573			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current				7	μA	Max	V_{IN} = 7.0V
	Breakdown Test							
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}
								All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open
	(Note 4)				0.12	MHz		$\overline{OE}$ = GND, LE = V_{CC} (Note 3)
								One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.9	V	5.0	T_A = 25°C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-1.7	V	5.0	T_A = 25°C (Note 5)

Note 5: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH}	Propagation Delay	1.0	6.4	ns	*Figure 4*
t_{PHL}	D_n to O_n	1.5	6.7		
t_{PLH}	Propagation Delay	1.0	7.1	ns	*Figure 4*
t_{PHL}	LE to O_n	1.5	7.5		
t_{PZH}	Output Enable Time	0.8	6.5	ns	*Figure 6*
t_{PZL}		1.5	7.2		
t_{PHZ}	Output Disable Time	1.5	7.7	ns	*Figure 6*
t_{PLZ}	Time	1.0	7.0		

AC Operating Requirements

Symbol	Parameter	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_s(H)	Set Time, HIGH	2.5		ns	*Figure 7*
t_s(L)	or LOW D_n to LE	2.5			
t_h(H)	Hold Time, HIGH	2.5		ns	*Figure 7*
t_h(L)	or LOW D_n to LE	2.5			
t_w(H)	Pulse Width, LE HIGH	3.3		ns	*Figure 5*

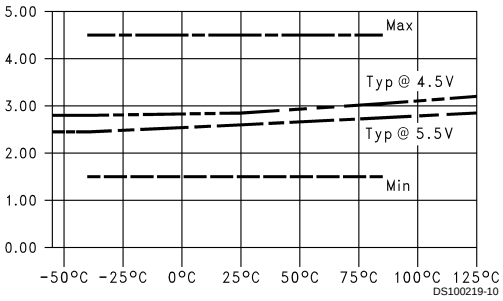
Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V
C_{OUT} (Note 6)	Output Capacitance	9	pF	V_{CC} = 5.0V

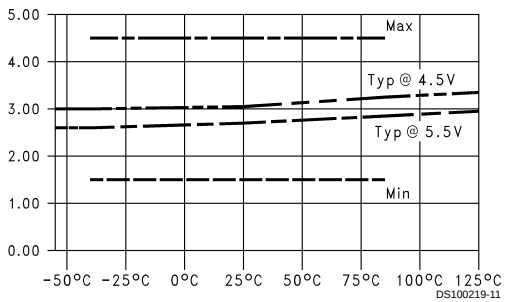
Note 6: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

Capacitance (Continued)

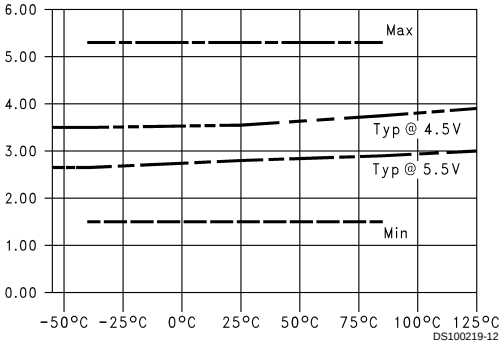
T_{PLH} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to Output



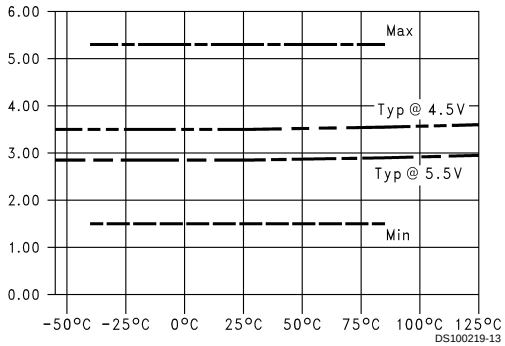
T_{PHL} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to Output



T_{PZH} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, OE to Output



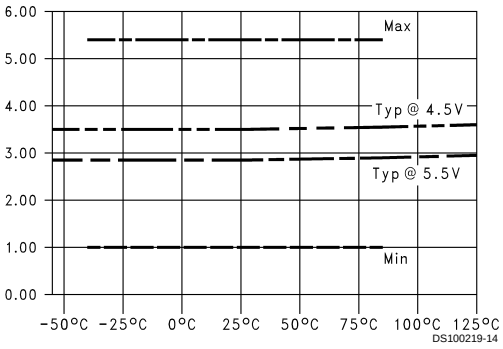
T_{PZL} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, OE to Output



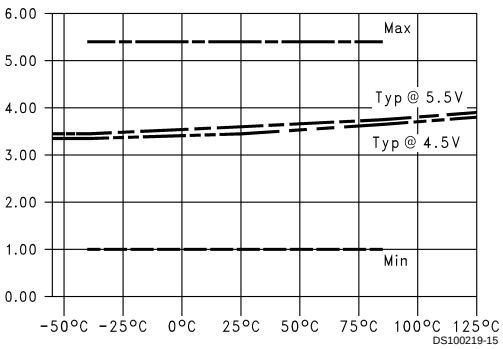
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

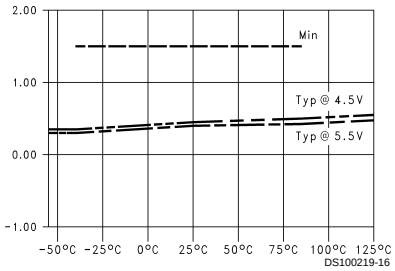
T_{PHZ} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, OE to Output



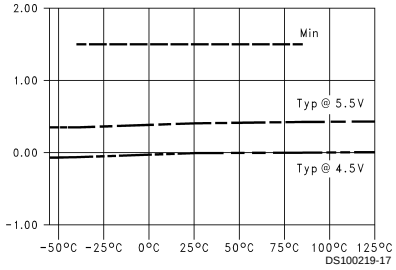
T_{PLZ} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, OE to Output



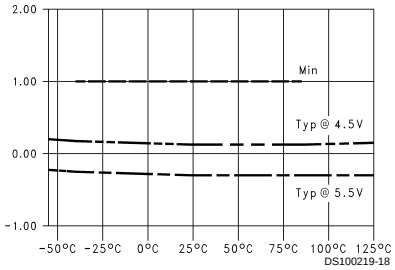
T_{SET} LOW vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to LE



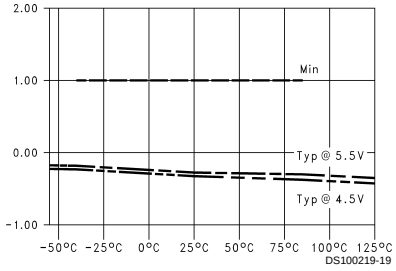
T_{SET} HIGH vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to LE



T_{HOLD} HIGH vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to LE



T_{HOLD} LOW vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, Data to LE



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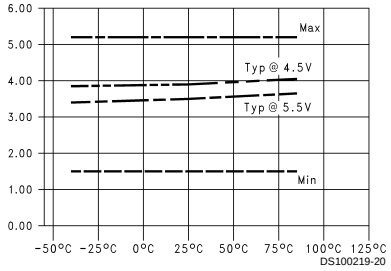
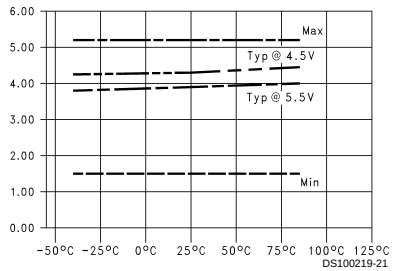
Capacitance (Continued)

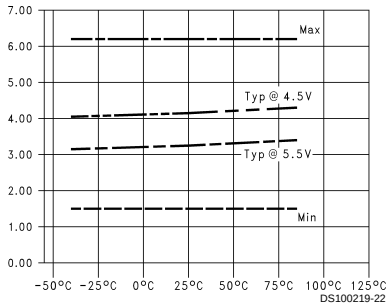
T_{PLH} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, Data to Output



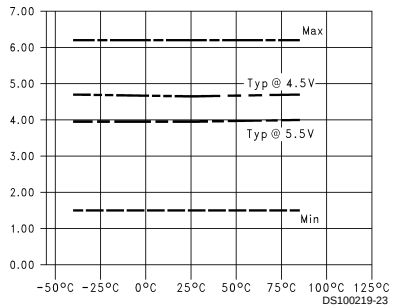
T_{PHL} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, Data to Output



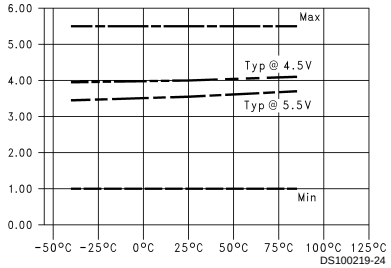
T_{PZH} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, OE to Output



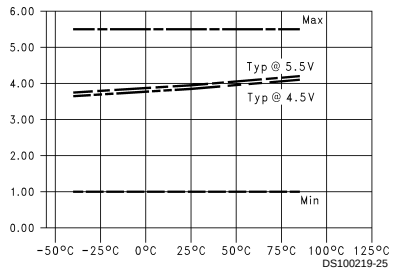
T_{PZL} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, OE to Output



T_{PHZ} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, OE to Output



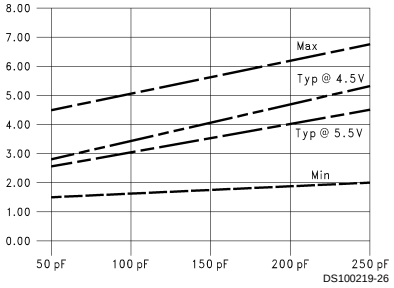
T_{PLZ} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, OE to Output



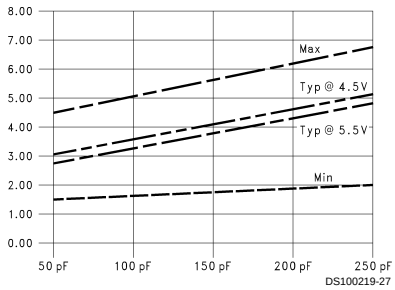
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

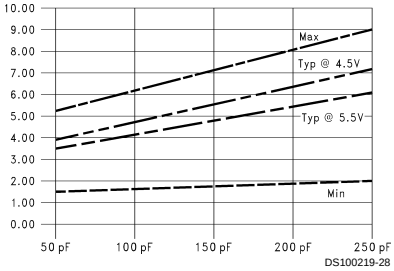
T_{PLH} vs Load Capacitance T_A = 25°C, 1 Output Switching, Data to Output



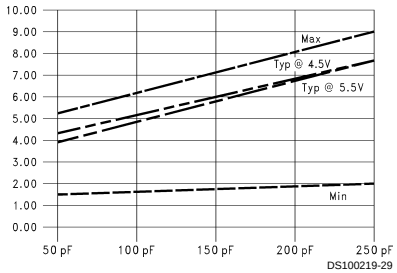
T_{PHL} vs Load Capacitance T_A = 25°C, 1 Output Switching, Data to Output



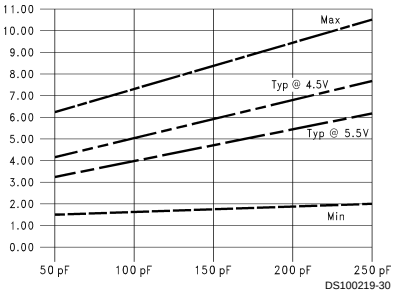
T_{PLH} vs Load Capacitance T_A = 25°C, 8 Outputs Switching, Data to Output



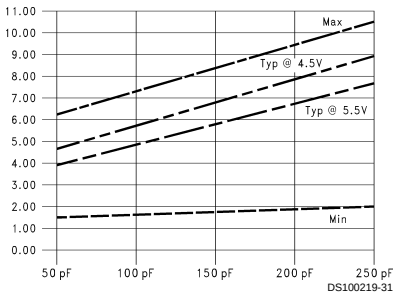
T_{PHL} vs Load Capacitance T_A = 25°C, 8 Outputs Switching, Data to Output



T_{PZH} vs Load Capacitance T_A = 25°C, 8 Outputs Switching, $\overline{OE}$ to Output



T_{PZL} vs Load Capacitance T_A = 25°C, 8 Outputs Switching, $\overline{OE}$ to Output



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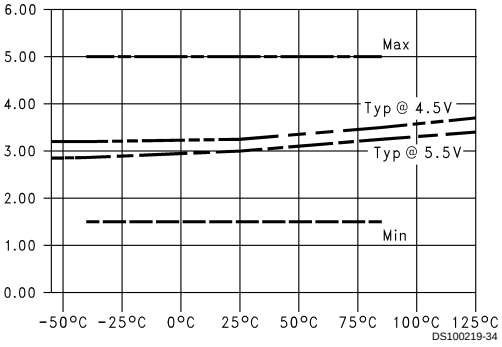
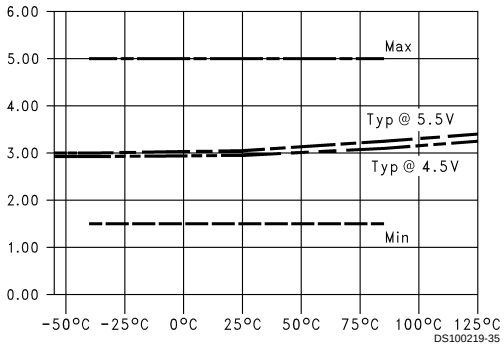
Capacitance (Continued)

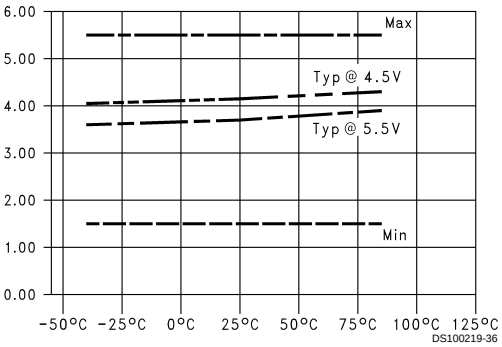
T_{PLH} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, LE to Output



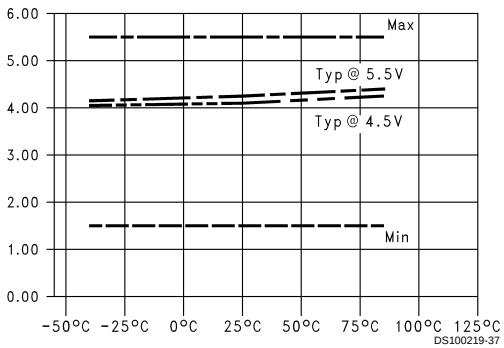
T_{PHL} vs Temperature (T_A), C_L = 50 pF, 1 Output Switching, LE to Output



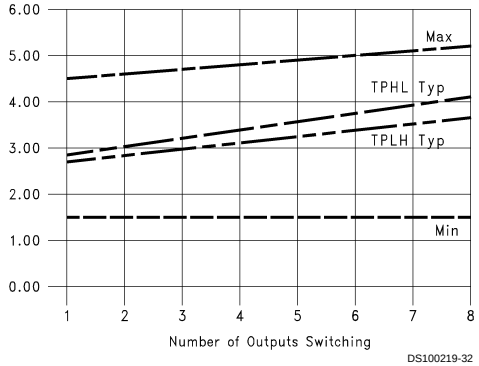
T_{PLH} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, LE to Output



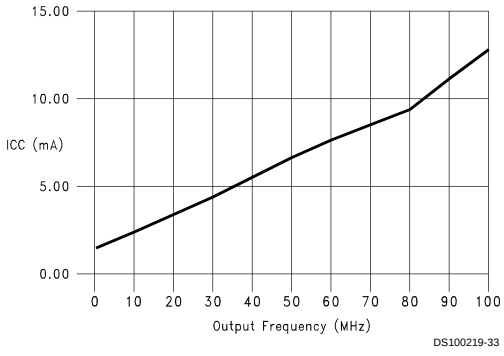
T_{PHL} vs Temperature (T_A), C_L = 50 pF, 8 Outputs Switching, LE to Output



T_{PLH} and T_{PHL} vs Number Outputs Switching, C_L = 50 pF, T_A = 25°C, V_{CC} = 5.0V, Outputs In Phase Data to Output



Typical I_{CC} vs Output Switching Frequency, C_L = 0 pF, V_{CC} = V_{IH} = 5.5V, LE = GND, 1 Output Switching at 50% Duty Cycle, Data to Output, Transparent Mode with Unused Data Inputs = V_{IH}



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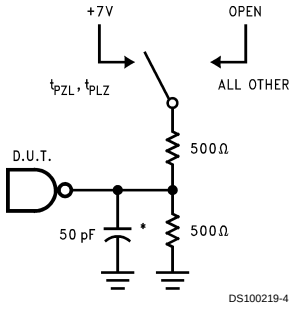
AC Loading



*Includes jig and probe capacitance

FIGURE 1. Test Load

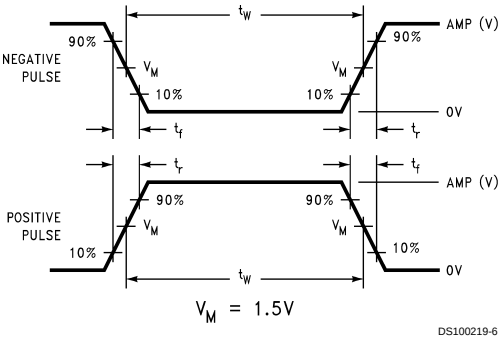


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

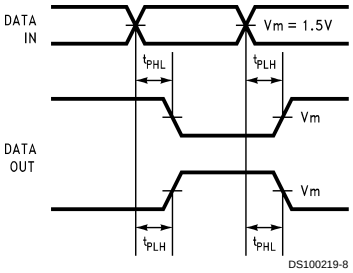


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

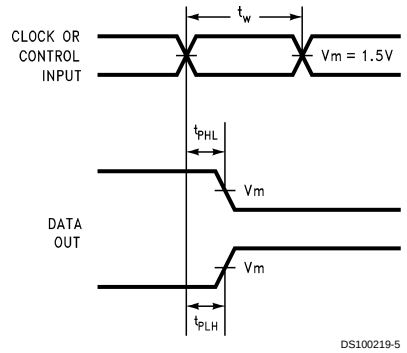


FIGURE 5. Propagation Delay, Pulse Width Waveforms

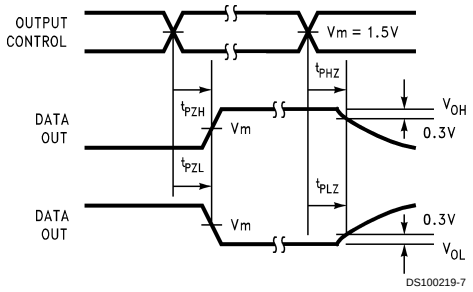


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

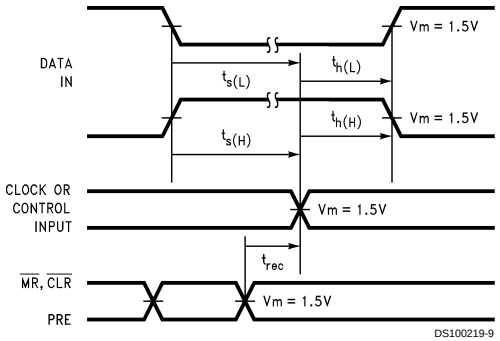
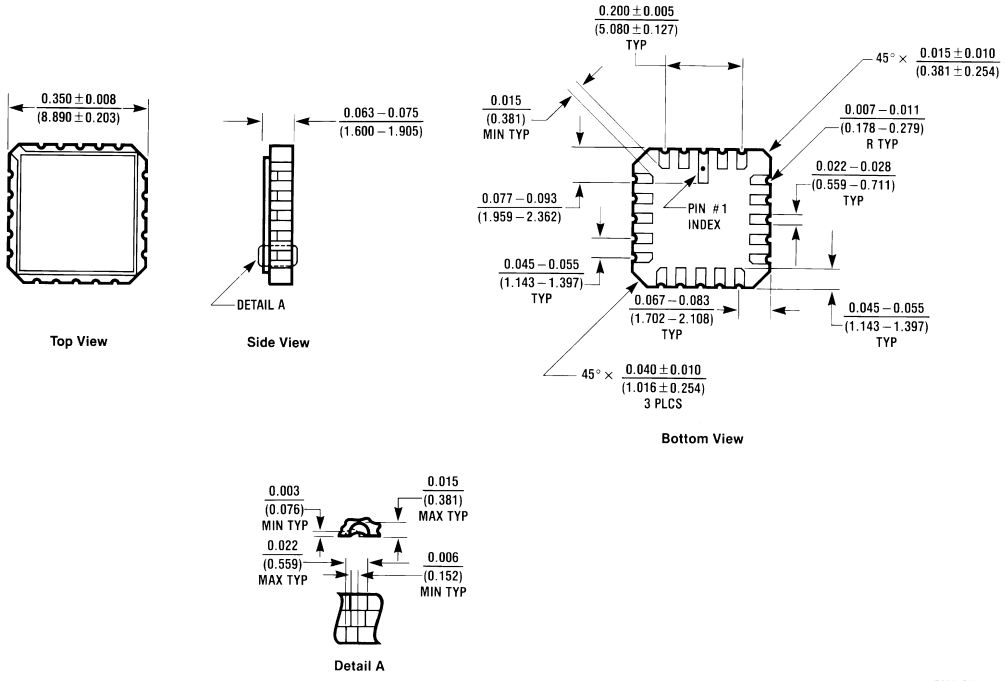
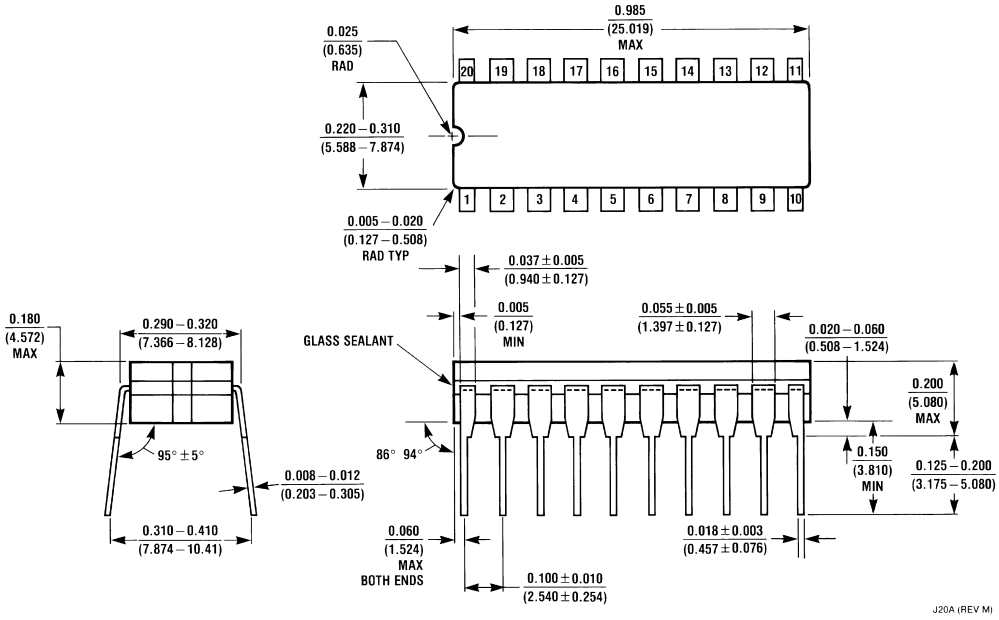


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

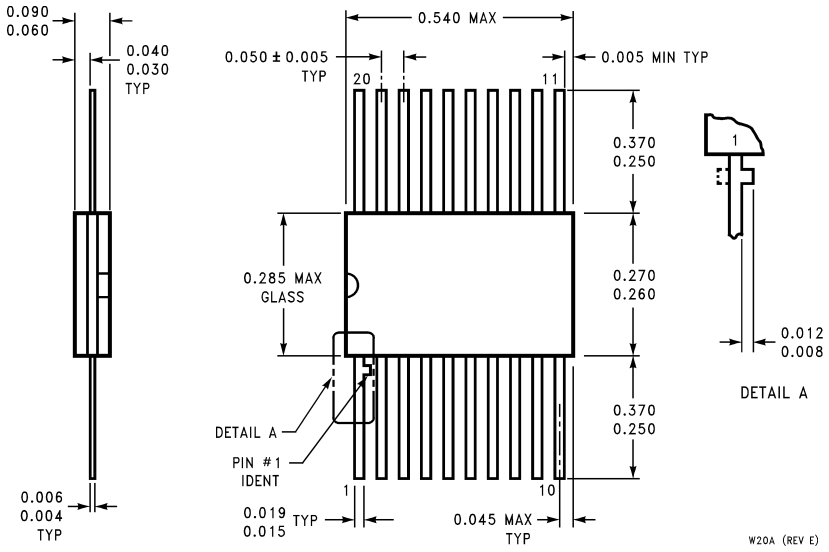


20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



20-Lead Ceramic Dual-In-Line
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpack
NS Package Number W20A

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