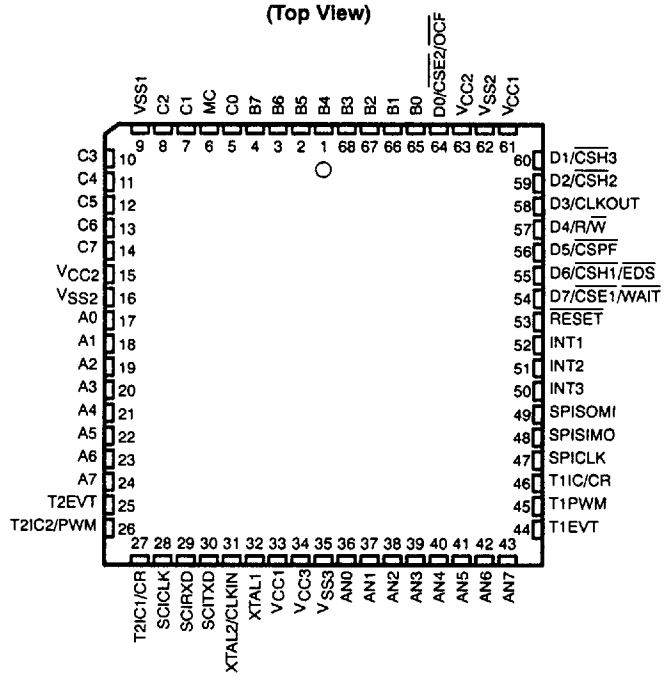
TMS370Cx5x
8-BIT MICROCONTROLLERS

SPNS010B — DECEMBER 1986 — REVISED JULY 1991

- CMOS/EEPROM/EPROM Technology on a Single Device
  - — Mask ROM Devices for High-Volume Production
  - — One Time Programmable (OTP) Devices for Low-Volume Production
  - — EPROM Devices for Prototyping Purposes
- Flexible Operation Features
  - — Power-Reduction STANDBY and HALT Modes
  - — Commercial and Industrial Temperature Ranges
  - — Input Clock Frequency 2 MHz to 20 MHz
  - — Voltage (V_{CC}): 5 V ± 10%
- System Memory Configurations
  - — On-Chip Program Memory Versions
    - – ROM: 4K-, 8K-, and 16K-Bytes
    - – EPROM: 16K-Bytes
    - – ROMless
  - — Data EEPROM: 256-Bytes or 512-Bytes
  - — Static RAM: 256-Bytes or 512-Bytes
  - — External Memory/Peripheral WAIT States
  - — Precoded External Chip Select Outputs in Microcomputer Mode
    - – Allows 112K-Bytes External Addressable Memory
    - – No Logic Needed for External Memory Addressing
- Eight-Channel 8-Bit A/D Converter
- Two 16-Bit General-Purpose Timers
  - — Software Configurable as Two 16-Bit Event Counters, or Two 16-Bit Pulse Accumulators, or Three 16-Bit Input Capture Functions, or Four Compare Registers, or Two Self-Contained PWM Functions
  - — Software Programmable Input Polarity
  - — One Timer Has an 8-Bit Prescaler, Providing a 24-Bit Realtime Timer
- On-Chip 24-Bit Watchdog Timer
- Serial Communications Interface (SCI)
  - — Asynchronous and Isosynchronous Modes
  - — Full Duplex, Double-Buffered Rx and Tx
  - — Two Multiprocessor Communications Formats
- Plastic and Ceramic 68-Pin Leaded Chip Carrier Packages

FN/FZ Package
(Top View)



- Serial Peripheral Interface (SPI)
  - — Variable-Length High-Speed Shift Register
  - — Synchronous Master/Slave Operation
- Flexible Interrupt Handling
  - — Two S/W Programmable Interrupt Levels
  - — Global and Individual Interrupt Masking
  - — Programmable Rising or Falling Edge Detect
- 55 CMOS/TTL Compatible I/O Pins
  - — All Peripheral Function Pins Software Configurable for Digital I/O
  - — 46 Bidirectional, 9 Input Pins
- TMS370 Series Compatibility
  - — Register-to-Register Architecture
  - — 256 General-Purpose Registers
  - — Fourteen Powerful Addressing Modes
- PC-Based Workstation Development Support Emphasizes Productivity, Featuring:
  - — C Compiler Support
  - — Realtime In-Circuit Emulation
  - — Symbolic Debug
  - — Extensive Breakpoint/Trace Capability
  - — Software Performance Analysis
  - — Multi-Window User Interface
  - — EEPROM/EPROM Programming

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TMS370Cx5x
8-BIT MICROCONTROLLERS

T-49-19-01

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description

TMS370Cx5x family of single-chip 8-bit microcontrollers provides cost-effective realtime system control through VLSI integration of advanced peripheral function modules and various on-chip memory configurations. The TMS370Cx5x family presently consists of eleven devices, which can be grouped into three main sub-families: the TMS370Cx50, the TMS370Cx52, and the TMS370Cx56.

Unless otherwise noted, the following terms are used to refer to the individual devices described in this data sheet:

TMS370Cx50 refers to the TMS370C050, TMS370C150, TMS370C250, and TMS370C350 devices.

TMS370Cx52 refers to the TMS370C052 and TMS370C352 devices.

TMS370Cx56 refers to the TMS370C056, TMS370C156, TMS370C256, TMS370C356, and TMS370C756 devices.

TMS370Cx5x refers to the TMS370Cx50, TMS370Cx52, and TMS370Cx56 subfamilies.

The TMS370Cx5x family is implemented using high-performance silicon-gate CMOS technology. The low operating power, wide operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx5x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, and telecommunications.

The on-chip memory configurations of the TMS370Cx5x family include various amounts of static RAM, data EEPROM, and program memory (ROM or EPROM). TMS370Cx5x devices with mask ROM program memory are presently available in sizes ranging form 4K-bytes to 16K-bytes. A device with EPROM program memory is available with 16K-bytes. Devices are also available as ROMless microprocessors. The following table provides an overview of the various memory configurations and operating modes of the TMS370Cx5x devices.

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		OPERATING MODES†		PACKAGE
	ROM	EPROM	RAM	EEPROM	µC	µP	
TMS370CX50: TMS370C050, TMS370C150, TMS370C250 AND TMS370C350							
TMS370C050	4K	–	256	256	√	√	FN - PLCC
TMS370C150	–	–	256	–	–	√	FN - PLCC
TMS370C250	–	–	256	256	–	√	FN - PLCC
TMS370C350	4K	–	256	–	√	√	FN - PLCC
TMS370Cx52: TMS370C052, AND TMS370C352							
TMS370C052	8K	–	256	256	√	√	FN - PLCC
TMS370C352	8K	–	256	–	√	√	FN - PLCC
TMS370Cx56: TMS370C056, TMS370C156, TMS370C256, TMS370C356 AND TMS370C756							
TMS370C056	16K	–	512	512	√	√	FN - PLCC
TMS370C156	–	–	512	–	–	√	FN - PLCC
TMS370C256	–	–	512	512	–	√	FN - PLCC
TMS370C356	16K	–	512	–	√	√	FN - PLCC
TMS370C756	–	16K	512	512	√	√	FN - PLCC
EPROM DEVICE: SE370C756							
SE370C756‡	–	16K	512	512	√	√	FZ - CLCC

† µC – Microcomputer mode; µP – Microprocessor Mode

‡ System evaluators and development tools are for use only in the prototype environment and their reliability has not been characterized.

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All TMS370Cx5x devices contain a minimum of the following on-chip peripheral modules:

- 256 bytes RAM (usable as registers)
- 8-channel, 8-bit Analog-to-Digital converter (A/D)
- Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Two 24-bit general-purpose timers, one of which can be used as a Watchdog timer
- One 16-bit general-purpose timer

The TMS370Cx5x provides two power reduction modes (STANDBY and HALT) for applications where low power consumption is critical. Both modes stop all CPU activity (i.e., no instructions are executed). In the STANDBY mode the internal oscillator, the general purpose timer, and the SCI receiver start bit detection remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both powerdown modes.

The TMS370Cx5x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (e.g., ADD r24, r47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx5x family is fully instruction-set-compatible, allowing easy transition between members.

The TMS370Cx5x family offers an 8-channel Analog-to-Digital converter with 8-bit accuracy. The 33-μs conversion time at 20 MHz and the variable sample period, combined with selectable positive reference voltage sources, turn real-world analog signals into digital data.

The SPI and the two operational modes of the SCI give three methods of serial communications. The SCI allows standard RS-232-C communications between other common data transmission equipment, while the SPI gives high speed communications between simpler shift register type devices, such as display drivers, A/D converter, PLL, I/O expansion, or other microcontrollers in the system.

For large memory applications, the TMS370Cx5x family provides an external bus with non-multiplexed address and data. Precoded memory chip select outputs can be enabled, which allow minimum-chip-count system implementations. Wait-state support facilitates performance matching between the CPU and external memory and the peripherals. All pins associated with memory expansion interface are individually software configurable for general-purpose digital input/output pins when operating in the microcomputer mode.

Two versions of the TMS370Cx5x family that have 16K EPROM program memory with a superset of the memory and peripherals of all the other family members are SE370C756FZ and TMS370C756FN.

The SE370C756FZ is available in a 68-pin, windowed ceramic package (FZ suffix) that allows memory reprogramming during the development design prototyping phase. This achieves quick updates to breadboards and prototype systems using socketed FFE devices while iterating initial designs.

The TMS370C756FN is available in a 68-pin plastic package (FN suffix) and is one time programmable (OTP). This is an effective microcomputer to use for immediate production updates for other members of the TMS370Cx5x family or for low-volume production runs that cannot satisfy minimum volume or cycle time requirement for the lower cost mask ROM devices.

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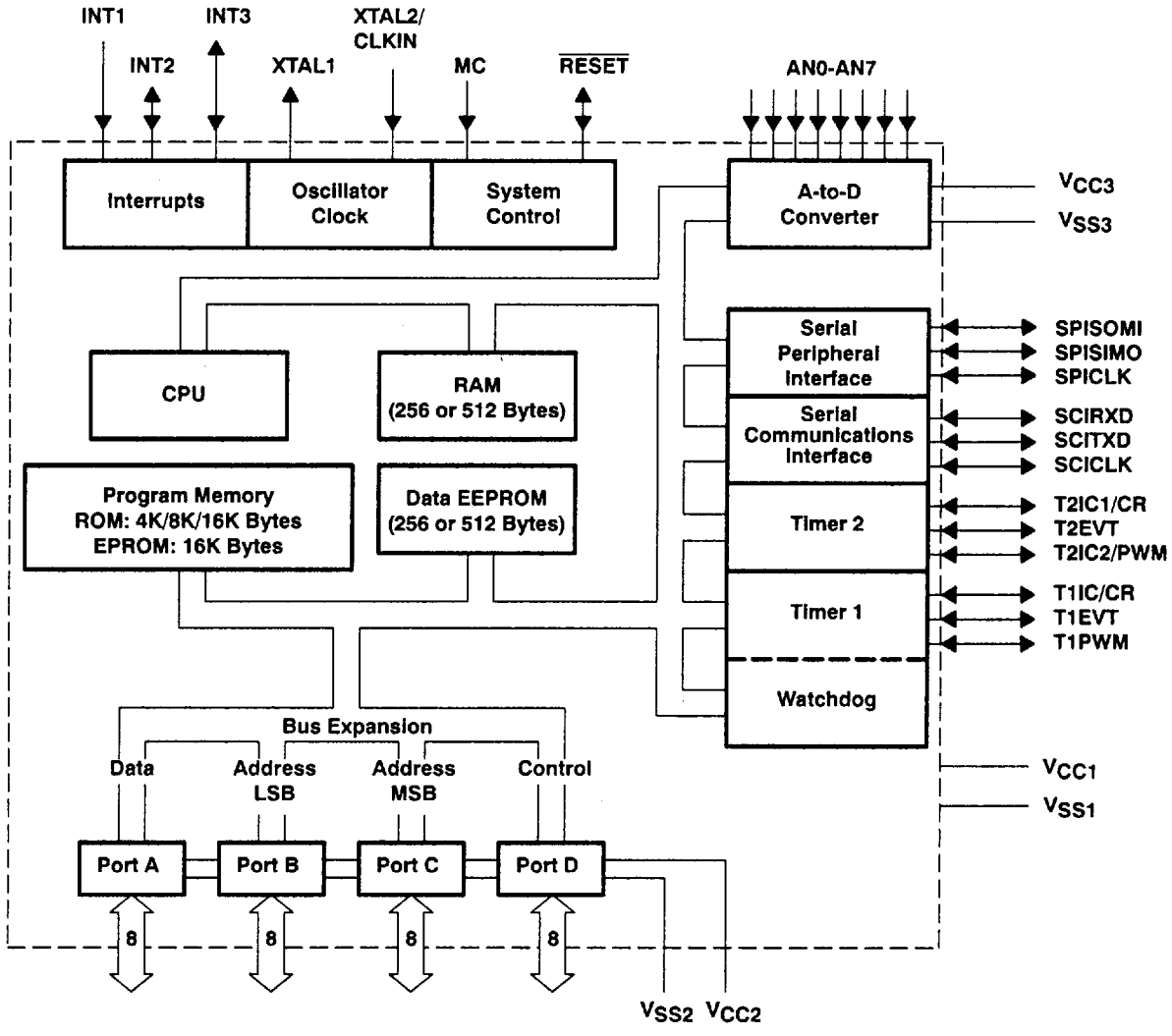
The TMS370Cx5x family provides a very economical, efficient solution to realtime control applications. The TMS370 family eXtended Development System (XDS) solves the challenge of efficiently developing the software and hardware required to design the TMS370Cx5x into an ever-increasing number of complex applications. The application source code can be written in assembly language or in C. The TMS370 family XDS communicates via standard RS-232-C interface with an existing personal computer to form a PC-DOS hosted workstation. This allows use of the PC's editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that the system designer can begin developing software with minimum training. Precise realtime in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reducing time-to-market cycle.

The TMS370Cx5x family mask ROM and EPROM, together with the TMS370 family XDS for applications development, the SE370C756 EPROM devices, and comprehensive product documentation and customer support provide a complete solution to the needs of the system designer.

functional block diagram



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TERMINAL FUNCTIONS

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PIN			I/O	DESCRIPTION
NAME	ALTERNATE FUNCTION	NO.		
A0	DATA0 (LSB)	17	I/O	Single-Chip Mode: Port A is a general purpose bidirectional I/O port.
A1	DATA1	18	I/O	
A2	DATA2	19	I/O	Expansion Mode: Port A may be individually programmed as the external bidirectional data bus (DATA0–DATA7).
A3	DATA3	20	I/O	
A4	DATA4	21	I/O	
A5	DATA5	22	I/O	
A6	DATA6	23	I/O	
A7	DATA7 (MSB)	24	I/O	
B0	ADD0	65	I/O	Single-Chip Mode: Port B is a general purpose bidirectional I/O port.
B1	ADD1	66	I/O	
B2	ADD2	67	I/O	Expansion Mode: Port B may be individually programmed as the low order address output bus (ADD0–ADD7).
B3	ADD3	68	I/O	
B4	ADD4	1	I/O	
B5	ADD5	2	I/O	
B6	ADD6	3	I/O	
B7	ADD7	4	I/O	
C0	ADD8	5	I/O	Single-Chip Mode: Port C is a general purpose bidirectional I/O port.
C1	ADD9	7	I/O	
C2	ADD10	8	I/O	Expansion Mode: Port C may be individually programmed as the high order address output bus (ADD8–ADD15).
C3	ADD11	10	I/O	
C4	ADD12	11	I/O	
C5	ADD13	12	I/O	
C6	ADD14	13	I/O	
C7	ADD15	14	I/O	

TERMINAL FUNCTIONS (continued)

PIN NAME	PIN ALTERNATE FUNCTION		PIN NO.	I/O	DESCRIPTION
	FUNCTION A	FUNCTION B			Single-Chip Mode: Port D is a general purpose bidirectional I/O port. Each of the Port D pins can be individually configured as either a general purpose I/O pin, a primary memory control signal (Function A), or a secondary memory control signal (Function B). All chip selects are independent and can be used for memory bank switching.
D0	$\overline{CSE2}$	$\overline{OCF}$	64	I/O	I/O Pin, *or* Function A: Chip Select Eighth output 2 goes low during memory accesses to 2000h–3FFFh, *or* Function B: Opcode fetch goes low during the opcode fetch memory cycle.
D1	$\overline{CSH3}$		60	I/O	I/O Pin, *or* Function A: Chip Select Half output 3 goes low during memory accesses to 8000h–FFFFh.
D2	$\overline{CSH2}$		59	I/O	I/O Pin, *or* Function A: Chip Select Half output 2 goes low during memory accesses to 8000h–FFFFh.
D3	CLKOUT	CLKOUT	58	I/O	I/O Pin, *or* Functions A & B: Internal clock signal is 1/4 XTAL2/CLKIN frequency.
D4	R/$\overline{W}$	R/$\overline{W}$	57	I/O	I/O Pin, *or* Function A & B: Read/Write output pin.
D5	$\overline{CSPF}$		56	I/O	I/O Pin, *or* Function A: Chip Select Peripheral output for peripheral file; goes low during memory accesses to 10C0h–10FFh.
D6	$\overline{CSH1}$	$\overline{EDS}$	55	I/O	I/O Pin, *or* Function A: Chip Select Half output 1 goes low during memory accesses to 8000h–FFFFh, *or* Function B: External Data Strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects.
D7	$\overline{CSE1}$	$\overline{WAIT}$	54	I/O	I/O Pin, *or* Function A: Chip Select Eighth output 1 goes low during memory accesses to 2000h–3FFFh, *or* Function B: Wait input pin extends bus signals.
INT1	INTIN		52	I	External interrupt (non-maskable or maskable)/General purpose input pin.
INT2	INTIO1		51	I/O	External maskable interrupt input/General purpose bidirectional pin.
INT3	INTIO2		50	I/O	External maskable interrupt input/General purpose bidirectional pin.
T1IC/CR	T1IO1		46	I/O	Timer 1 input Capture/Counter Reset input pin/General purpose bidirectional pin.
T1PWM	T1IO2		45	I/O	Timer 1 PWM output pin/General Purpose bidirectional pin.
T1EVT	T1IO3		44	I/O	Timer 1 External Event input pin/General purpose bidirectional pin.
T2IC1/CR	T2IO1		27	I/O	Timer 2 input Capture 1/Counter Reset input pin/General purpose bidirectional pin.
T2IC2/PWM	T2IO2		26	I/O	Timer 2 input Capture 2 input pin/PWM output pin/General purpose bidirectional pin.
T2EVT	T2IO3		25	I/O	Timer 2 External Event input pin/General purpose bidirectional pin.

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TERMINAL FUNCTIONS (continued)

PIN			I/O	DESCRIPTION
NAME	ALTERNATE FUNCTION	NO.		
SPISOMI	SPIIO1	49	I/O	SPI Slave Output pin, Master Input pin/General purpose bidirectional pin.
SPISIMO	SPIIO2	48	I/O	SPI Slave Input pin, Master Output pin/General purpose bidirectional pin.
SPICLK	SPIIO3	47	I/O	SPI bidirectional Serial Clock pin/General purpose bidirectional pin.
SCITXD	SCIIO1	30	I/O	SCI Transmit Data output pin/General purpose bidirectional pin.
SCIRXD	SCIIO2	29	I/O	SCI Receive Data input pin/General purpose bidirectional pin.
SCICLK	SCIIO3	28	I/O	SCI bidirectional Serial Clock pin/General purpose bidirectional pin.
AN0	E0	36	I	A/D analog input (AN0 – AN7) or positive reference pins (AN1 – AN7).
AN1	E1	37	I	
AN2	E2	38	I	Port E may be individually programmed as general purpose input pins if not used as A/D converter analog input or positive reference input..
AN3	E3	39	I	
AN4	E4	40	I	
AN5	E5	41	I	
AN6	E6	42	I	
AN7	E7	43	I	
V_{CC3}		34		A/D converter positive supply voltage and optional positive reference input pin.
V_{SS3}		35		A/D converter ground supply and low reference input pin.
$\overline{RESET}$		53	I/O	System reset bidirectional pin. As input it initializes microcontroller, as open drain output it indicates an internal failure was detected by the Watchdog or Oscillator Fault circuit.
MC		6	I	Microprocessor/Microcomputer mode control input pin, also enables EEPROM Write Protection Override (WPO) mode. For devices with EPROM, this pin is used for V_{PP} external supply for EPROM programming.
XTAL2/CLKIN		31	I	Internal oscillator crystal input/External clock source input.
XTAL1		32	O	Internal oscillator output for crystal.
V_{CC1}		33,61		Positive supply voltage for digital logic.
V_{CC2}		15,63		Positive supply voltage for digital I/O pins.
V_{SS1}		9		Ground reference for digital logic.
V_{SS2}		16,62		Ground reference for digital I/O pins.

NOTE 1: Each pin associated with the Interrupt, Timer 1, Timer 2, SPI, and SCI functional blocks may be individually programmed as a general purpose bidirectional pin if it is not used for its primary block function.

operating modes

The TMS370Cx5x has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before the $\overline{\text{RESET}}$ pin goes inactive. The two memory configurations are then selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, expanded microcomputer, microprocessor, and microprocessor with internal program memory.

In the **microcomputer single chip mode**, the TMS370Cx5x functions as a self-contained microcomputer with all memory and peripherals on chip, increasing the number of pins for direct I/O control applications.

The **expanded microcomputer mode** supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, EPROM, and data EEPROM) remains active. Digital I/O ports (Ports A,B,C, and D), under control of their associated port control registers, can be configured via software to become the external 16-bit address bus, 8-bit data bus, and control interface. In applications where the entire address, data, or control bus is not required, each of these pins can be individually programmed as a general-purpose input/output or as its associated memory expansion alternate function, thereby maximizing the pins available for general-purpose input/output. The address bus and data bus are not multiplexed, eliminating the requirement for an external address/data latch and lowering the system cost.

Further reductions in external interface decode logic can be realized by using the precoded chip-select outputs that provide direct memory/peripheral chip-select or chip-enable functions. When memory accesses are performed to any location between 2000h and 3FFFh, pins $\overline{\text{CSE1}}$ and $\overline{\text{CSE2}}$ will become active if enabled by their port control registers. Similarly, memory accesses to any location between 8000h and FFFFh will activate $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ if enabled by their respective port control registers. As a result, up to 96K bytes of external memory can be mapped into the 32K-byte logical address space of 8000h to FFFFh by using $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ as memory bank selects under software control.

In the **microprocessor mode**, Ports A,B,C, and D are the address, data, and control buses for interface to external memory and peripherals. In this mode these ports are not programmable. The on-chip RAM and data EEPROM remain active, while the on-chip ROM, or EPROM is disabled. The program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.

The **microprocessor mode with internal program memory** is configured just as the microprocessor mode with respect to the external bus interface. However, the application program in external memory enables the internal program ROM or EPROM to also to be active in the system. This is accomplished by writing a zero to the MEMORY DISABLED control bit (SCCR1.2) of the SCCR1 control register.

Operating Mode Summary

OPERATING MODE	MC PIN	$\overline{\text{RESET}}$	OTHER
Microcomputer single chip	Low	↑	None
Microcomputer with expanded memory	Low	↑	Set digital I/O registers to function A or B†
Microprocessor	High	↑	None
Microprocessor with internal memory	High	↑	Enable internal memory (Clear SCCR1.2)

† Function A: Port D = chip select signals $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, $\overline{\text{CSH3}}$ and $\overline{\text{CSPF}}$
Function B: Port D = Expansion memory control signals $\overline{\text{OCF}}$, $\overline{\text{EDS}}$ and $\overline{\text{WAIT}}$

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memory/peripheral wait operation

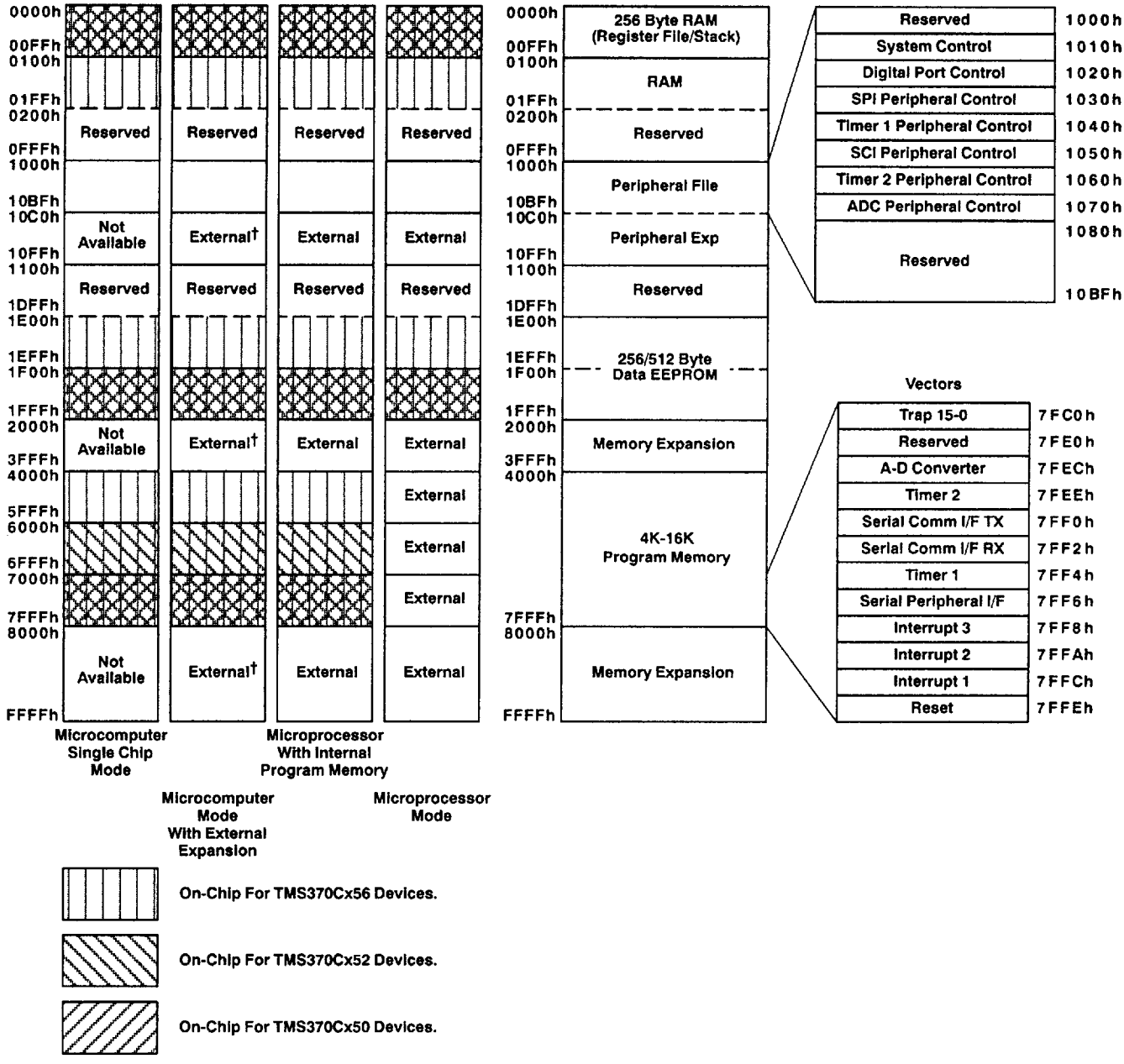
The TMS370Cx5x enhances interface flexibility by providing $\overline{\text{WAIT}}$ state support, thereby decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend their read/write accesses indefinitely by asserting the $\overline{\text{WAIT}}$ input pin, and the CPU will continue to wait as long as this signal remains active.

Programmable automatic wait state generation is also provided by the TMS370Cx5x on-chip bus controller. The TMS370Cx5x is configured, following hardware reset, to automatically add one wait state to all external bus transactions, and memory and peripheral accesses, thus making every external access a minimum of three system clock cycles. The designer can disable the automatic wait state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be independently extended to four system clock cycles if the PF AUTO WAIT bit in SCCR1 is set to 1. Programmable wait states can be used in conjunction with the external $\overline{\text{WAIT}}$ pin. In applications where the external device read/write access can interface with the TMS370Cx5x CPU using one wait state, the automatic wait state generation can eliminate external $\overline{\text{WAIT}}$ interface logic, lowering system cost.

memory map

The TMS370 family architecture is based on the Von Neumann architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped into this same common address space. In the expansion mode, external memory or peripherals are also memory mapped into this common address. As shown in Figure 1, the TMS370 provides a 16-bit address range to access internal or external RAM, ROM, EPROM, EEPROM, input/output pins, and peripheral functions.

The peripheral file contains all input/output port control, on-and off-chip peripheral status and control, EPROM memory programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. This page of 256 contiguous addresses is logically divided into 16 Peripheral File Frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx5x has its on-chip peripherals and system control assigned to Peripheral File Frames 1 through 7, addresses 1010h through 107Fh.



† Precoded Chip Select Outputs Available on External Expansion Bus.

NOTE: The term ***Reserved*** in this figure means the address space is reserved for future expansion, while the term ***Not Available*** means the address space is unavailable in the particular mode illustrated by that block.

Figure 1. TMS370Cx5x Memory Map

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on-chip memories

RAM/register file

The TMS370Cx5x family has up to 512 bytes of on-chip static RAM, addressed as 512 consecutive bytes mapped from location 0000h to 01FFh. The first 256 bytes (0000h-00FFh) serve as both the CPU register file and general purpose memory, the second 256 bytes (0100h-01FFh) serve as general purpose RAM. The first 256 bytes of RAM are treated as registers by the instruction set and are referenced as R0 through R255. The first two registers, R0 and R1, are also called the A and B registers, respectively. The stack is located in the on-chip RAM, and operates as a last-in first-out read/write memory. It is used to store the return address on subroutine calls and the status register during interrupts. Accessing this memory as registers is performed in one system clock cycle (t_c), while general purpose memory access is performed in two system clock cycles.

Instructions may be executed from RAM. This versatility enables the internal RAM to be used for functions such as microcontroller self-test, diagnostics, or system test of the end application. The user may load external programs or data into the RAM by incorporating a simple bootstrap loader in the program memory, or by operating the microcontroller in the microprocessor mode.

data EEPROM

The TMS370Cx5x family has up to 512 bytes of on-chip Electrically Erasable Programmable ROM (EEPROM), addressed as 512 consecutive bytes mapped from locations 1E00h to 1FFFh (1F00h to 1FFFh for devices with 256 bytes). The data EEPROM provides nonvolatile programmable storage for items such as calibration constants and configuration information for personalization of a generic program ROM/EPROM algorithm for use in specific end applications. The data EEPROM supports bit, byte, and block write/erase modes. Instructions may be executed from the data EEPROM, providing additional program space and the ability to patch algorithms by placing a branch table for volatile routines in the data EEPROM.

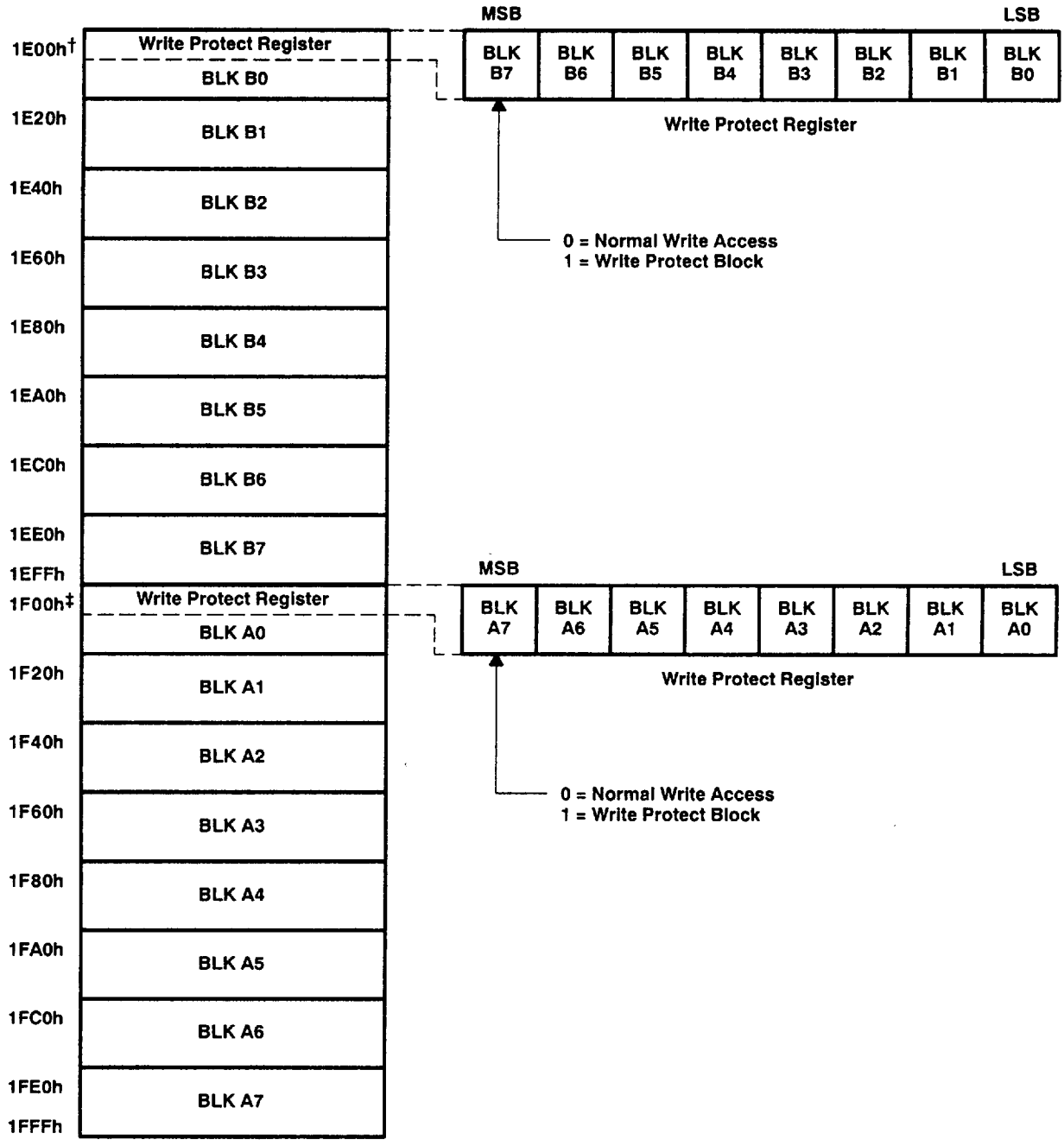
The data EEPROM uses the 5-V V_{CC} supply voltage and provides the programming voltage via an internal dedicated generator, eliminating the need for an external high-voltage programming source. The dedicated voltage generator optimizes the programming voltage characteristics, increasing the reliability as well as extending the write/erase endurance of the array.

Programming control and status monitoring are performed through the data EEPROM control register (DEECTL) in the peripheral file. An EEPROM write/erase operation is performed in the following sequence:

1. Perform normal memory write to the target EEPROM location.
2. Write to DEECTL control register to select WRITE1/WRITE0 and set the EXECUTE (EXE) bit to 1.
3. Wait for program time to elapse [$t_{w(PGM)B}$ or $t_{w(PGM)AR}$].
4. Write to DEECTL control register to set the EXECUTE (EXE) bit to 0.

The WRITE1/WRITE0 control bit selects whether the zeros or the ones in the data byte are to be programmed into the selected EEPROM location. For example, a WRITE1 operation will program ones into all bit positions within the EEPROM byte that have ones in the data byte, while bits that are zero in the data byte will not affect the EEPROM contents. The WRITE1 operation effectively performs a logical OR of the information previously stored on the EEPROM byte with the data byte. The WRITE0 operation effectively performs a logical AND between these two bytes. Single bit programming within an EEPROM byte is performed by writing only the zeros or ones of the data byte. The EEPROM programming algorithm may use this bit-programming capability to optimize the useful life of the EEPROM.

When a data value cannot be achieved by writing only zeros or only ones into the EEPROM byte, a WRITE1 followed by a WRITE0 will program any data value into the EEPROM byte, regardless of the previous data stored at that location.



† For devices with 512 bytes data EEPROM, the first first block of 32 bytes begins at loaction 1E00h and the last block ends at location 1FFFh.
‡ For devices with 256 bytes data EEPROM, the first first block of 32 bytes begins at loaction 1F00h and the last block ends at location 1FFFh.

Figure 2. Write Protect Register for TMS370Cx5x Devices With a Data EEPROM Array

Data EEPROM read accesses are performed as normal memory read operations in two system clock cycles. A memory read cycle to any EEPROM location while EXE = 1 returns the value currently being written to the EEPROM. Following an EEPROM write operation, the EEPROM voltages must stabilize prior to performing an EEPROM read operation. The BUSY FLAG indicates the status of the EEPROM voltage. When set, the EEPROM is not ready for a read operation. The BUSY flag is reset to 0 by the EEPROM control logic when 128 system clock cycles have elapsed following the EXE bit being set to 0. If an EEPROM read operation is performed while BUSY = 1, automatic WAIT states will be generated until BUSY = 0, and then the read operation will be performed.

Bytes within the data EEPROM can be protected from inadvertent overwriting of critical information. As shown in Figure 2, the 8-bit Write Protect Register (WPR), located at 1F00h within the data EEPROM, provides write protection for the TMS370Cx50 and TMS370Cx52 devices containing a 256-byte data EEPROM array, segmenting the array into eight blocks of 32 bytes each. The TMS370Cx56 devices containing a 512-byte data EEPROM array possess an additional Write Protection Register (see Figure 2) located at 1E00h within the data EEPROM, which will also segment the additional 256-byte array into eight blocks of 32 bytes each. Each of these 32-byte blocks may be individually write- and erase-protected by setting the corresponding bit to 1 in the appropriate WPR. Since the WPRs reside in the array in BLK A0 and BLK B0, the WPRs may also be write-protected, thereby increasing the system reliability by preventing bytes from being reprogrammed. Bytes left unprotected may be written to by the normal EEPROM programming sequence. The Write Protection Override (WPO) mode enables data to be written to any location in the data EEPROM, regardless of the WPR contents. The WPO mode is typically used in a service environment to update the protected EEPROM contents.

All unprotected bytes within the data EEPROM array may be programmed during a single EEPROM programming cycle by setting the ARRAY PROG bit DEECTL to 1 at the start of the programming cycle for TMS370Cx5x devices with a 256-byte data EEPROM array. The TMS370Cx5x devices with a 512-byte data EEPROM array must be in the WPO mode to enable array programming.

program ROM

The program ROM consists of 4K to 16K bytes of mask programmable read-only memory. The program ROM is used for permanent storage of data or instructions, with read operations performed in two system clock cycles. Memory addresses 7FECh through 7FFFh are reserved for interrupt and reset vectors. Memory locations 7FE0h through 7FEBh are reserved for factory use. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication.

program EPROM (TMS370C756 and SE370C756)

The program EPROM of the TMS370C756 and the SE370C756 is a 16K electrically programmable read-only memory, addressed as 16K consecutive bytes mapped from location 4000h to 7FFFh. It provides application performance identical to the TMS370Cx5x mask ROM devices with up to 16K bytes. Program instructions are read from the program EPROM in two system clock cycles, providing the prototyping capability of the mask program ROM.

An external supply is needed at the MC pin to provide the necessary programming voltage (V_{PP}). Programming is controlled through a register (EPCTL) in the peripheral file.

The TMS370C756 comes in a plastic package and cannot be erased. It is one-time-programmable (OTP). The SE370C756 comes in a ceramic package with a quartz window. Before programming, the SE370C756's EPROM is erased by exposing the device through the transparent window to high-intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, the entire array is in logic 1 state. A

programmed logic 0 can be erased to a logic 1 only by exposure to ultraviolet light. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SE370C756, the window should be covered with an opaque label. All devices are erased to a logic high upon delivery from the factory.

CAUTION

Exposing the EPROM module to ultraviolet light may also cause erasure in any EEPROM module. Any useful data stored in the EEPROM must be reprogrammed after exposure to UV light.

Programming lows into the EPROM is controlled by the EPCTL register via the EXE bit and the VPPS bit. The EXE bit initiates EPROM programming when set and disables programming when cleared. The VPPS bit connects the programming voltage V_{PP} at the MC pin to the EPROM module. VPPS (EPCTL.6) and EXE (EPCTL.0) should be set separately, and the VPPS bit should be set at least two microseconds before the EXE bit is set. After programming, the application programming should wait for four microseconds before any read attempt is made. The programming operation (see Figure 3) is performed in the following recommended sequence:

1. Supply the programming voltage to the MC pin.
2. Write to the EPCTL register to set the VPPS bit to 1.
3. Perform normal memory write register to the target EPROM location.
4. Write to the EPCTL register to set the EXE bit register to 1. (Wait at least two microseconds after step 2.)
5. Wait for program time to elapse (one millisecond).
6. Write to the EPCTL register to clear the EXE bit (leave VPPS bit set to 1).
7. Read the byte being programmed; if correct data is not read, repeat steps 4 through 6 up to a maximum X of 25.
8. Write to the EPCTL register to set the EXE bit to 1 for final programming.
9. Wait for program time to elapse (3× milliseconds duration).
10. Write to the EPCTL register to clear the EXE and VPPS bits.

An external power supply at V_{PP}, I_{PP} (30 mA), is required for programming operation. Programming voltage V_{PP} is supplied via the MC pin. This also automatically puts the microcontroller in the Write Protection Override (WPO) mode. Programming voltage may be applied via the MC pin anytime after $\overline{\text{RESET}}$ and remain at V_{PP} after programming (after the EXE bit is cleared). Applying programming voltage while $\overline{\text{RESET}}$ is active will put the microcontroller in a reserved mode, where programming operation is inhibited.

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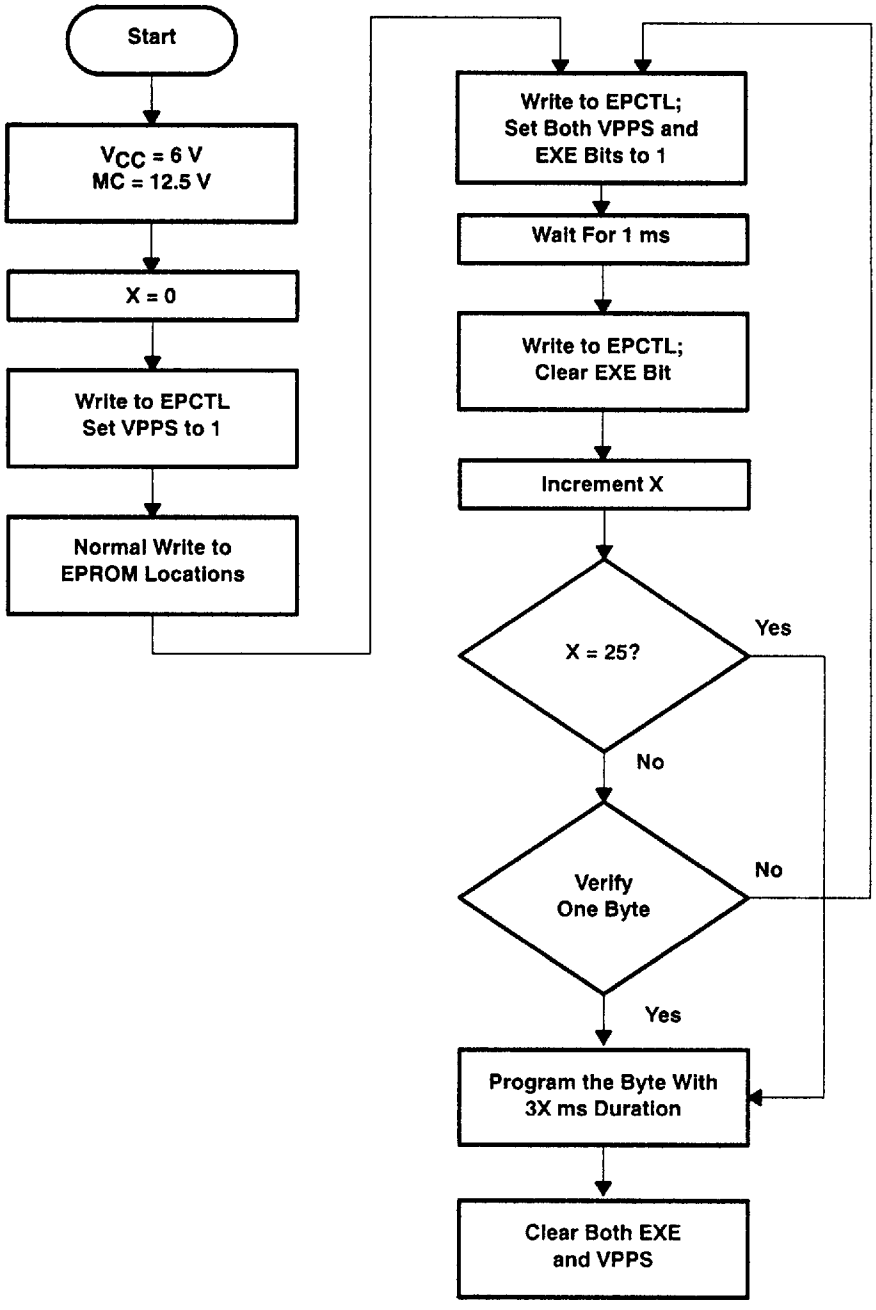

Figure 3. EPROM Programming Operation

central processing unit

The central processing unit (CPU) of the TMS370 family is an enhanced version of the TMS7000 Family CPU. The enhancements include additional user instructions such as integer divide, conditional jump instructions based on the overflow status bit, and addressing modes such as stack-pointer-relative addressing for subroutine parameter passing. The efficient register-to-register architecture of the TMS7000 family has been carried over to the TMS370 family to avoid the conventional accumulator bottleneck. The complete TMS370 family instruction set is summarized in the *TMS370 Instruction Set Summary*, page 47.

In addition to the interpretation and execution of the user program, the CPU performs the functions of bus protocol generation and interrupt priority arbitration. While the CPU is implemented independent of the memory, input/output, and peripheral modules, it performs the central system control function through communications with these on-chip modules and external memory and peripherals.

The TMS370 family CPU registers accessible to the programmer are shown in Figure 4. The register file consists of 256 general purpose registers, R0 through R255, implemented in on-chip RAM, and is used by the CPU for general purpose 8- and 16-bit source and destination operands, index registers, and indirect addressing. The first two registers, R0 and R1, are also called registers A and B and are used by the CPU for general purpose registers or for implied operands. The program counter (PC) contains the address of the next instruction to be executed. The stack pointer (SP) contains the address of the last or top entry on the stack, which is located in the on-chip register file. The status register (ST) contains four bits that reflect the outcome of the instruction just executed, and two bits that control the masking of the interrupt priority chains.

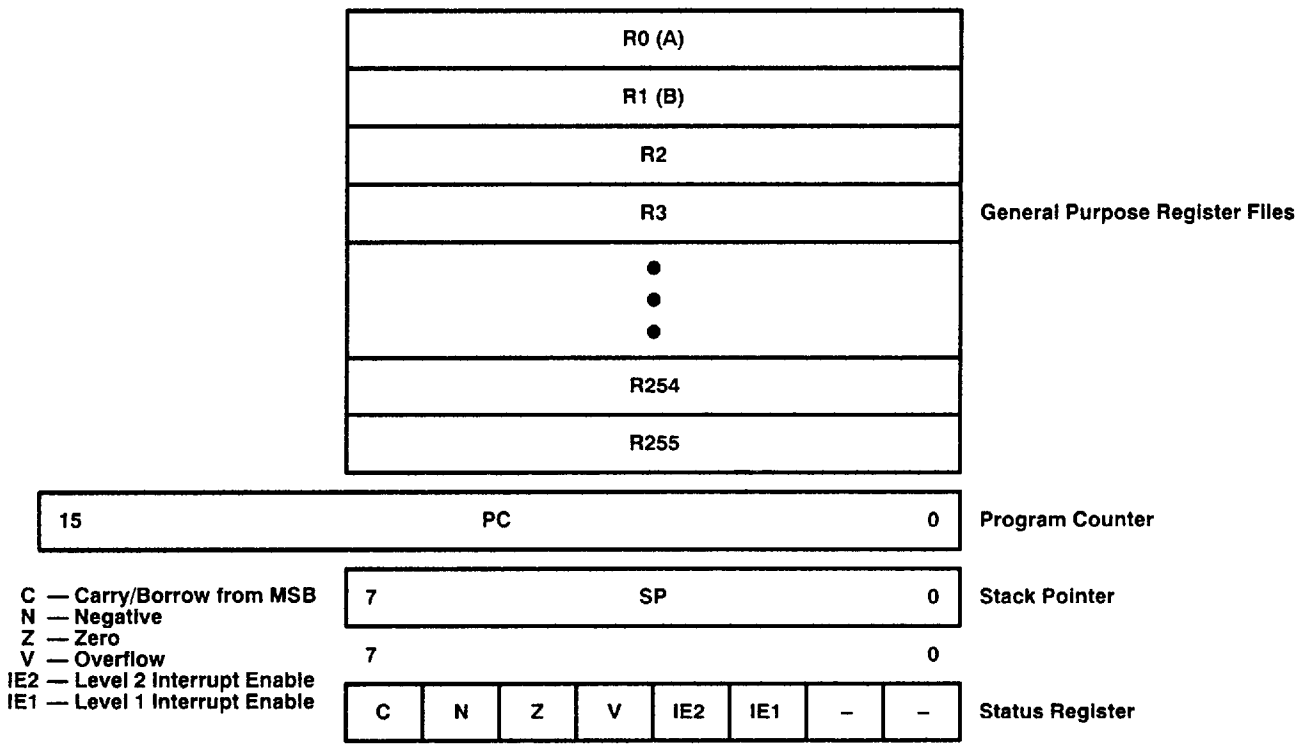

Figure 4. CPU Registers

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system resets

The TMS370Cx5x has three possible reset sources: a low input to the $\overline{\text{RESET}}$ pin, a programmable watchdog timer timeout, or a programmable oscillator fault failure. The $\overline{\text{RESET}}$ pin, an input/output pin, initiates TMS370Cx5x hardware initialization and ensures an orderly software startup. A low level input of at least 50 ns initiates the reset sequence. The microcontroller is held in reset until the $\overline{\text{RESET}}$ pin goes inactive (high). If the $\overline{\text{RESET}}$ input signal is low for less than eight system clock cycles, the TMS370Cx5x will hold the external $\overline{\text{RESET}}$ pin low for eight system clock cycles to reset external system components. The $\overline{\text{RESET}}$ pin must be activated by the application at power-up, which can be accomplished by an external input or an RC power-up reset circuit. Recall that the basic operating mode, microcomputer or microprocessor, is determined by the voltage level applied to the MC pin two cycles before the $\overline{\text{RESET}}$ pin goes inactive (high). The $\overline{\text{RESET}}$ pin can be asserted at any time during operation, resulting in an immediate initiation of the reset sequence.

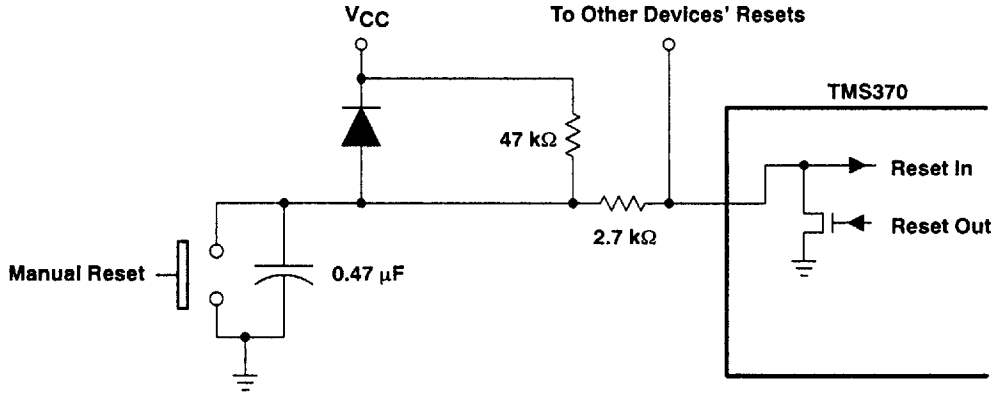

Figure 5. Typical Reset Circuit

The watchdog timer provides system software integrity by detecting a program that has become lost or is not executing as expected. A system reset is generated if the watchdog timer is not properly re-initialized by a specific software sequence, or if the re-initialization does not occur before the watchdog timer times out. The watchdog timer timeout initiates the TMS370Cx5x reset sequence and drives the external $\overline{\text{RESET}}$ pin low for eight system clock cycles to reset external system components. The watchdog reset function is enabled by setting WD OVRFL RST ENA bit of T1CTL2 to 1. Once the software enables the watchdog reset function, subsequent writes to the WD OVRFL RST ENA bit are ignored. Watchdog control bits can be initialized only following a powerup reset. The timer section discusses additional information on the watchdog timer and its configurations.

The oscillator fault circuit provides the means to monitor failures of the oscillator input signal (XTAL2/CLKIN). This function is enabled under software control by setting the OSC FLT RST ENA bit of SCCR2 to 1. If the oscillator input signal frequency remains above the 90% point of the minimum operating frequency (CLKIN), the oscillator input will not to be activated. However, if the oscillator input is lost or its frequency falls below 20 kHz and the oscillator fault reset is enabled, the TMS370Cx5x is reset and the external $\overline{\text{RESET}}$ pin is driven low.

Reset Sources

REGISTER	ADDRESS	PF	BIT #	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold or Warm start reset
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

When an oscillator input failure occurs, the internal clocks are stopped and $\overline{\text{RESET}}$ is held active until the oscillator input frequency is greater than 100 kHz typical. If the OSC FLT RST ENA bit of SCCR2 is set to 0, the fault detection circuit independently sets the OSC FLT FLAG of SCCR0 without generating a system reset. The OSC FLT RST ENA bit is protected during non-privileged operation and therefore should be software configured during the initialization sequence following system reset. During a HALT mode, the oscillator fault circuitry will be disabled.

During a microcontroller reset. the majority of the peripheral file bits are set to 0, with the exception of the bits shown in the following table. During all reset, the COLD START, OSC FLT FLAG, and the WD OVRFL FLAG are appropriately set by the active reset and may be interrogated by the program to determine the source of the system reset. Registers A and B are set to zero during all resets. The other registers are not affected by a reset under power (warm reset).

Control Bit States Following Reset

REGISTER	CONTROL BIT	POWER-UP	WARM RESET	
			MICROCOMPUTER	MICROPROCESSOR
SCCR0	μP/μC MODE	0	0	1
SCCR0	MC PIN DATA	0	0	1
SCCR0	COLD START	1	†	†
SCCR0	OSC FLT FLAG	0	†	†
T1CTL2	WD OVRFL FLAG	0	†	†
TXCTL	TX EMPTY	1	1	1
TXCTL	TXRDY	1	1	1
ADSTAT	AD READY	1	1	1

† Status bit corresponding to active reset source is set to 1.

interrupts

The TMS370 family software programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet realtime interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 6. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be independently masked by the global interrupt mask bits (IE1 and IE2) of the Status Register.

Each system interrupt is independently configured on either the high or low priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high or low priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion to future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx5x has ten hardware system interrupts as shown in the following table (page 18). Each system interrupt has a dedicated interrupt vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. (e.g., SCI RXINT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt.

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Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR INTERRUPT	PRIORITY§
External $\overline{\text{RESET}}$ Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$†	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1†	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2†	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3†	7FF8h, 7FF9h	4
SPI RX/TX Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 Overlfow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC INT FLAG WD OVRFL INT FLAG	T1INT‡	7FF4h, 7FF5h	6
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT†	7FF2h, 7FF3h	7
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8
Timer 2 Overflow Timer 2 Compare 1 Timer 2 Compare 2 Timer 2 External Edge Timer 2 Input Capture 1 Timer 2 Input Capture 2	T2 OVRFL INT FLAG T2C1 INT FLAG T2C2 INT FLAG T2EDGE INT FLAG T2IC1 INT FLAG T2IC2 INT FLAG	T2INT	7FEEh, 7FEFh	9
A-D Conversion Complete	AD INT FLAG	ADINT	7FECh, 7FEDh	10

† Releases microcontroller from STANDBY and HALT low power modes.
‡ Releases microcontroller from STANDBY low power mode.
§ Relative priority within an interrupt level.

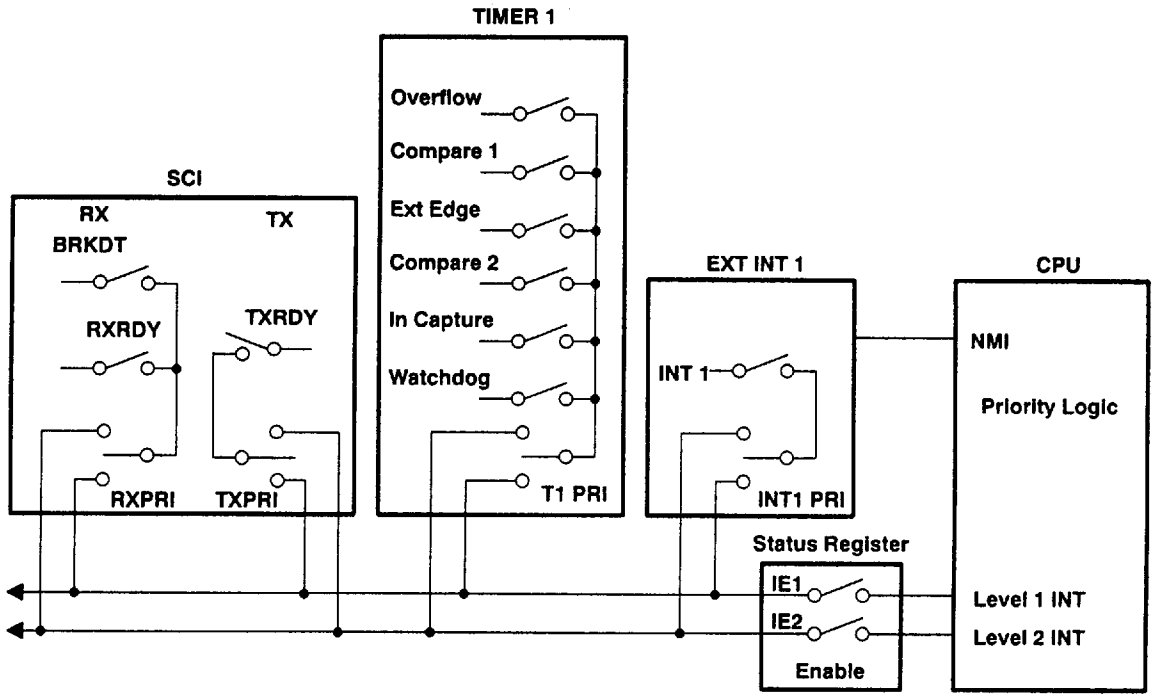

Figure 6. Interrupt Control

Six of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable bits. Recall that the INT1 NMI bit is protected during nonprivileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

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privileged operation and EEPROM write protection override

The TMS370Cx5x family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The non-privileged mode of operation ensures the integrity of the system configuration once defined for an end application. Following a hardware reset, the TMS370Cx5x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access and the application program will configure the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) will be set to 1, entering the non-privileged mode and disabling write operations to specific configuration control bits within the peripheral file. The following system configuration bits are write-protected during the non-privileged mode and must be configured by software prior to exiting the privileged mode:

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5	PF AUTO-WAIT
SCCR0	P010.6	OSC POWER
SCCR1	P011.2	MEMORY DISABLE
SCCR1	P011.4	AUTOWAIT DISABLE
SCCR2	P012.0	PRIVILEGE DISABLE
SCCR2	P012.6	PWRDWN/IDLE
SCRR2	P012.7	HALT/STANDBY
SCCR2	P012.1	INT1 NMI
SCRR2	P012.2	OSC FLT DISABLE
SCCR2	P012.5	OSC FLT RST ENA
SPIPRI	P03F.6	SPI PRIORITY
SPIPRI	P05F.6	SCI TX PRIORITY
SPIPRI	P05F.5	SCI RX PRIORITY
T1PRI	P04F.6	T1 PRIORITY
T2PRI	P06F.6	T2 PRIORITY
ADPRI	P07F.6	AD PRIORITY

† Identified by name and bit location within the register

The privileged bits are shown in a **bold typeface** in the following section Peripheral File Frame 1.

The Write Protection Override (WPO) mode provides an external hardware method of overriding the Write Protection Registers (WPR) of the data EEPROM on the TMS370Cx5x. The WPO mode is entered by applying a 12-V input to the MC pin after the $\overline{\text{RESET}}$ pin input goes high. The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the personality or calibration information in the data EEPROM while the device remains in the application, but only while requiring a 12-volt external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

peripheral file frame 1

Peripheral File Frame 1 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a **bold typeface** in the Peripheral File Frames.

Peripheral File Frame 1: System Configuration and Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1010h	P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
1011h	P011	—	—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
1012h	P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	**OSC FLT RST ENA**	**BUS STEST**	**CPU STEST**	**OSC FLT DISABLE**	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
1013h to 1016h	P013 to P016	Reserved								
1017h	P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
1018h	P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
1019h	P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
101Ah	P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
101Bh	P01B	Reserved								
101Ch	P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
101Dh 101Eh 101Fh	P01D P01E P01F	Reserved								

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peripheral file frame 2

Peripheral File Frame 2 contains the digital I/O pin configuration and control registers. The following figure details the specific addresses, registers, and control bits within this Peripheral File Frame.

Peripheral File Frame 2: Digital Port Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1020h	P020	Reserved								APORT1
1021h	P021	Port A Control Register 2								APORT2
1022h	P022	Port A Data								ADATA
1023h	P023	Port A Direction								ADIR
1024h	P024	Reserved								BPORT1
1025h	P025	Port B Control Register 2								BPORT2
1026h	P026	Port B Data								BDATA
1027h	P027	Port B Direction								BDIR
1028h	P028	Reserved								CPORT1
1029h	P029	Port C Control Register 2								CPORT2
102Ah	P02A	Port C Data								CDATA
102Bh	P02B	Port C Direction								CDIR
102Ch	P02C	Port D Control Register 1								DPORT1
102Dh	P02D	Port D Control Register 2								DPORT2
102Eh	P02E	Port D Data								DDATA
102Fh	P02F	Port D Direction								DDIR

Port Configuration Registers Set-up

PORT	PIN	INPUT XPORT1 = 0† XPORT2 = 0 XDATA = y XDIR = 0	OUTPUT XPORT1 = 0† XPORT2 = 0 XDATA = q XDIR = 1	FUNCTION A XPORT1 = 0† XPORT2 = 1 XDATA = x XDIR = x	FUNCTION B (μP MODE) XPORT1 = 1† XPORT2 = 1 XDATA = x XDIR = x
A	0 – 7	Data In y	Data Out q	Data Bus	Reserved
B	0 – 7	Data In y	Data Out q	Low ADDR	Reserved
C	0 – 7	Data In y	Data Out q	HI ADDR	Reserved
D	0	Data In y	Data Out q	$\overline{CSE2}$	$\overline{OCF}$
D	1	Data In y	Data Out q	$\overline{CSH3}$	
D	2	Data In y	Data Out q	$\overline{CSH2}$	
D	3	Data In y	Data Out q	CLKOUT	CLKOUT
D	4	Data In y	Data Out q	R/$\overline{W}$	R/$\overline{W}$
D	5	Data In y	Data Out q	$\overline{CSPF}$	
D	6	Data In y	Data Out q	$\overline{CSH1}$	$\overline{EDS}$
D	7	Data In y	Data Out q	$\overline{CSE1}$	$\overline{WAIT}$

XPORT1 = 1
XPORT2 = 0
XDATA = x
XDIR = x
} Not Defined

† DPORT ONLY

low-power operating modes

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY=0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, Timer 1 and the receiver start bit detection circuit of the serial communications interface remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupts, Timer 1 interrupt, or a low level on the receive pin of the serial communications interface) is detected.

In the HALT mode (HALT/STANDBY=1), the TMS370Cx5x is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt, or low level on the receive pin of the serial communications interface) is detected.

POWERDOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	Standby
1	1	Halt

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. All CPU instruction processing is stopped during the STANDBY and HALT modes, and clocking of the watchdog timer is inhibited.

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programmable timers

The two programmable timer modules of the TMS370Cx5x provide the designer with the enhanced timer resources required to perform realtime system control. The Timer 1 module contains the general-purpose timer T1 and the Watchdog timer (WD). The three independent 16-bit timers, T1, T2, and WD, allow program selection of input clock sources (realtime, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. These timers provide the capabilities for:

System Requirements	Timer Resource
Realtime System Control	Interval Timers with Interrupts
Input Pulse-Width Measurement	Pulse-Accumulate or Input-Capture Functions
External Event Synchronization	Event Counter Function
Timer Output Control	Compare Function
Pulse-Width Modulated Output Control	PWM Output Function
System Integrity	Watchdog Function

timer 1 module

The timer 1 module consists of three major blocks:

1. Prescaler/Clock Source, which determines the independent clock sources for the general purpose timer and the watchdog timer.
2. 16-bit General Purpose Timer, T1, which provides the event count, input capture, and compare functions.
3. 16-bit Watchdog Timer, which may be software programmed as an event counter/pulse accumulator if the watchdog function is not desired.

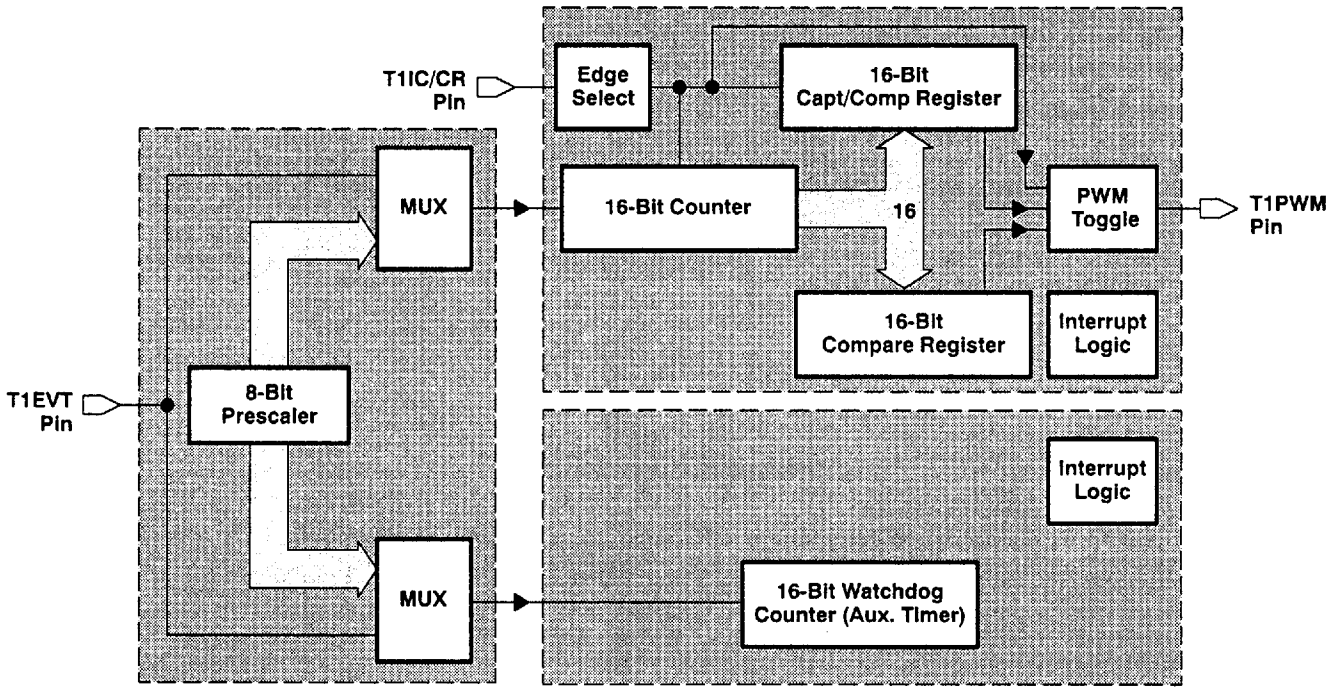

Figure 7. Timer 1 Module Block Diagram

timer 1 module prescaler/clock source

The clock source inputs for the general purpose timer and the watchdog timer are independently configured by the T1 and WD INPUT SELECT control bits of the T1CTL1 control register. The WD INPUT SELECT control bits cannot be changed after entering the watchdog mode (WD RST ENA = 1). Eight possible clock sources are programmable for each counter.

T1 INPUT			CLOCK SOURCE	WD INPUT		
SELECT 2	SELECT 1	SELECT 0		SELECT 2	SELECT 1	SELECT 0
0	0	0	System Clock	0	0	0
0	0	1	Pulse Accumulate	0	0	1
0	1	0	Event Input	0	1	0
0	1	1	No Clock Input	0	1	1
1	0	0	System Clock/4	1	0	0
1	0	1	System Clock/16	1	0	1
1	1	0	System Clock/64	1	1	0
1	1	1	System Clock/256	1	1	1

For realtime control applications, both the general-purpose timer and the watchdog timer are independently programmable from 16 to 24 bits in length. The 24-bit prescaler/timer generates overflow rates ranging from 13.1 ms with 200 ns timer resolution to 3.35 seconds with 51.2 μs timer resolution (external clock = 20 MHz).

In the **event counter mode**, an external high-to-low transition on the T1EVT pin is used to provide the clock for the internal timers. As shown in Figure 8, the T1EVT input provides the timer clock and is not routed through the prescaler. The T1EVT external clock frequency may not exceed the system clock frequency divided by 2. The general-purpose timer and the watchdog timer are programmable as 16-bit event counters.

In the **pulse accumulate mode**, an external input on the T1EVT pin is used to gate the internal system clock to the internal timers. While T1EVT input is logic 1, the timers will be clocked at the system clock rate and will accumulate system clock pulses until the T1EVT pin returns to logic 0. Both the general purpose timer and the watchdog timer are programmable as 16-bit pulse accumulators.

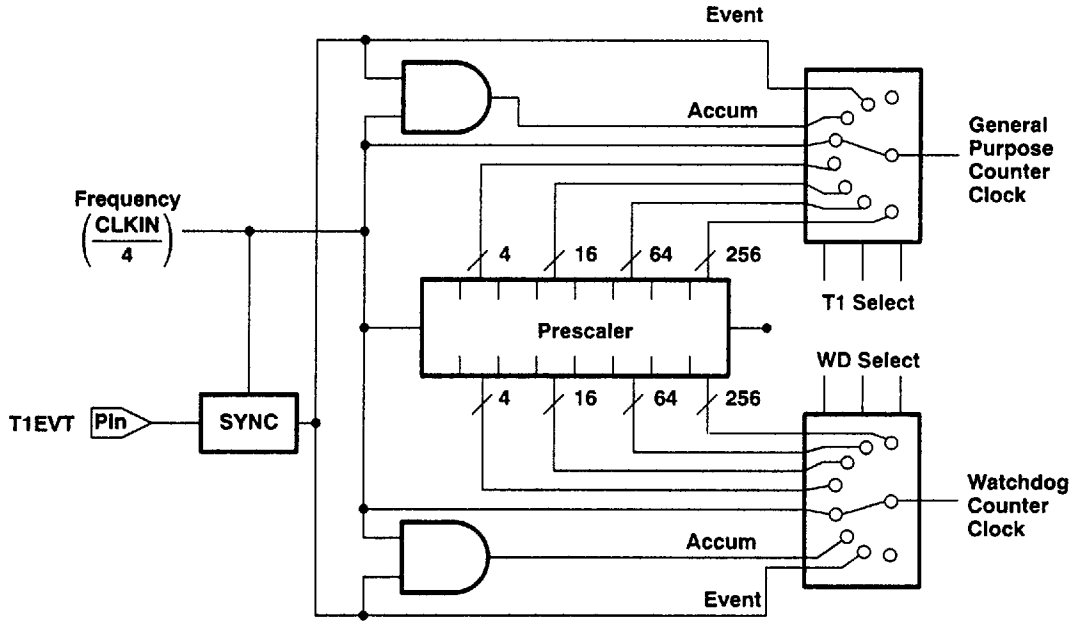

Figure 8. Timer 1 Counter Prescaler

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timer 1 general purpose timer

The 16-bit general purpose timer, T1, is composed of a 16-bit resettable counter, a 16-bit compare register and associated compare logic, and a 16-bit register that functions as a capture register in one mode and a compare register in the other mode. The T1 MODE bit selects whether T1 operates in the Capture/Compare mode or the Dual Compare mode.

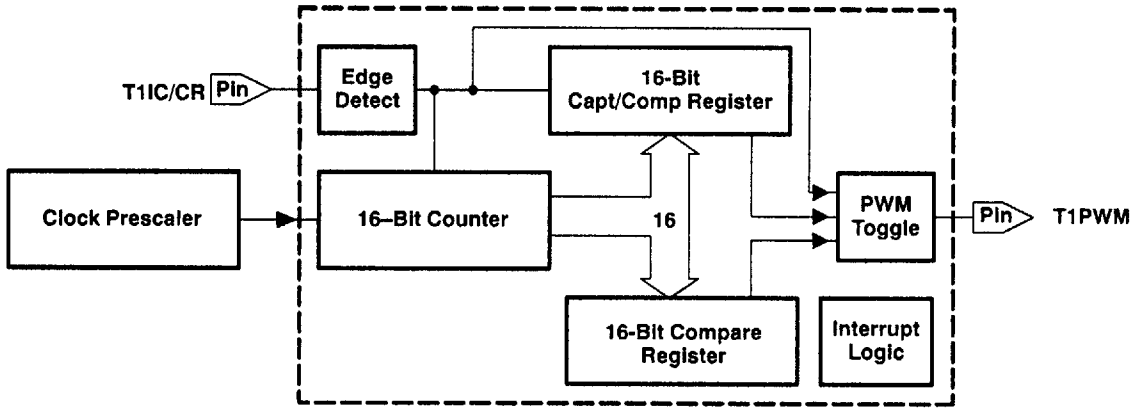


Figure 9. Timer 1 — General Purpose Timer

The counter is a free-running, 16-bit up-counter, clocked by the output of the Prescaler/Clock source. During initialization the counter is loaded with 0000h and begins its up-count. If the counter is not reset before reaching FFFFh, the counter will roll over to 0000h and continue counting. Upon counter roll-over, the T1 OVRFL INT FLAG is set to 1, and a timer interrupt is generated if the T1 OVRFL INT ENA bit is set to 1.

The counter may be reset to 0000h during counting by either, 1) writing a 1 to the T1 SW RESET bit, 2) a compare equal condition from the dedicated T1 compare function, or 3) an external pulse on the T1 IC/CR pin (Dual Compare mode). The designer may select via software (T1EDGE POLARITY bit) which external transition, low-to-high or high-to-low, on the T1IC/CR pin will cause the counter to be reset.

Special circuitry prevents the 16-bit registers, including the Counter, Compare, or Capture registers, from changing in the middle of a 16-bit read or write operation. When reading a 16-bit register, read the LSB first, then read the MSB. When writing to a 16-bit register, write the MSB first, then write the LSB. Take care to prevent accesses to another 16-bit register within this module during a 16-bit read or write. Such accesses might occur during the interrupt routines.

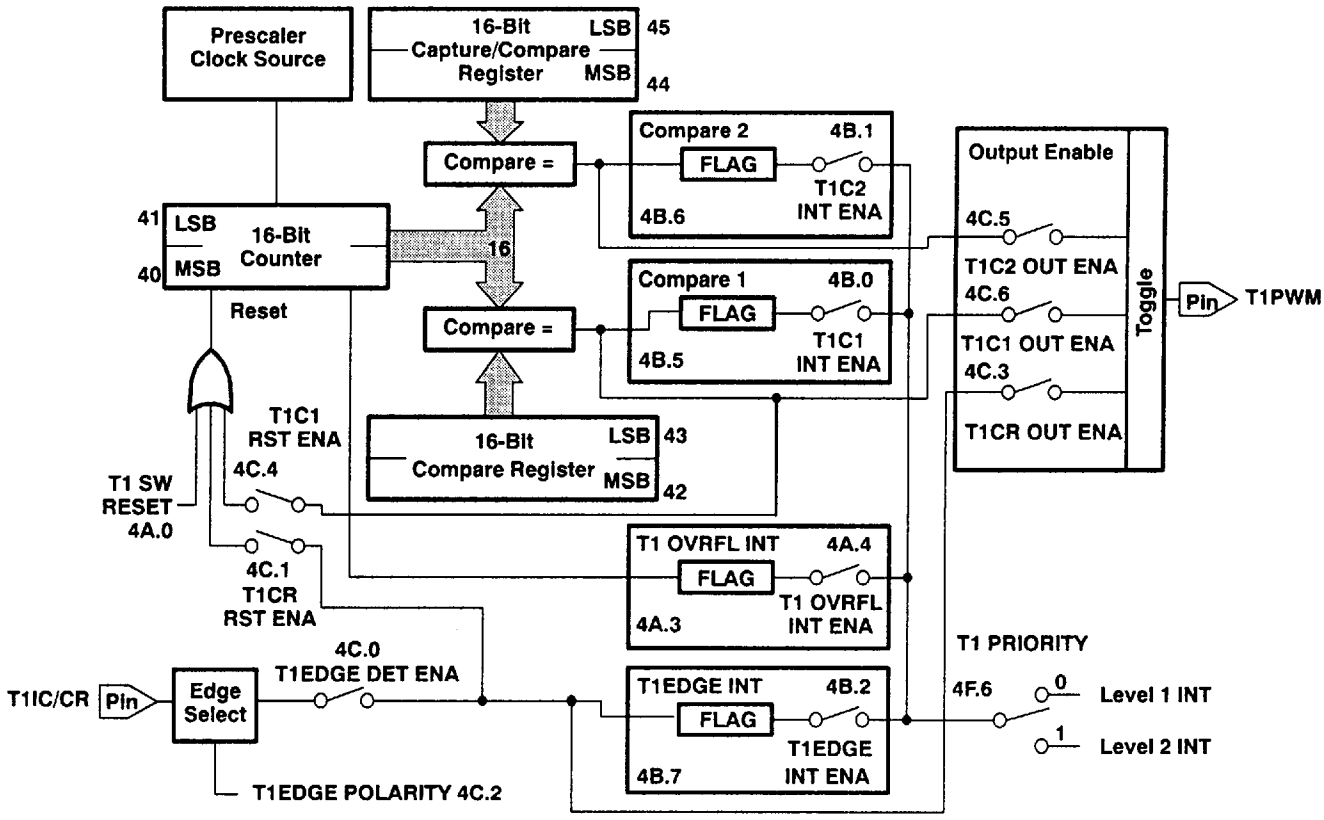
The timer 1 module has three I/O pins used for the functions as shown in the following table. Any of these three pins not used in a timer application may be individually configured as general purpose digital I/O pins by the timer 1 module port control registers (T1PC1 and T1PC2).

Timer 1 Module I/O Pin Functions

PIN	DUAL COMPARE MODE	CAPTURE/COMPARE MODE
T1IC/CR T1PWM T1EVT	Counter Reset input PWM output External Event input or Pulse Accumulate input	Input Capture input Compare output External Event input or Pulse Accumulate input

The **Dual Compare mode** (T1 MODE = 0) provides two compare registers, an external resettable counter, and a timer output pin. These allow the timer to act as an interval timer, a PWM output, simple output toggle, or many other timer functions. The Dual Compare mode as shown in Figure 10 continuously compares the contents of the two compare registers to the current value of the 16-bit counter. If a timer compare register equals the counter, the circuit sets the associated interrupt flag to 1 and toggles the T1PWM output pin if enabled, and/or generates a Timer 1 interrupt. An output compare equal condition from the dedicated compare register can also initiate a counter reset. A programmable interval timer function, selected by using the compare equal condition to generate a system interrupt and the counter reset function, generates a periodic interrupt.

Either compare function may be used to toggle the T1PWM output pin when a timer compare equal occurs, while the other compare function may be used for another system timing function. Using both compare functions to control the T1PWM pin allows direct PWM generation with minimal CPU software overhead. In typical PWM applications, the compare register is written with the periodic interval and is configured to allow counter reset on compare equal, and the Capture/Compare register is written with the pulse width to be generated within that interval. The program pulse width may be changed by the application program during the timer operation to alter the PWM output. For high-speed control applications, a minimum pulse width of 200 ns and a period as low as 400 ns can be maintained when using a clock of 20 MHz.

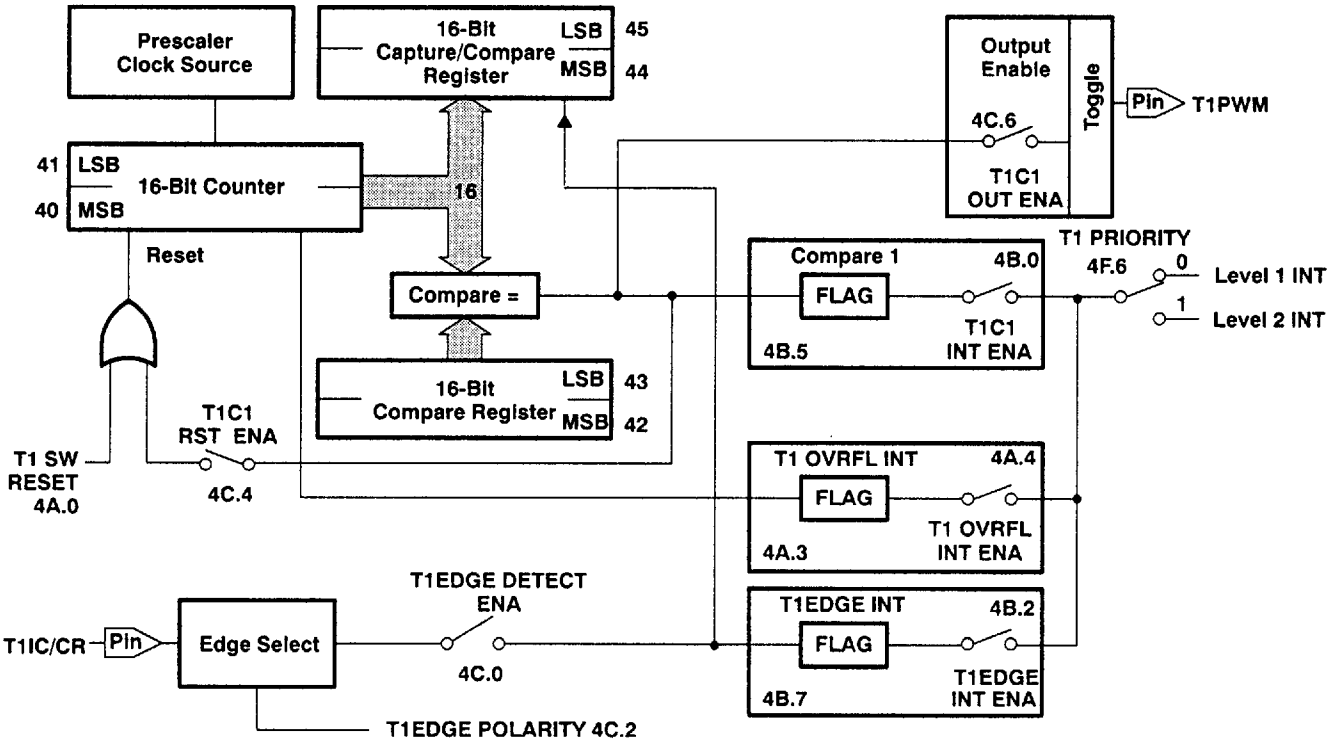


NOTE 2: The numbers on the diagram such as 4C.0, identify the register and the bit in the peripheral frame. For example, the actual address of 4C.0 is 104Ch, bit 0, in the T1CTL4 register.

Figure 10. Timer 1 — Dual Compare Mode

In addition, a PWM output that is initiated by a transition on an external pin is provided by the timer hardware to support time-critical control applications. Typically, in these applications an external input (T1IC/CR) is used to reset the counter, generate a timer interrupt, and toggle the T1 PWM pin to start the PWM output. The compare function will then toggle the output after the programmed pulse width has elapsed. The input edge detect function is enabled under program control by the T1CR DET ENA bit, and upon the next occurrence of the selected edge transition, the T1EDGE INT FLAG bit is set to 1, a timer interrupt is generated (if T1EDGE INT ENA = 1), and the T1PWM output pin is toggled (if T1CR OUT ENA = 1). Selection of the active input transition is under control of T1EDGE POLARITY. In the Dual Compare mode, the edge detect function must be re-enabled after each valid edge detect.

In the **Capture/Compare mode** (T1 MODE = 1), T1 is configured to provide one input capture register for external timing and pulse width measurement, and one compare register for use as a programmable interval timer. The compare register in this mode functions the same as in the Dual Compare mode described above, including the ability to toggle the PWM pin. The capture/compare register functions in this mode as a 16-bit input capture register, as shown in Figure 11. On the occurrence of a valid input on the T1IC/CR pin, the current counter value is loaded into the 16-bit input capture register, the T1EDGE INT FLAG is set to 1, and a timer interrupt is generated (if T1EDGE INT ENA = 1). The input detect function is enabled by the T1EDGE DET ENA bit, with T1EDGE POLARITY selecting the active input transition. In the Capture/Compare mode, the edge detect function, once enabled, remains enabled following a valid edge detect.



NOTE 2: The numbers on the diagram, such as 4C.0, identify the register and the bit in the peripheral frame. For example, the actual address of 4C.0 is 104Ch, bit 0, in the T1CTL4 register.

Figure 11. Timer 1 — Capture/Compare Mode

timer 1 module watchdog timer

The watchdog timer, contained in the timer 1 module, is a free-running 16-bit resettable up-counter clocked by the output of the Prescaler/Clock Source. The timer is software configured as either a watchdog timer to protect against system software failures and errors, or as a general purpose timer if the watchdog function is not desired. The 16-bit up-counter is programmable (via the WD OVRFL TAP SEL bit) to set the initial count at either 0000h or 8000h. The current value of the watchdog timer may be read at any time during its operation.

In the **watchdog mode** (WD OVRFL RST ENA = 1), the timer will generate a system reset if the timer is re-initialized by an incorrect value or if the counter overflows. The required re-initialization frequency is determined by the system clock frequency, the prescaler/clock source selected, and whether the WD OVRFL TAP SEL bit is set for a 15 or 16 bit counter rollover. With a clock = 20 MHz, the watchdog timer overflow rates range from 6.55 ms to 3.35 seconds. These values are selected prior to entering the watchdog mode because once the software enables the watchdog reset function (WD OVRFL RST ENA set to 1), subsequent writes to these control bits are ignored. Writes to these watchdog control bits can occur only following a powerup reset, which enhances watchdog timer system software integrity.

The watchdog timer is re-initialized by writing a predefined value to the watchdog reset key (WDRST) located in the peripheral file. The proper reset key alternates between 55h and AAH, beginning with 55h following the enable of the watchdog reset function. Writes of the correct value must occur prior to the timer overflow period. A write of any value other than the correct predefined value to the watchdog reset key will be interpreted as a lost program and a system reset will be initiated. A watchdog timer overflow or incorrect reset key will set the WD OVRFL INT FLAG bit to 1 and may be interrogated by the program following system reset to determine the source of the reset.

In the **non-watchdog mode** (WD OVRFL RST ENA = 0), the watchdog timer may be used as an event counter, pulse accumulator, or as an interval timer. In this mode, the system reset function is disabled. The watchdog counter is re-initialized by writing any value to the watchdog reset key (WDRST). When used as an interval timer, the timer overflow interval is determined by the system clock frequency, the prescaler/clock source value selected, and the value of the WD OVRFL TAP SEL bit. If the WD counter is not reset before overflowing, the counter will roll over to either 0000h or 8000h, as determined by the WD OVRFL TAP SEL bit, and continue counting. Upon counter overflow, the WD OVRFL INT FLAG is set to 1 and a timer interrupt is generated if the WD OVRFL INT ENA bit is set to 1. Alternately, an external input on the T1 EVT pin may be used with the watchdog timer to provide an additional 16-bit event counter or pulse accumulator.

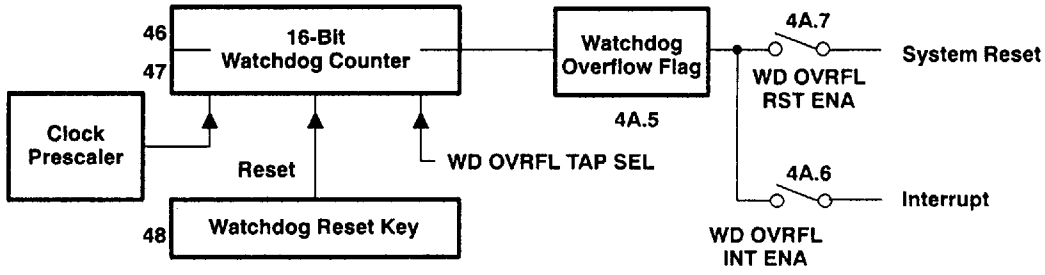


Figure 12. Watchdog/General Purpose Timer

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Peripheral File Frame 4: Timer 1 Module Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1040h	P040	Bit 15			Counter MSB				Bit 8	T1CNTR
1041h	P041	Bit 7			Counter LSB				Bit 0	
1042h	P042	Bit 15			Compare Register MSB				Bit 8	T1C
1043h	P043	Bit 7			Compare Register LSB				Bit 0	
1044h	P044	Bit 15			Capture/Compare Register MSB				Bit 8	T1CC
1045h	P045	Bit 7			Capture/Compare Register LSB				Bit 0	
1046h	P046	Bit 15			Watchdog Counter MSB				Bit 8	WDCNTR
1047h	P047	Bit 7			Watchdog Counter LSB				Bit 0	
1048h	P048	Watchdog Reset Key								WDRST
1049h	P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1INPUT SELECT2	T1INPUT SELECT1	T1INPUT SELECT0	T1CTL1
104Ah	P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	TI OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual Compare										
104Bh	P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
104Ch	P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare										
104Bh	P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
104Ch	P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
104Dh	P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
104Eh	P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
104Fh	P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until after a full power-down cycle has been completed.

The formulas in Figure 13 show the calculations for the resulting time, given values in the compare registers T1C and T1CC.

$$\text{time} = \left(\frac{4}{\text{CLKIN}}\right) (\text{prescale}) \ (\text{compare} + 1)$$

or

$$\text{time} = t_c \ (\text{prescale}) \ (\text{compare} + 1)$$

Figure 13. Timer 1 Compare Register Formulas

timer 2 module

Timer 2 consists of a clock source block and a 16-bit general purpose timer that provides the event count, input capture, and compare functions.

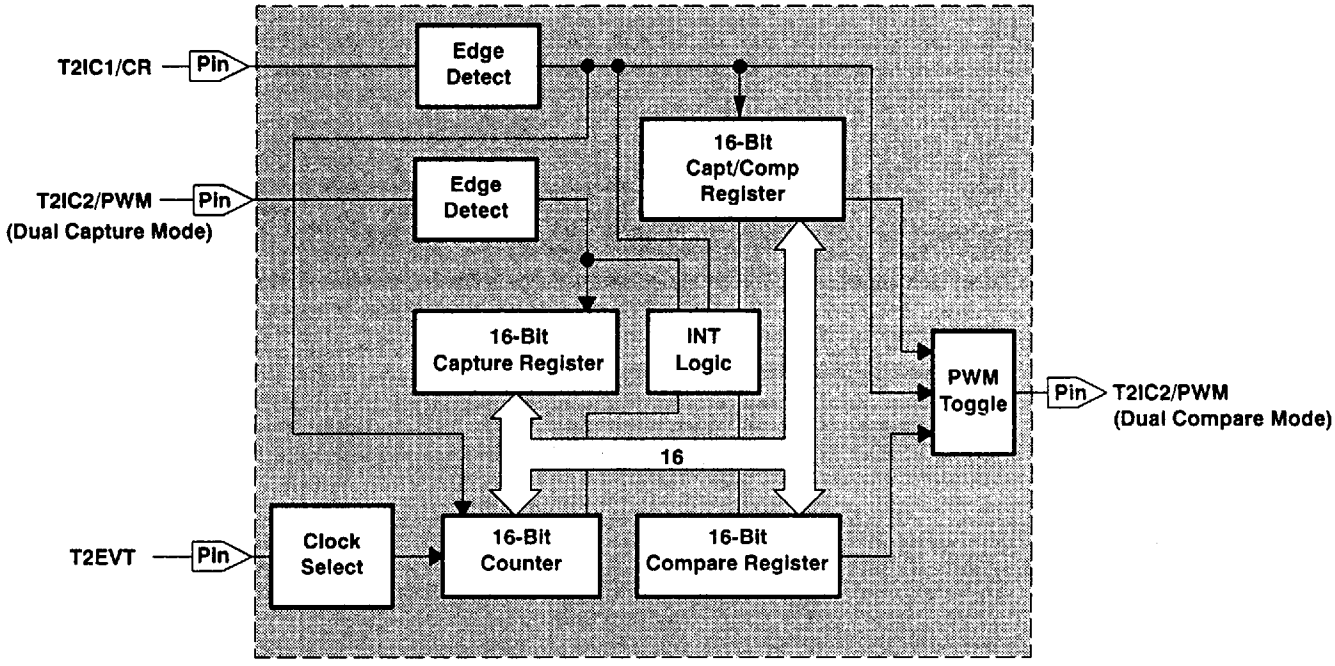

Figure 14. Timer 2 Module Block Diagram

timer 2 clock source

The clock source input for the general purpose timer is configured by the T2 INPUT SELECT control bits of the T2CTL1 control register. The four programmable clock sources for the general purpose counter are system clock, pulse accumulate, event input, or no clock input (counter stopped). When using the system clock input, the 16-bit timer generates an overflow rate of 13.1 ms with 200 ns resolution (clock = 20 MHz).

In the **event counter mode**, the general purpose timer is programmable as a 16-bit event counter. An external low-to-high transition on the T2EVT pin is used to provide the clock for the internal timer. The T2EVT external clock frequency may not exceed the system clock frequency divided by 2.

In the **pulse accumulate mode**, the general purpose timer is programmable as a 16-bit pulse accumulator. An external input on the T2EVT pin is used to gate the internal system clock to the internal timers. While T2EVT input is logic 1, the timers will be clocked at the system clock rate and will count system clock pulses until the T2EVT pin returns to logic zero.

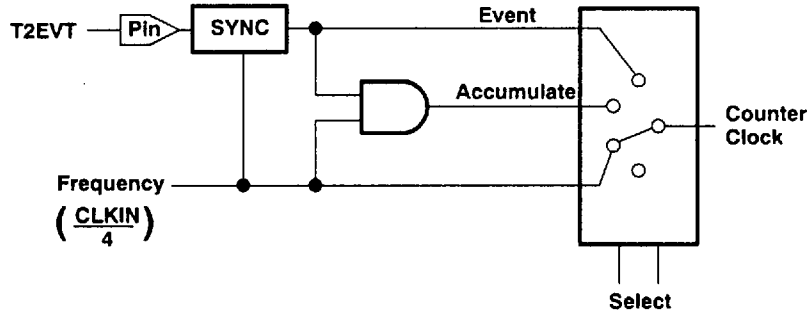

Figure 15. Timer 2 Clock Select

timer 2 general purpose timer

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The 16-bit general purpose timer, T2 , is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, a 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and a compare register in the other mode. The T2 MODE bit selects whether T2 operates in the Dual Compare mode or the Dual Capture mode.

The counter is a free-running 16-bit up-counter, clocked by the system clock, external event, or system clock while external event active (pulse accumulate). During initialization, the counter is loaded with 0000h and begins its up-count. If the counter is not reset before reaching FFFFh, the counter will roll over to 0000h and continue counting. Upon counter roll-over, the T2 OVRFLINT FLAG is set to 1, and a timer interrupt is generated if the T2 OVRFL INT ENA bit is set to 1.

The counter may be reset to 0000h during counting by either; 1) writing a 1 to the T2 SW RESET bit, 2) a compare equal condition from the dedicated T2 compare function, or 3) an external pulse on the T2IC1/CR pin (Dual Compare mode). The designer may select via software (T2CR POLARITY bit) which external transition, low-to-high or high-to-low, on the T2IC1/CR pin will cause the counter to be reset.

Special circuitry prevents the 16-bit registers, including the Counter, Compare, or Capture registers, from changing in the middle of a 16-bit read or write operation. When reading a 16-bit register, read the LSB first and then read the MSB. When writing to a 16-bit register, write the MSB first and then write the LSB. The register value will not change between reading or writing the bytes when done in this order.

Timer 2 has three I/O pins used for functions as shown in the table below. Any of these three pins not used in a timer application may be individually configured as general purpose digital I/O pins by the Timer 2 port control registers (T2PC1 and T2PC2).

Timer 2 I/0 Pin Functions

PIN	DUAL COMPARE MODE	DUAL CAPTURE MODE
T2IC1/CR	Counter reset input.	Input Capture 1 input.
T2IC2/PWM	PWM output.	Input Capture 2 input.
T2EVT	External event input or pulse accumulate input.	External event input or pulse accumulate input.

The **Dual Compare mode** (T2 MODE = 0) provides two compare registers, an external resettable counter, and a timer output pin. These allow the timer to act as a interval timer, a PWM output, simple output toggle, or many other timer functions. In this mode, the capture/compare register functions as a 16-bit read/write compare register, as shown in Figure 16. The operation of T2 is identical to T1 while operating in the dual compare mode.

In the **Dual Capture mode** (T2 MODE = 1), T2 is configured to provide one compare register for use as a programmable interval timer, and two input capture registers for external input timing and pulse width measurement. In this mode the capture/compare register functions as a 16-bit input capture register, as shown in Figure 17. Each capture input pin (T2IC1/CR and T2IC2/PWM) has an input edge detect function enabled by the associated DET ENA control bit, with the associated POLARITY bit selecting the active input transition. On the occurrence of a valid input on the T2IC1/CR or T2IC2/PWM pin, the current counter value is loaded into the 16-bit capture/compare and 16-bit input capture register, respectively. In addition, the respective input capture INT FLAG is set to 1 and a timer interrupt is generated if the respective INT ENA is set to 1.

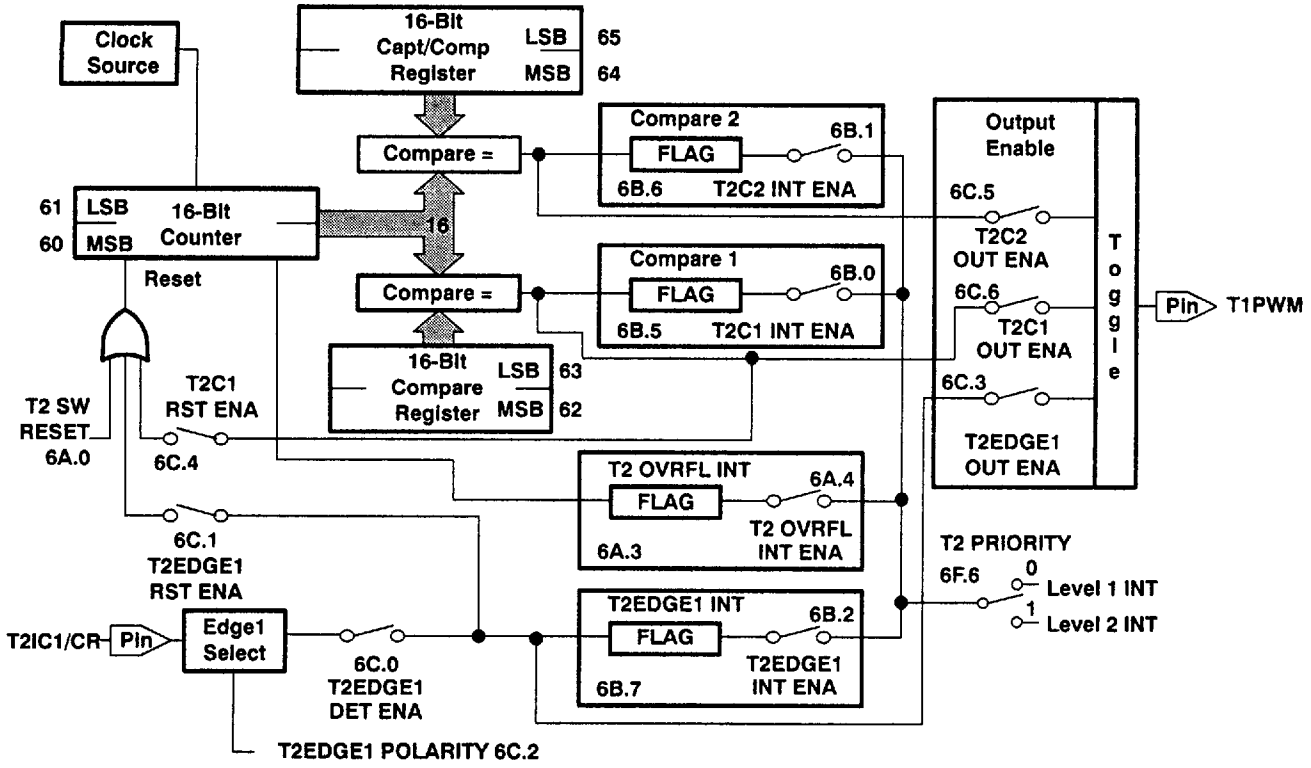

Figure 16. Timer 2— Dual Compare Mode

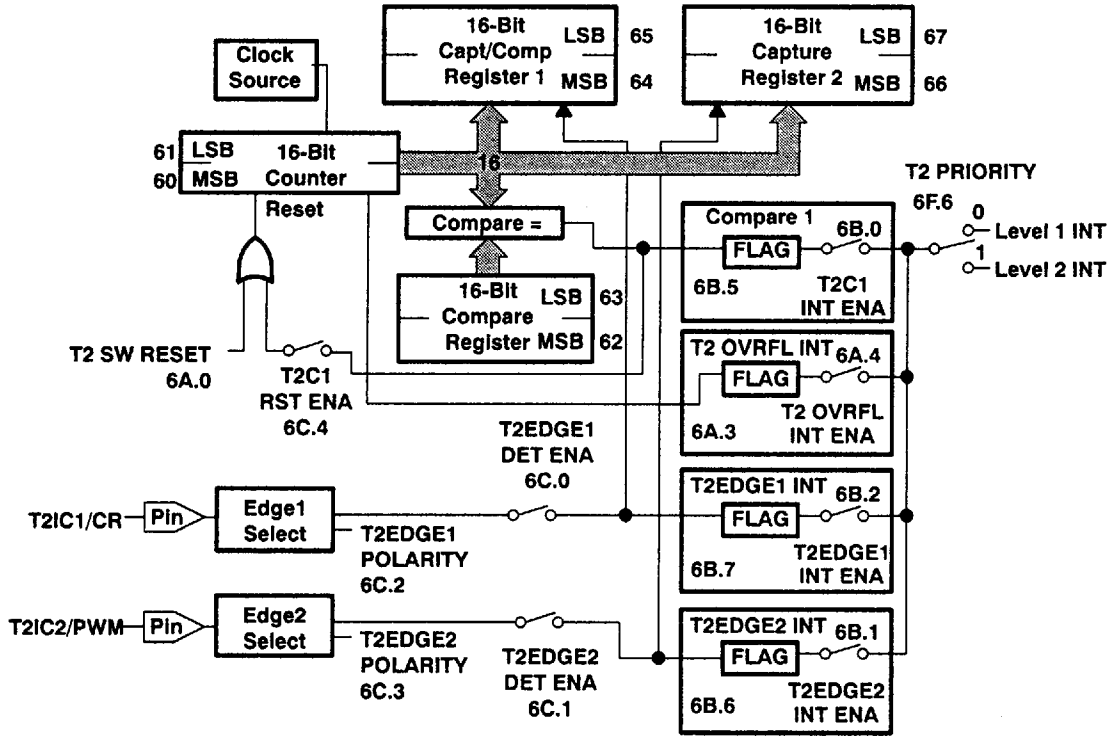

Figure 17. Timer 2— Dual Capture Mode

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Peripheral File Frame 6: Timer 2 Module Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1060h	P060	Bit 15			T2 Counter MSB				Bit 8	T2CNTR
1061h	P061	Bit 7			T2 Counter LSB				Bit 0	
1062h	P062	Bit 15			T2 Compare 1 Register MSB				Bit 8	T2C
1063h	P063	Bit 7			T2 Compare 1 Register LSB				Bit 0	
1064h	P064	Bit 15			T2 Capture 1/Compare 2 Register MSB				Bit 8	T2CC
1065h	P065	Bit 7			T2 Capture 1/Compare 2 Register LSB				Bit 0	
1066h	P066	Bit 15			T2 Capture Register 2 MSB				Bit 8	T2IC
1067h	P067	Bit 7			T2 Capture Register 2 LSB				Bit 0	
1068h 1069h	P068 P069	Reserved								
106Ah	P06A	—	—	—	T2OVRFL INT ENA	T2OVRFL INT FLAG	T2INPUT SELECT1	T2INPUT SELECT0	T2 SW RESET	T2CTL1
Mode: Dual Compare										
106Bh	P06B	T2EDGE1 INT FLAG	T2C2 INT FLAG	T2C1 INT FLAG	—	—	T2EDGE1 INT ENA	T2C2 INT ENA	T2C1 INT ENA	T2CTL2
106Ch	P06C	T2 MODE = 0	T2C1 OUT ENA	T2C2 OUT ENA	T2C1 RST ENA	T2EDGE1 OUT ENA	T2EDGE1 POLARITY	T2EDGE1 RST ENA	T2EDGE1 DET ENA	T2CTL3
Mode: Dual Capture										
106Bh	P06B	T2EDGE1 INT FLAG	T2EDGE2 INT FLAG	T2C1 INT FLAG	—	—	T2EDGE1 INT ENA	T2EDGE2 INT ENA	T2C1 INT ENA	T2CTL2
106Ch	P06C	T2 MODE = 1	—	—	T2C1 RST ENA	T2EDGE2 POLARITY	T2EDGE1 POLARITY	T2EDGE2 DET ENA	T2EDGE1 DET ENA	T2CTL3
106Dh	P06D	—	—	—	—	T2EVT DATA IN	T2EVT DATA OUT	T2EVT FUNCTION	T2EVT DATA DIR	T2PC1
106Eh	P06E	T2IC2/PWM DATA IN	T2IC2/PWM DATA OUT	T2IC2/PWM FUNCTION	T2IC2/PWM DATA DIR	T2IC1/CR DATA IN	T2IC1/CR DATA OUT	T2IC1/CR FUNCTION	T2IC1/CR DATA DIR	T2PC2
106Fh	P06F	**T2 STEST**	**T2 PRIORITY**	—	—	—	—	—	—	T2PRI

The formulas in Figure 18 show the calculations for the resulting time, given values in the compare registers T2C and T2CC.

$$\text{time} = \left(\frac{4}{\text{CLKIN}}\right) (\text{prescale}) (\text{compare} + 1)$$

or

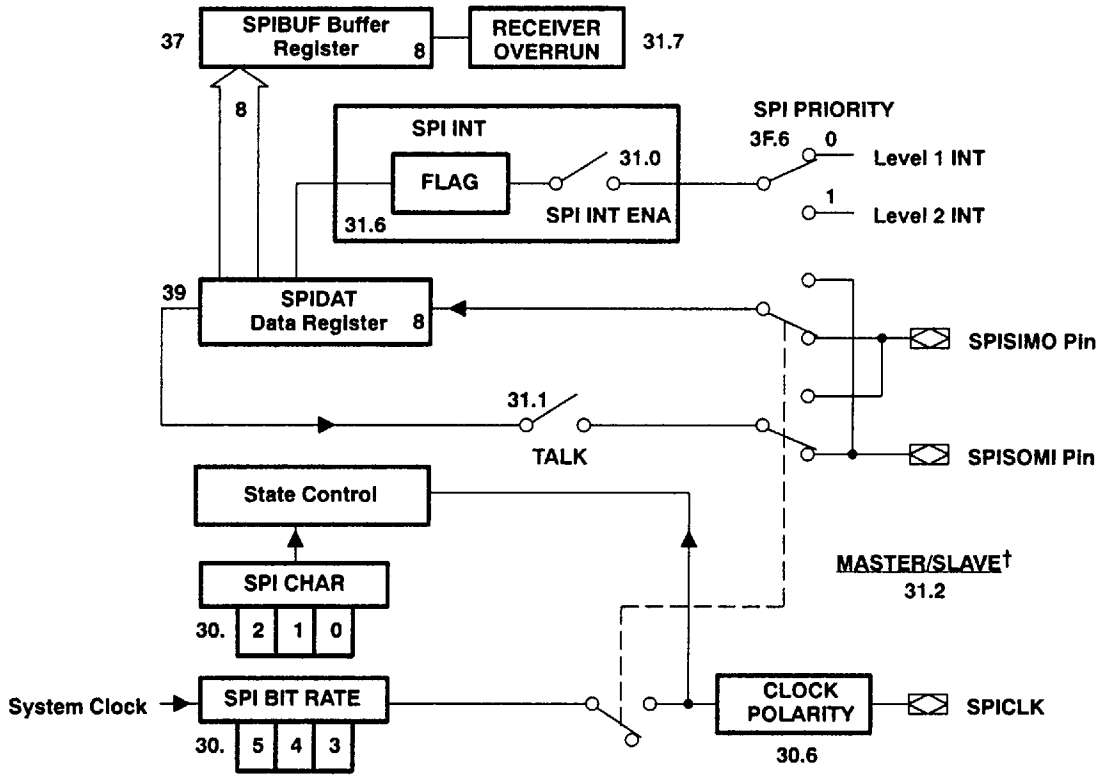
$$\text{time} = t_c (\text{prescale}) (\text{compare} + 1)$$

Figure 18. Timer 2 Compare Register Formulas

serial peripheral interface (SPI)

The Serial Peripheral Interface (SPI) is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight data bits) to be shifted into or out of the device at a programmed bit transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion using devices such as shift registers, display drivers, A/D converters, etc. Multiprocessor communications are also supported by the master/slave operation of the SPI.

Three I/O pins are associated with the SPI. These include the SPI slave-in master-out (SPISIMO), SPI slave-out master-in (SPISOMI), and SPI serial clock (SPICLK). These I/O pins can be configured for three-wire full-duplex transmit/receive or two-wire receive or transmit only. Any of these three pins not used in an SPI application may be individually configured as general purpose digital I/O pins controlled by SPIPC1 and SPIPC2.



† Diagram shown in SLAVE mode.

Figure 19. SPI Block Diagram†

A variety of multiprocessor configurations can be supported, ranging from single master with multiple slaves to multi-master systems. General purpose I/O pins can be used to implement the slave enables and multi-master hardware handshakes between microcontrollers in the network.

The MASTER/SLAVE bit of the SPICTL control register determines if the SPI operates in the master or slave mode. Master or slave data transmission can be disabled by writing a zero to the TALK bit of the SPICTL control register, forming a two-wire receive-only network (SPICLK and data in).

In the **master mode** (MASTER/SLAVE = 1), the SPI provides the serial clock on the SPICLK pin for the entire serial communications network. The SPICCR register (SPI BIT RATE2, RATE1, RATE0) determines the bit transfer rate for the network, both transmit and receive. For any specific system clock frequency, there are eight data transfer rates that can be selected by these control bits. The data transfer rate is defined by selecting a one-of-eight divide-by of the system clock frequency (divide-by-2, -4, -8, -16, -32, -64, -128, and -256).

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$$\text{SPI Baud Rate} = \frac{\text{CLKIN}}{8 \times 2^{b}}$$

where b = bit rate in SPICCR bit 3, 4, 5 (range 0 – 7).

Data written to the SPIDAT register initiates data transmission on the SPISIMO pin, MSB of data transmitted first.Simultaneously, received data is shifted in through the SPISOMI pin into the SPIDAT register, and upon completion of transmitting the selected number of bits, the data is transferred to the SPIBUF (double buffered receiver) for reading by the CPU to permit new transactions to take place. Data is shifted into the SPI (the most significant bit first), there it is stored right-justified in the SPIBUF. To receive a character when operating as a master, data must be written to the SPIDAT to initiate the transaction. When the specified number of data bits have been shifted into or out of the SPIDAT register, the SPI INT FLAG bit is set and if the SPI INT ENA bit is set to one, an Interrupt is asserted.

In the **slave mode** (MASTER/SLAVE = 0), data shifts out on the SPISOMI pin and in on the SPISIMO pin. The SPICLK pin is used as the input for the serial shift clock, which is supplied from the external network master. The transfer rate is defined by the input clock on the SPICLK pin, which is supplied from the network master. The SPICLK input frequency should be no greater than system clock frequency divided by eight.

Data written to the SPIDAT register will be transmitted to the network when the SPICLK is received from the network master. To receive data, the SPI waits for the network master to send SPICLK and then shifts the data on the SPISIMO pin into the SPIDAT register. If data is to be transferred by the slave simultaneously, it must be written to the SPIDAT register prior to the beginning of SPICLK.

Compatibility with the broadest range of existing peripheral devices is provided by the SPI through its software programmable transmit/receive character length, bit transfer rate, and clock polarity. A character length from one to eight data bits is selected by writing to the SPICCR control register (SPI CHAR2, CHAR1, and CHAR0) to specifically match the peripheral's data length requirements, thereby not requiring the overhead of data bit padding during communications. Applications requiring more than eight bits of serial data use multiple back-to-back SPI operations.

External peripherals enable output data on either the rising or the falling edge of the serial clock, while latching incoming data on the opposite edge. The SPI supports data transfer using either of these approaches. The CLOCK POLARITY bit controls the steady-state or at-rest condition of the SPICLK signal. This bit affects both master and slave modes of operation. When CLOCK POLARITY is set to 1, the at-rest level of SPICLK is a logic 1 . Data is enabled at the output on the falling edge of SPICLK, and data is latched by the network master and slaves on the rising edge of SPICLK. When CLOCK POLARITY is set to 0, the at-rest level of SPICLK is a logic 0. Data is enabled for output on the rising edge of SPICLK, and data is latched by the network master on the falling edge of SPICLK.

Peripheral File Frame 3: Serial Peripheral Interface (SPI) Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1030h	P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
1031h	P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
1032h to 1036h	P032 to P036	Reserved								
1037h	P037	SPI Receive Data Buffer Register								SPIBUF
1038h	P038	Reserved								
1039h	P039	SPI Serial Data Register								SPIDAT
103Ah to 103Ch	P03A to P03C	Reserved								
103Dh	P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
103Eh	P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
103Fh	P03F	**SPI STEST**	**SPI PRIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI

serial communications interface (SCI)

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The Serial communications Interface (SCI) is a full-duplex serial I/O port that supports standard NRZ serial communications in a programmed data format (start bit, 1 to 8 data bits, parity even/odd/off, one or two stop bits) at a variety of programmable baud rates. High-speed isosynchronous communications, as well as standard asynchronous communications, are supported for interfacing to peripheral devices. The isosynchronous communications mode combines features of the asynchronous mode with a synchronizing clock signal. The isosynchronous mode has the same format as the asynchronous mode using start, stop, parity, and data bits, but it it uses one serial clock cycle per bit to achieve a much higher transmission speed. Multiprocessor communications using idle line wake-up and address bit wake-up protocols are also supported by the SCI transmit and receive hardware.

As shown in Figure 20, the SCI receiver and transmitter are double buffered to reduce the possibility of overwriting data prior to the previous data being read or transmitted from the SCI.

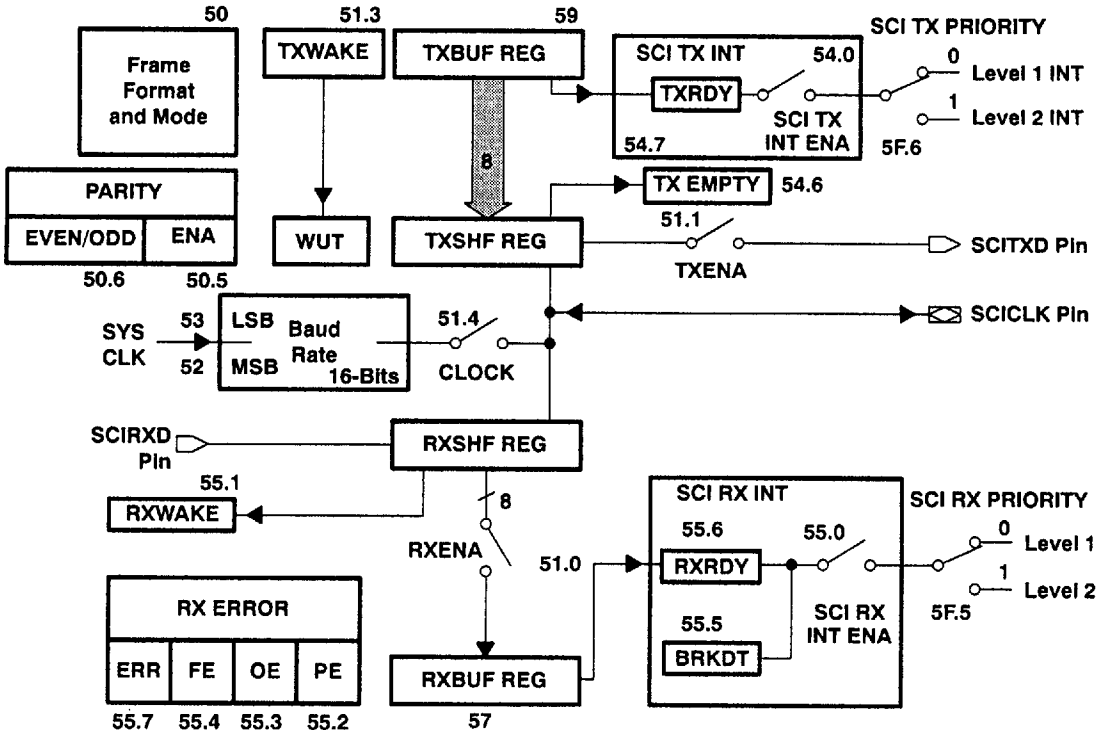

Figure 20. SCI Block Diagram

The SCI provides independent interrupt requests and vectors for the receiver and transmitter. Interrupts requested by the SCI receiver and SCI transmitter can be software programmed onto different priority levels by the SCI RX PRIORITY and SCI TX PRIORITY control bits. When SCI interrupt requests are made on the same level, the receiver always has higher priority than the transmitter to reduce the possibility of receiver overrun. An SCI TXINT interrupt is asserted whenever TXBUF is transferred to TXSHF. An SCI RXINT interrupt is asserted whenever the SCI receives a complete frame (RXSHF transfers to RXBUF) or when a break detect condition occurs (SCIRXD is low for 10 bit periods following a stop bit).

If the TMS370Cx5x has been placed in HALT or STANDBY low-power mode with the SCI RX INT ENA bit = 1, the detection of the start bit (one-to-zero transition) by the SCI receiver initiates receipt of the SCI input, exits the low power mode, activates the microcontroller (CPU, clocks, on-chip peripherals), and initiates execution of the SCI RXINT interrupt service routine. To ensure valid data receipt of the first frame, the baud rate must be slow enough for the SCI to sample for a valid start bit after exiting from the power down mode, or the first data byte must be ignored.

The SCI transmitter and receiver are functionally independent to support full-duplex communications; however, they use the same data format, baud rate, communications mode, and multiprocessor communications protocol. The SCICCR control register selects the transmit and receive data format. Figure 21 shows the SCI data format of one frame of information, which consists of an idle line (logic 1), one start bit (logic 0), one to eight data bits, an address bit (if in address bit wake-up mode), a parity bit (if enabled), and one or two stop bits (logic 1). The character length of one to eight data bits is selected by the SCI CHAR2, SCI CHAR1, and SCI CHAR0 control bits. Parity on/off is selected by PARITY ENABLE with the EVEN/ODD PARITY bit selecting the type. Parity generation and verification is performed in the SCI hardware, requiring no CPU calculation overhead. One or two stop bits for transmission are selected by the STOP BITS control bit. The receiver checks for one stop bit on incoming data.

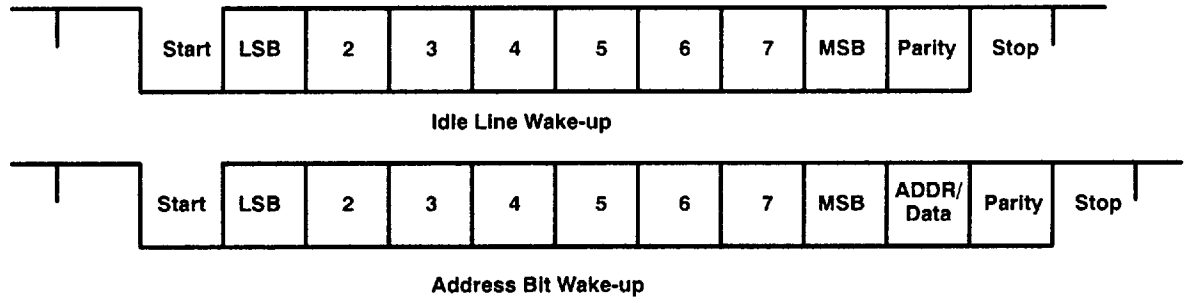

Figure 21. Frame Formats

The SCI communications mode is selected by the ASYNC/ISOSYNC control bit. The transmit and receive data format as described above are identical in both communication modes. In the **asynchronous mode** (ASYNC/ISOSYNC = 1), the external communications interface consists of the SCITXD and SCIRXD pins with an optional SCICLK input for driving the internal SCICLK. The transmit baud rate is 1/16 that of the SCICLK frequency. The receiver internally samples the data input at 16 times the bit rate. The receiver uses majority vote sampling on the seventh, eighth, and ninth SCICLK periods to determine the value of the start bit, data bits, parity, and first stop bit. Asynchronous data rates are supported up to 156K baud (SYSCLK/2^{21} to SYSCLK/32) at 20 MHz.

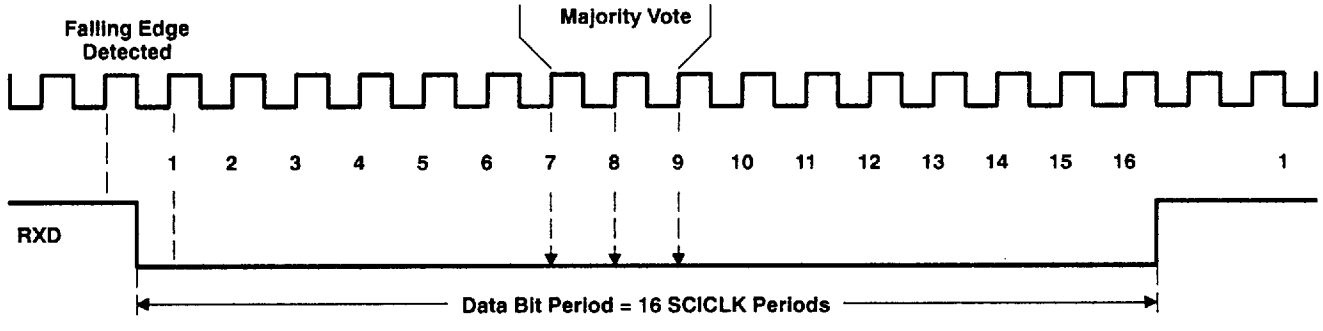

Figure 22. Asynchronous Mode

The **Isosynchronous mode** (ASYNC/ISOSYNC = 0) has the same format as the asynchronous mode, consisting of a start bit, one to eight data bits, an even/odd/no parity bit, and one or two stop bits, but uses an additional synchronizing clock to support high speed serial communications. The external system interface consists of the SCITXD and SCIRXD pins and a continuous synchronizing clock on on the SCICLK pin. Isosynchronous transmit and receive data is clocked at a rate equal to the SCICLK rate, and receiver values are read on a single sample basis. Isosynchronous data rates with synchronizing SCICLK are supported up to 2.5M baud (SYSCLK/2^{17} to SYSCLK/2) at 20 MHz.

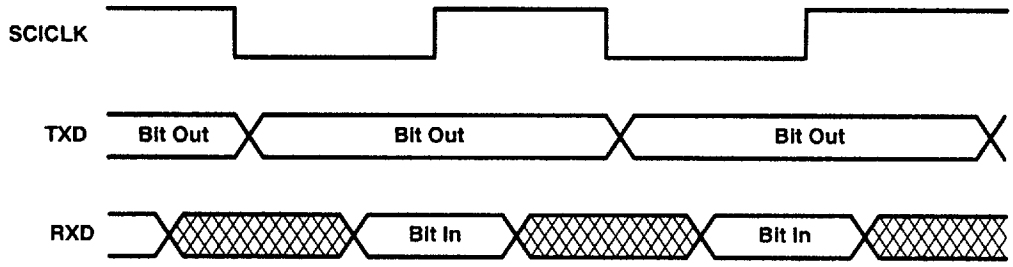

Figure 23. Isosynchronous Mode

The CLOCK bit in SCICTL determines whether the SCI clocking signal comes in from an external source through the SCICLK pin or goes out through SCICLK after generation in the integral baud rate timer. The isosynchronous mode baud rate equals the SCICLK rate; the asynchronous mode baud rate 1/16 the SCICLK rate. The maximum frequency of an external clock source can be no greater than 1/10 the system clock frequency. The frequency of the SCICLK when generated by the internal baud rate timer given by the formula.

$$\text{SCICLK} = \frac{\text{CLKIN}}{8(\text{Baud Rate Reg} + 1)}$$

The baud rate using the internal clock equals the SCICLK rate in the isosynchronous mode and equals 1/16 the SCICLK in the asynchronous mode. The 16-bit baud rate register allows the selection of many different standard baud rates.

$$\text{Asynchronous Baud Rate} = \frac{\text{CLKIN}}{128(\text{Baud Rate Reg} + 1)}$$

$$\text{Isosynchronous Baud Rate} = \frac{\text{CLKIN}}{8(\text{Baud Rate Reg} + 1)}$$

NOTE

When an external serial clock signal is used, the maximum SCICLK frequency is CLKIN/40.

In both asynchronous and isosynchronous modes, if the transmitter is enabled (TXENA = 1), SCI transmission is initiated following a CPU write to the TXBUF register. This sets TX EMPTY to 0; TXSHF is loaded from TXBUF, TXRDY flag is set to 1, and if SCI TX INT ENA is set to 1, SCI transmit interrupt (TXINT) will be asserted. Another write may then be performed to the TXBUF; if not, the transmitter idles (SCITXD outputs continuous high), and TX EMPTY is set to 1 (both TXBUF and TXSHF are empty) until the next write to TXBUF.

In both asynchronous and isosynchronous modes, when a frame is fully received, RXBUF is loaded from RXSHF, the error status bits are set accordingly, RXRDY flag is set to 1, and if SCI RX INT ENA is set to 1, an SCI receiver interrupt (RXINT) will be asserted. The SCI receiver performs extensive error checking during data bit reception and provides individual error flags for parity error (PE), overrun error (OE), framing error (FE), and break detect (BRKDT) for application program querying.

The SCI supports two multiprocessor communication formats to allow efficient transfer of information between many microcontrollers on the same serial data link. Information is typically transferred as a block of data from a source to a destination, with the destination address identified at the beginning of the block. The SCI has the ability to inhibit all SCI receiver flags and interrupts until a start of a block of data (a destination address) is identified. When a block start is identified, the SCI initiates the following sequence for both multiprocessor communication formats:

1. The serial port wakes up at the start of the block and receives the first frame (containing the destination address).
2. A software routine responds to the SCI receiver interrupt and checks the incoming byte against its address byte stored in memory.
3. If the block is addressed to the microcontroller, the SCI remains active and the CPU reads the rest of the block. If the address does not compare, the software routine puts the serial port to sleep and the SCI will inhibit all SCI receiver flags and interrupts until the next block start.

To provide system flexibility, the SCI, in both asynchronous and isosynchronous modes, recognizes the idle line wake-up and address bit wake-up multiprocessor protocols. The multiprocessor protocol is selected by the ADDRESS/IDLE WUP control bit in the SCICCR register. Both protocols use the SLEEP and TXWAKE bits to control the receive and transmit features of the wake-up mode, and the RXWAKE status bit to provide the receiver wake-up condition.

In **idle line wake-up**, blocks are separated by having a longer idle time (logic one) between the blocks than between frames within the blocks. As shown in Figure 24, an idle time of 10 or more bits after a frame indicates a start of a new block and wakes up all receivers. Under software control, all receivers that do not recognize the address in the first frame of the message ignore the rest of the message and await the next idle line. The SCI transmitter allows an idle time of exactly one frame to be transmitted to indicate the start of the next block to maintain serial data link efficiency by minimizing the idle time between block starts. Idle line wake-up protocol has no overhead within the message frames and is typically used when transferring large blocks of data.

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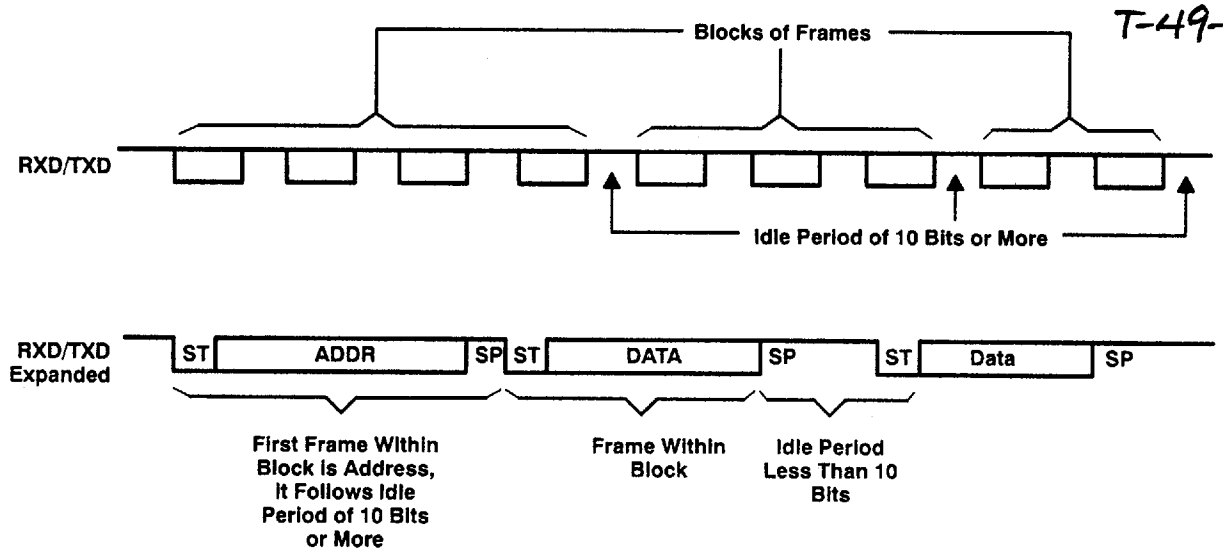

Figure 24. Idle Line Multiprocessor Mode

In **address bit wake-up**, each frame has an extra bit, the ADDR/DATA bit, positioned just before the parity bit (if used). As shown in Figure 25, block starts are distinguished by the ADDR/DATA bit set to 1 in the first frame of the block and all subsequent frames of the block have the ADDR/DATA bit set to 0. The start of the next block is identified by the next frame that has a 1 in ADDR/DATA. The idle line time is irrelevant in this protocol. All receivers wake up upon receiving a frame with ADDR/DATA set to 1. Under software control, all receivers that do not recognize their address in the first frame of the message ignore the rest of the message and await the next active ADDR/DATA bit. Address bit wake-up protocol eliminates interblock gaps and is efficient in transferring many small blocks of data.

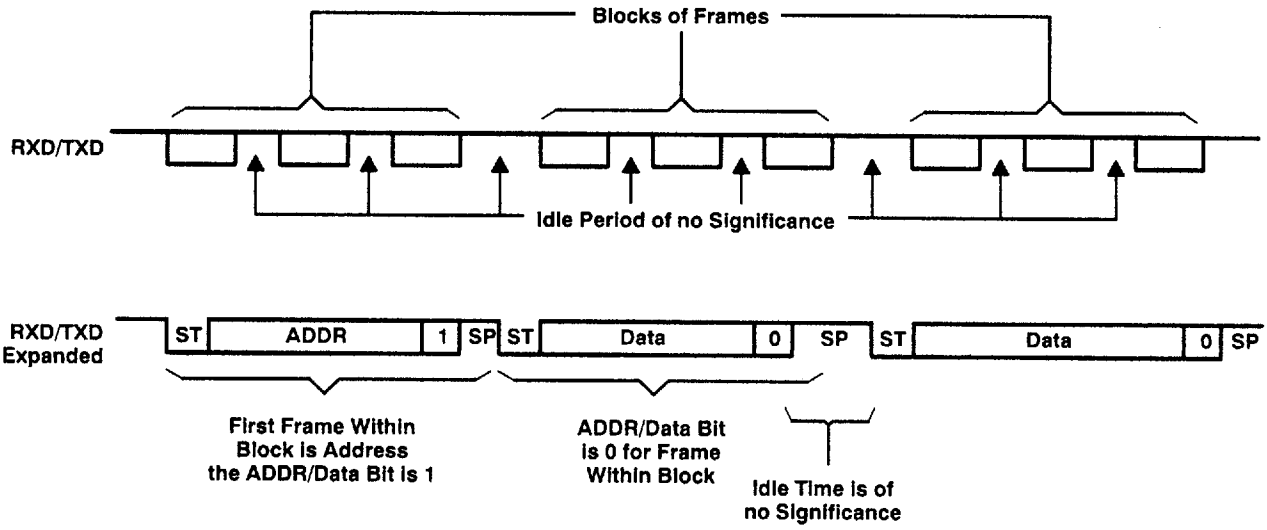

Figure 25. Address Bit Multiprocessor Mode

Peripheral File Frame 5: Serial Communication Interface (SCI) Control Registers

ADDR	PF	7	6	5	4	3	2	1	0	REG
1050h	P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
1051h	P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
1052h	P052	Bit 15	Baud Rate Select Register MSB						Bit 8	BAUD MSB
1053h	P053	Bit 7	Baud Rate Select Register LSB						Bit 0	BAUD LSB
1054h	P054	TXRDY	TX EMPTY	—	—	—	—	—	SCITX INT ENA	TXCTL
1055h	P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCIRX INT ENA	RXCTL
1056h	P056	Reserved								
1057h	P057	Receive Data Buffer Register								RXBUF
1058h	P058	Reserved								
1059h	P059	Transmit Data Buffer Register								TXBUF
105Ah	P05A	Reserved								
105Bh	P05B									
105Ch	P05C									
105Dh	P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
105Eh	P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
105Fh	P05F	**SCI STEST**	**SCI TX PRIORITY**	**SCI RX PRIORITY**	**SCI ESPEN**	—	—	—	—	SCIPRI

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analog-to-digital converter

The 8-bit analog-to-digital (A/D) converter provides the designer with eight multiplexed analog input channels. The A/D converter has internal sample and hold circuitry and uses a successive approximation conversion technique. The accuracy of the A/D conversion process is increased by providing separate analog positive supply and analog ground input pins (V_{CC3} and V_{SS3}). The V_{SS3} pin also provides the low reference voltage input for the conversion process.

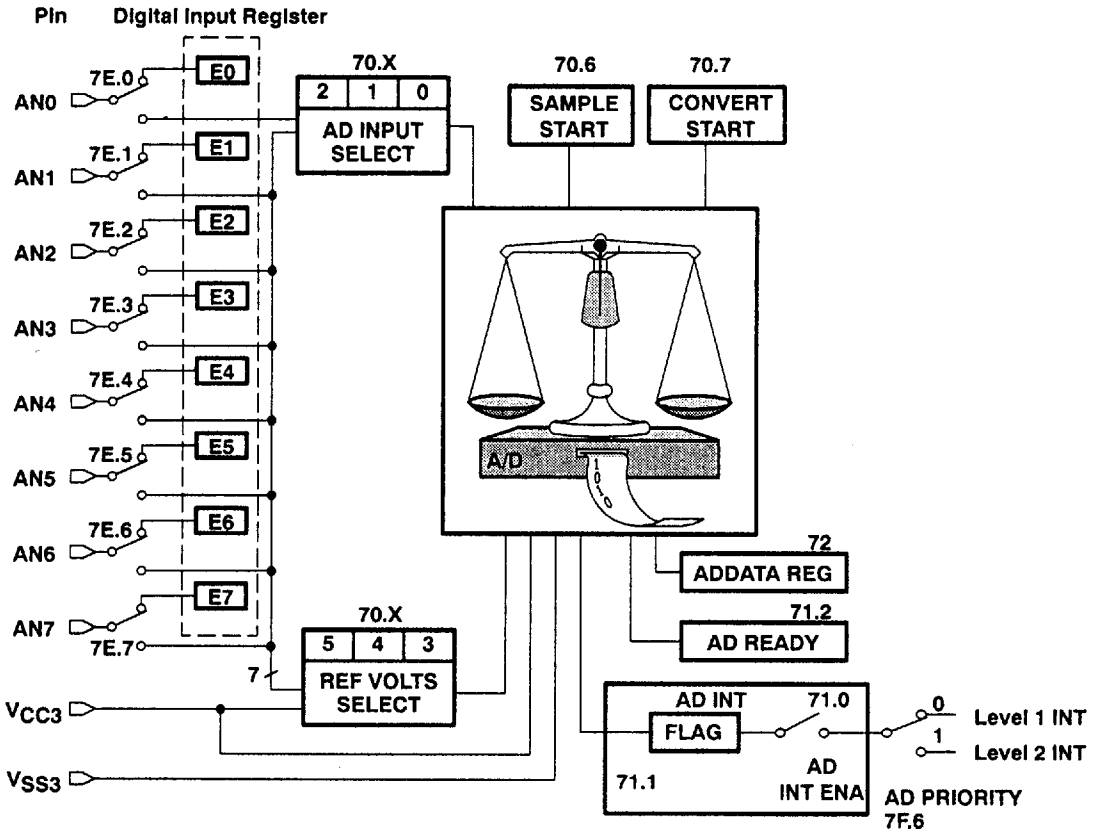

Figure 26. A/D Converter Block Diagram

The A/D converter high reference voltage input is software selectable as one of eight positive reference inputs, as shown in the table below. The A/D conversion process is ratiometric, using V_{SS3} and the software-selected high-reference voltage input as the limits for the selected analog input channel. An input voltage equal to or greater than the high reference input converts to FFh (full scale) with no overflow. An input voltage equal to or less than V_{SS3} converts to 00h. Ratiometric conversions allow analog inputs to be scaled against selected high reference inputs to achieve the greatest accuracy.

AD INPUT SELECT			ANALOG
SEL2	SEL1	SEL0	INPUT CHANNEL
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

REF VOLTS SELECT			HIGH REFERENCE
SEL2	SEL1	SEL0	INPUT
0	0	0	V_{CC3}
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

To read an A/D channel:

1. Write to the ADCTL peripheral file control register to:
   - Select the high reference voltage input (ADCTL.5-3).
   - Select the analog input channel for conversion (ADCTL.2-0).
   - Set the SAMPLE START bit to 1 (ADCTL.6).
2. Wait for the sample time to elapse.
3. Write to the ADCTL peripheral file control register to:
   - Set the CONVERT START bit to 1 and leave SAMPLE START bit set to 1.
4. Wait for either the interrupt flag to be set or the A/D interrupt to occur.
5. Read the conversion value from ADDATA when AD INT FLAG is set to 1 or the A/D interrupt occurs.
6. Clear the interrupt flag (ADSTAT.1).

To provide the designer with the flexibility to optimize the A/D conversion process with both high and low impedance sources, the sample time is independently defined by the application program. At the completion of the sample time, the conversion is initiated by settling the CONVERT START and SAMPLE START bits to 1. Eighteen clock cycles after the CONVERT START bit is set to 1, the CONVERT START and SAMPLE START bits will both be set to 0 by the A/D converter, indicating the conversion has started and the analog input signal can be removed. The AD READY bit is set to 0 by the A/D converter to indicate a conversion is in progress. The conversion is complete 164 system clock cycles after it is initiated by setting the CONVERT START bit to 1, and the result is located in the ADDATA result register. Upon completion of the conversion, the AD INT FLAG bit is set, and if the AD INT ENA bit is set to 1 an interrupt will be asserted.

The A/D converter has eight bits of resolution with absolute accuracy of plus or minus one LSB, with (high Reference Voltage – V_{SS3}) = 5 V.

To maximize I/O control capability, all analog input pins not used for an analog input or high reference voltage input to be individually configured as general purpose digital input pins. The control and input data values are contained in the ADENA and ADIN peripheral file control registers.

Peripheral File Frame 7: A-to-D Converter Control Registers

ADDR	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
1070h	P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
1071h	P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
1072h	P072	A-to-D Conversion Data Register								ADDATA
1073h to 107Ch	P073 to P07C	Reserved								
107Dh	P07D	Port E Data Input Register								ADIN
107Eh	P07E	Port E Input Enable Register								ADENA
107Fh	P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

instruction set

The TMS370x5x family instruction set consists of 64 instructions that control input, output, data manipulations, data comparisons, and program flow. The instruction set is supported with fourteen addressing modes to provide the flexibility to optimize programs to the user's applications. For example, the MOV instruction has 27 operand combinations supported by its addressing modes.

ADDRESSING MODE	EXAMPLE		OPERATION
GENERAL:			
Implied	LDSP		(B) → (SP)
Register	MOV	R5,R4	(R5) → (R4)
Peripheral	MOV	P025,A	(1025h) → A
Immediate	ADD	#123,R3	123 + (R3) → (R3)
PC Relative	JMP	offset	PCN + offset → (PC)
Stack Pointer Relative	MOV	2(SP),(A)	(2 + (SP)) → (A)
EXTENDED:			
Absolute Direct	MOV	A,1234	(A) → (1234)
Absolute Indexed	MOV	1234(B),A	(1234 + (B)) → (A)
Absolute Indirect	MOV	@R4,A	((R3:R4)) → (A)
Absolute Offset Indirect	MOV	12(R4),A	(12 + (R3:R4)) → (A)
Relative Direct	JMPL	1234	PCN + 1234 → (PC)
Relative Indexed	JMPL	1234(B)	PCN + 1234 + (B) → (PC)
Relative Indirect	JMPL	@R4	PCN + (R3:R4) → (PC)
Relative Offset Indirect	JMPL	12(R4)	PCN + 12 + (R3:R4) → (PC)

PCN = 16-bit address of next instruction.
(x) = Contents of memory at address x.
((x)) = Contents of memory location designated by contents at address x.

The CPU controls instruction execution by executing microinstructions from a dedicated control memory at a rate of one microinstruction per internal system clock cycle, t_c. The number of system clock cycles required to execute one assembly language instruction varies depending on the instruction complexity, operand addressing mode, and number of wait states. Instruction execution times are stated in terms of the number of integral system clock cycles per instruction. Instruction execution times vary from 5 to 63 internal system clock cycles, with most instructions requiring less than 10 cycles to complete.

Similarly, the number of bytes of program memory required to store an instruction will vary with instruction complexity and addressing mode. TMS370 instructions require from one to five bytes of program memory space, with most instructions occupying one or two bytes.

The *TMS370 Instruction Set Summary*, beginning on page 48, shows the instruction set, the addressing modes, the program memory byte length, and the execution cycle count for each instruction. The Addressing Mode entries are in the format of BYTE LENGTH/CYCLE COUNT. The following symbols and abbreviations are used:

SYMBOL	DEFINITION
s	Source Operand
A	Register A or R0 in Register File
Rs	Source Register in Register File
Ps	Source Register in Peripheral File
Rps	Source Register Pair (Rn, Rn – 1)
Rp	General Purpose Register Pair
iop8	8-bit Immediate Operand
off8	8-bit Signed Offset (label – PCN)
PC	Program Counter
SP	Stack Pointer
#	Immediate Operand
C	Status Register Carry Bit
( )	Contents of

SYMBOL	DEFINITION
d/D	Destination Operand (8-bit/16-bit)
B	Register B or R1 in Register File
Rd	Destination Register in Register File
Pd	Destination Register in Peripheral File
Rpd	Destination Register Pair (Rn, Rn – 1)
label	16-bit Label
iop16	16-bit Immediate Operand
off16	16-bit Signed Offset
PCN	16-bit Address of Next Instruction
ST	Status Register
@	Extended Addressing Operand (Direct, Indirect, Indexed)
→	Is Assigned to

TMS370 Instruction Set Summary

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
ADC	B, __	1/8										Add with Carry
	Rs, __	2/7	2/7	3/9								(s) + (d) + (C) → (d)
	#iop8, __	2/6	2/6	3/8								
ADD	B, __	1/8										Add
	Rs, __	2/7	2/7	3/9								(s) + (d) → (d)
	#iop8, __	2/6	2/6	3/8								
AND	A, __				2/9							And
	B, __	1/8			2/9							(s). AND. (d) → (d)
	Rs, __	2/7	2/7	3/9								
	#iop8, __	2/6	2/6	3/8	3/10							
BR						3/9	2/8	3/11	4/16			Branch; D → (PC)
BTJO†	A, __,off8				3/10							Bit Test and Jump If One
	B, __,off8	2/10			3/10							If (s). AND. (d) ≠ 0 then
	Rs, __,off8	3/9	3/9	4/11								PCN + offset → (PC)
	#iop8, __,off8	3/8	3/8	4/10	4/11							
BTJZ†	A, __,off8				3/10							Bit Test and Jump If Zero
	B, __,off8	2/10			3/10							If (s).AND.(not d) ≠ 0 then
	Rs, __,off8	3/9	3/9	4/11								PCN + offset → (PC)
	#iop8, __,off8	3/8	3/8	4/10	4/11							
CALL	__					3/13	2/12	3/15	4/20			Call; Push PCN, D → (PC)
CALLR	__					3/15	2/14	3/17	4/22			Call Relative
												Push PCN, PCN + (d) → (PC)
CLR	__	1/8	1/8	2/6								Clear; 0 → (d)
CLRC											1/19	Clear Carry; 0 → (C)
CMP	__,A					3/11	2/10	3/13	4/18	2/8		Compare
	B, __	1/8										(d) – (s) computed and
	Rs, __	2/7	2/7	3/9								Status Register flags set
	#iop8, __	2/6	2/6	3/8								
CMPBIT	__			3/8	3/10							Complement Bit
CMPL	__	1/8	1/8	2/6								Two's complement;
												0100h – (s) → (d)
DAC	B, __	1/10										Decimal Add with Carry
	Rs, __	2/9	2/9	3/11								(s) + (d) + (C) → (d) (BCD)
	#iop8, __	2/8	2/8	3/10								
DEC	__	1/8	1/8	2/6								Decrement; (d) – 1 → (d)
DINT											2/6	Disable Interrupt; 00 → (ST)
DIV	Rs, __	3/55–63‡										Integer Divide; 16 by 8-bit
												A:B/Rs → A(=quo), B(=rem)
												# cycles depends on operands
DJNZ†	__,off8	2/10	2/10	3/8								Decrement and Jump If Not 0
												(d) – 1 → (d); if (d) .NE. 0
												then PCN + offset → (PC)

† Add 2 to cycle count if jump is taken.
‡ Actual number of cycles is 14 if the quotient is greater than 8 bits (overflow condition).

TMS370 Instruction Set Summary (continued)

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
DSB	B, __	1/10										Decimal Subtract with Borrow
	RS, __	2/9	2/9	3/11								(d) – (s) – 1 + (C) → (d) (BCD)
	#iop8, __	2/8	2/8	3/10								
EINT											2/6	Enable Interrupts; 0Ch → (ST)
EINTH											2/6	EINT High Priority; 04h → (ST)
EINTL											2/6	EINT Low Priority; 08h → (ST)
IDLE											1/6	Idle Until Interrupt, Low Power entry
INC	__	1/8	1/8	2/6								Increment; (d) + 1 → (d)
INCW	#off8, __			3/11								Increment Word (Rp) + offset → (Rp)
INV	__	1/8	1/8	2/6								Invert; .NOT. (d) → (d)
JMP	__										2/7	Jump; PCN + offset8 → (PC)
JMPL	__					3/9	2/8	3/11	4/16			Jump; PCN + D → (PC)
Jcnd†												Jump Conditional
JN											2/5	Negative
JZ											2/5	Zero
JC											2/5	Carry
JP											2/5	Positive
JPZ											2/5	Positive or Zero
JNZ											2/5	Negative or Zero
JNC											2/5	No Carry
JV											2/5	Overflow, signed
JNV											2/5	No Overlfow, signed
JGE											2/5	Greater Than or Equal, signed
JL											2/5	Less Than, signed
JG											2/5	Greater Than, Signed
JLE											2/5	Less Than or Equal, signed
JL0											2/5	Lower Value
JHS											2/5	Higher or Same
JBIT0†	__			4/10	4/11							Jump If Bit = 0
JBIT1 †	__			4/10	4/11							Jump If Bit = 1
LDSP											1/7	Load Stack Pointer; (B) → (SP)
LDST	#iop8										2/6	Load ST Register; (s) → (STP)
MOV	A, __		1/9	2/7	2/8	3/10	2/9	3/12	4/17	2/7		Move; (s) → (d)
	__, A		1/8	2/7	2/8	3/10	2/9	3/12	4/17	2/7		
	B, __	1/8		2/7	2/8							
	Rs, __	2/7	2/7	3/9	3/10							
	Ps, __	2/8	2/8	3/10								
	#iop8, __	2/6	2/6	3/8	3/10							
MOVW	Rps, __			3/12								Move Word; 16-bit operands (s) → (d)
	#iop16, __			4/13								
	#iop16(B), __			4/15								
	#off8(Rp), __			5/20								

† Add 2 to cycle count if jump is taken.

TMS370 Instruction Set Summary (concluded)

OPERATION		ADDRESSING MODES										DESCRIPTION
		DIRECT				EXTENDED						
		A	B	Rd	Pd	label	@Rp	label(B)	off8(Rp)	off8(SP)	OTHER	
MPY	B, __	1/47										Multiply
	RS, __	2/46	2/46	3/48								(s) × (d) → (A:B)
	#iop8, __	2/45	2/45	3/47								A = MSB, B = LSB
NOP											1/7	NOP; (PC) +1 → (PC)
OR	A, __				2/9							OR
	B, __	1/8			2/9							(s) .OR. (d) → (d)
	Rs, __	2/7	2/7	3/9								
	#iop8, __	2/6	2/6	3/8	3/10							
POP	__	1/9	1/9	2/7							1/8	Pop Top of Stack
												((SP)) → (d); (SP) – 1 → (SP)
PUSH	__	1/9	1/9	2/7							1/8	Push onto Stack
												(SP) + 1 → (SP); (s) → ((SP))
RL	__	1/8	1/8	2/6								Rotate Left
RLC	__	1/8	1/8	2/6								Rotate Left Through Carry
RR	__	1/8	1/8	2/6								Rotate Right
RRC	__	1/8	1/8	2/6								Rotate Right Through Carry
RTI											1/12	Return from Interrupt
												Pop PC, Pop ST
RTS											1/9	Return from Subroutine, Pop PC
SBIT0	__			3/8	3/10							Set Bit to 0
SBIT1	__			3/8	3/10							Set BIT to 1
SETC											1/7	Set Carry; A0h → (ST)
SBB	B, __	1/8										Subtract with Borrow
	Rs, __	2/7	2/7	3/9								(d) – (s) – 1 + (C) → (d)
	#iop8, __	2/6	2/6	3/8								
STSP											1/8	Store Stack Pointer; (SP) → (B)
SUB	B, __	1/8										Subtract
	Rs, __	2/7	2/7	3/9								(d) – (s) → (d)
	#iop8, __	2/6	2/6	3/8								
SWAP	__	1/11	1/11	2/9								Swap Nibbles
												s(7–4,3–0) → d(3–0,7–4)
TRAPn											1/14	Trap to Subroutine; Push PCN;
												Vector n → (PC)
TST	__	1/9	1/10									Test; Set flags from register
XCHB	__	1/10	1/10	2/8								Exchange B; (B) ↔ (d)
XOR	A, __				2/9							Exclusive OR
	B, __	1/8			2/9							(s) .XOR. (d) → (d)
	Rs, __	2/7	2/7	3/9								
	#iop8, __	2/6	2/6	3/8	3/10							

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TMS370 Family OPCODE/Instruction Map

SECOND NIBBLE \ FIRST NIBBLE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP ra 2/7							INCW #n,Rd 3/11	MOV Ps,A 2/8			CLRC TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV n(SP),A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rn 2/6	TRAP 13 1/14	MOV A,n(SP) 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rn 2/6	TRAP 12 1/14	CMP n(SP),A 2/.8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rn 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A 3/9	BTJO #n,A 3/8	BTJO Rs,B 3/9	BTJO Rs,Rd 4/11	BTJO #n,B 3/8	BTJO B,A 2/10	BTJO #n,Rd 4/10	BTJO A,Pd 3/11	BTJO B,Pd 3/10	BTJO #n,Pd 4/11	XCHB A 1/10	XCHB B/ TESTB 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs,A 3/9	BTJZ #n,A 3/8	BTJZ Rs,B 3/9	BTJZ Rs,Rd 4/11	BTJZ #n,B 3/8	BTJZ B,A 2/10	BTJZ #n,Rd 4/10	BTJZ A,Pd 3/10	BTJZ B,Pd 3/10	BTJZ #n,Pd 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16(B),Rd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rs 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL @Rd 2/8	JMPL lab(B) 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV lab,A 3/10	MOV @Rs,A 2/9	MOV lab(B),A 3/12	DJNZ A,ra 2/10	DJNZ B,ra 2/10	DJNZ Rn,ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A,lab 3/10	MOV A,@Rd 2/9	MOV A,lab(B) 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rn 2/6	TRAP 4 1/14	PUSH ST 1/8
C	JNV ra 2/5	MPY Rs, A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rd 3/47	BR lab 3/9	BR @Rd 2/8	BR lab(B) 3/11	RR A 1/8	RR B 1/8	RR Rn 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP lab,A 3/11	CMP @Rs,A 2/10	CMP lab(B),A 3/15	RRC A 1/8	RRC B 1/8	RRC Rn 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL @Rd 2/12	CALL lab(B) 3/15	RL A 1/8	RL B 1/8	RL Rn 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR @Rd 2/14	CALLR lab(B) 3/17	RLC A 1/8	RLC B 1/8	RLC Rn 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

	E	F
8	MOVW n(Rn) 4/15	DIV Rn,A 3/14-63
9	JMPL n(Rn) 4/16	
A	MOV n(Rn),A 4/17	
B	MOV A,n(Rn) 4/17	
C	BR n(Rn) 4/16	
D	CMP n(Rn) 4/18	
E	CALL n(Rn) 4/20	
F	CALLR n(R) 4/22	

ra — relative address
Rn — Register
Rs — Register containing source byte
Rd — Register containing destination byte
Ps — Peripheral register containing source byte
Pd — Peripheral register containing destination byte
Pn — Peripheral register
#n — Immediate 8-bit number
#16 — Immediate 16-bit number
lab — 16-bit label
@Rn — 16-bit address of contents of register pair

development system support

The TMS370 family development support tools include an Assembler, a C-Compiler, a Linker, an In-Circuit emulator (XDS – eXtended Development Support), and an EEPROM/UVEPROM programmer.

- Assembler/Linker (Part No. TMDS3740810-02 for PC, Part No. TMDS3740210-08 for VAX™/VMS™, Part No. TMDS3740510-09 for Sun-3™ or Sun-4™)
  - — Extensive macro capability.
  - — High-speed operation.
  - — Format conversion utilities available for popular formats.
- ANSI C-Compiler (Part No. TMDS3740815-02 for PC, Part No. TMDS3740215-08 for VAX™/VMS™, Part No. TMDS3740515-09 for Sun-3™ or Sun-4™)
  - — Generates assembly code of the TMS370 that can be easily inspected.
  - — The compilation, assembly, and linking steps can all be performed with a single command.
  - — Enables the user to directly reference the TMS370's port registers by using a naming convention.
  - — Provides flexibility in specifying the storage for data objects.
  - — C functions and assembly functions can be easily interfaced.
- XDS/11 (eXtended Development Support) In-Circuit Emulator (Part Number TMDS3761111– For PC)
  - — PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment.
  - — Symbolic debugging.
  - — Execute single/multiple instructions, single/multiple statements, until/while condition, or at full speed until breakpoint.
  - — The user needs to provide a regulated 5-V power supply with a 3-A current capability.
- XDS/22 (eXtended Development Support) In-Circuit Emulator (Part Number TMDS3762210 – For PC)
  - — Contains all of the features of the XDS/11 described above but does not require an external power supply.
  - — Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly.
  - — Allows break points to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.
  - — Provides timers fo analyzing total and average time in routines.
  - — Contains an eight line logic probe for adding visibility of external signals to the breakpoint qualifier and to the trace display.
- EEPROM/EPROM Programmer
  - — Base (Part No. TMDS3760500 – base only, requires programmer head)
    - – Single unit head (Part No. TMDS3780510).
    - – Gang programmer head (Part No. TMDS3780521) supports programming 16 TMS370Cx5x devices in parallel.
  - — PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment.
- Design Kit (Part No. TMDS3770110 – For PC)
  - — Includes TMS370 Application Board and TMS370 Assembler diskette and documentation.
  - — Supports quick evaluation of TMS370 functionality.
  - — Capability to upload and download code.
  - — Capability to execute programs and software routines, and to single-step executable instructions.
  - — Software breakpoints to halt program execution at selected addresses.
  - — Wire-wrap prototype area.
  - — Reverse assembler.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1}, V_{CC2}, V_{CC3} (see Note 3) ..... – 0.6 V to 7 V
Input voltage range, All pins except MC ..... – 0.6 V to 7 V
MC ..... – 0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ ..... ±20 mA
Continuous output current per buffer, I_O (V_O = 0 to V_{CC})‡ ..... ±10 mA
Maximum I_{CC} current ..... 170 mA
Maximum I_{SS} current ..... –170 mA
Continuous power dissipation ..... 1 W
Storage temperature range ..... – 65°C to 150 °C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer may affect the levels on other buffers.

recommended operating conditions (see note 3)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC1}	Digital logic supply voltage		4.5	5	5.5	V
V_{CC1}	RAM data retention supply voltage (see Note 4)		3		5.5	V
V_{CC2}	Digital I/O supply voltage		4.5	5	5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS2}	Digital I/O supply ground		– 0.3	0	0.3	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{RESET}$	2		V_{CC}	V
		MC (non-WPO mode)	V_{CC} – 0.3		V_{CC}+0.3	
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		$\overline{RESET}$	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage (see Note 5)	EEPROM write protect override	11.7	12	13	V
		Microprocessor	V_{CC} – 0.3		V_{CC}+0.3	
		Microcomputer	V_{SS}		0.3	
		EPROM programming voltage (V_{PP})	12	12.5	13	
T_A	Operating free-air temperature	A version	– 40		85	°C
		L version	0		70	°C

NOTES: 3. All voltage values are with respect to V_{SS1}.
4. $\overline{RESET}$ is externally released while V_{CC} is within the recommended operating range of 4.5 V to 5.5 V and externally activated when $V_{CC} < 4.5$ or $V_{CC} > 5.5$ V. RAM data retention is valid throughout the 2 MHz-20 MHz frequency range. An active $\overline{RESET}$ initializes (clears) RAM locations 0000h and 0001h.
5. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin 2 µs before the $\overline{RESET}$ pin goes inactive (high). The WPO mode may be selected anytime a sufficient voltage is present on the MC pin.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	Ports A, B, C, D, and $\overline{RESET}$	I_{OL} = 2 mA			0.4	V
		Other outputs	I_{OL} = 1.4 mA			0.4	
V_{OH}	High-level output voltage		I_{OH} = – 50 µA	0.9 V_{CC}			V
			I_{OH} = – 2 mA	2.4			
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ V_{CC} – 0.3			50	
			V_{CC} – 0.3 V ≤ V_I ≤ V_{CC} + 0.3 V			10	
			V_{CC}+0.3 V < V_I ≤ 13 V			650	
		I/O pins	0V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current	Ports A, B, C, D and $\overline{RESET}$	V_{OL} = 0.4 V	2			mA
		Other outputs	V_{OL} = 0.4 V	1.4			
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC}	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (Operating mode) Osc Power bit = 0 (see Note 8)	TMS370Cx50, TMS370Cx52	Notes 6 and 7 CLKIN = 20 MHz		30	45	mA
		TMS370Cx56			35	56	
		TMS370Cx50, TMS370Cx52	Notes 6 and 7 CLKIN = 12 MHz		20	30	
		TMS370Cx56			22	36	
		TMS370Cx5x	Notes 6 and 7 CLKIN = 2 MHz		7	11	
I_{CC}	Supply current (Standby mode) Osc Power bit = 0 (see Note 9)		Notes 6 and 7 CLKIN = 20 MHz		12	17	mA
			Notes 6 and 7 CLKIN = 12 MHz		8	11	
			Notes 6 and 7 CLKIN = 2 MHz		2.5	3.5	
I_{CC}	Supply current (Standby mode) Osc Power bit = 1 (see Note 10)		Notes 6 and 7 CLKIN = 12 MHz		6	8.6	mA
			Notes 6 and 7 CLKIN = 2 MHz		2	3	
I_{CC}	Supply current (Halt mode)		Note 6 XTAL2/CLKIN < 0.2 V		2	30	µA

NOTES: 6. Single chip mode, ports configured as inputs, or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
7. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Currents may be higher with a crystal oscillator. At 20 MHz this extra current = .01 mA × (total load capacitance + crystal capacitance in pF).
8. Maximum operating current for TMS370Cx50 and TMS370Cx52 = 1.9 (CLKIN) + 7 mA.
Maximum operating current for TMS370Cx56 = 2.5 (CLKIN) + 5.8 mA.
9. Maximum standby current for TMS370Cx5x = 0.75 (CLKIN) + 2 mA.
10. Maximum standby current for TMS370Cx5x = 0.56 (CLKIN) + 1.9 mA. (Osc power bit valid only from 2 MHz to 12 MHz.)

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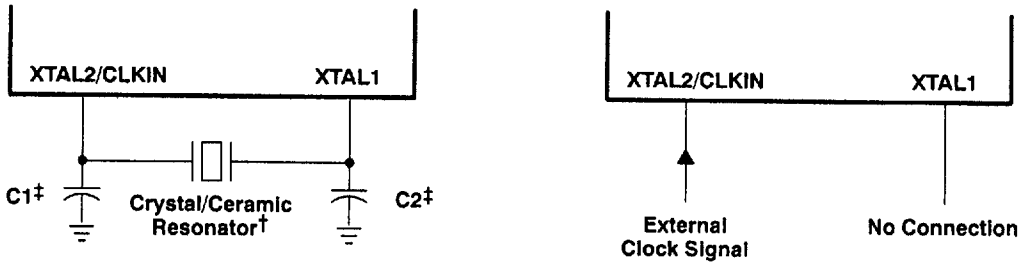
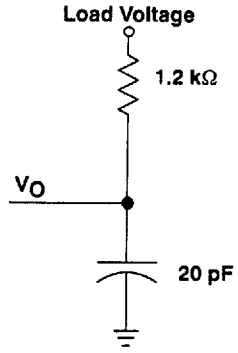
Recommended Crystal/Clock Connections



† The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
‡ The values of C1 and C2 should be the values recommended by the crystal/ceramic resonator manufacturer.

Typical Output Load Circuit§



Case 1: $V_O = V_{OH} = 2.4$ V; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4$ V; Load Voltage = 2.8 V for Ports A, B, C, D, and $\overline{\text{RESET}}$
Load Voltage = 2.1 for other Outputs

§ All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	R	Read
AR	Array	RXD	SCIRXD
B	Byte	S	Slave mode
CI	XTAL2/CLKIN	SCC	SCICLK
CO	CLKOUT	SIMO	SPISIMO
D	Data	SOMI	SPISOMI
E	$\overline{\text{EDS}}$	SPC	SPICLK
PGM	Program	W	Write
		WT	$\overline{\text{WAIT}}$

Lowercase subscripts and their meanings are:

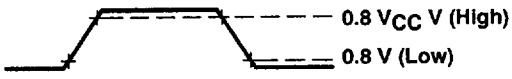
c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

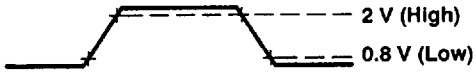
H	High	V	Valid
L	Low	Z	High Impedance

PARAMETER MEASUREMENT INFORMATION

All timings are measured between high and low measurement points as indicated in the figures below.



XTAL2/CLKIN Measurment Points



General Measurement Points

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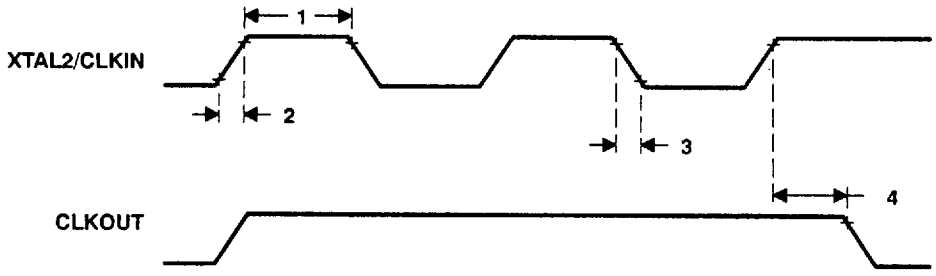
external clocking requirements†

NO.	PARAMETER		MIN	NOM	MAX	UNIT
1	$t_{w(CI)}$	XTAL2/CLKIN pulse duration (see Note 11)	20			ns
2	$t_{r(CI)}$	XTAL2/CLKIN rise time			30	ns
3	$t_{f(CI)}$	XTAL2/CLKIN fall time			30	ns
4	$t_{d(CIH-COL)}$	Delay time, XTAL2/CLKIN rise to CLKOUT fall			100	ns
	f_x	Crystal operating frequency	2		20	MHz

† For V_{IL} and V_{IH}, refer to "Recommended Operating Conditions".

NOTE 11: This pulse may be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

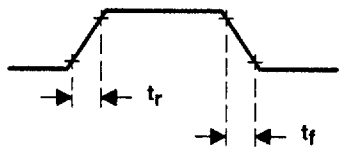
external clock timing



EXPANSION MODE OUTPUT

general purpose output signal switching time requirements

		MIN	NOM	MAX	UNIT
t_r Rise time	A, B, C, D, and $\overline{\text{RESET}}$		15		ns
	INT2 , INT3, SPISOMI, SPISIMO, SPICLK, T1IC/CR, T1PWM, T1EVT, T2IC1/CR, T2IC2/PWM, T2EVT, SCITXD, SCIRXD, SCICLK		30		ns
t_f Fall time	A, B, C, D, and $\overline{\text{RESET}}$		15		ns
	INT2, INT3, SPISOMI, SPISIMO, SPICLK, T1IC/CR, T1PWM, T1EVT, T2IC1/CR, T2IC2/PWM, T2EVT, SCITXD, SCIRXD, SCICLK		30		ns



recommended EPROM operating conditions for programming

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.5	6.0	V
V_{PP}	Supply voltage at MC pin	12	12.5	13	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)		30	50	mA
CLKIN	Operating crystal frequency	2		20	MHz

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(IEPGM)}$	Initial programming pulse (see Note 12)	0.95	1	1.05	ms
$t_{w(FEPGM)}$	Final programming pulse	2.85		78.75	ms

NOTE 12: Programming pulse is active when both EXE (EPCTL.0) and VPPS (EPCTL.6) are set.

recommended EEPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(PGM)B}$	Programming signal pulse duration to insure valid data is stored (byte mode)	10			ms
tw(PGM)AR	Programming signal pulse duration to insure valid data is stored (array mode)	20			ms

switching characteristics and timing requirements

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	CLKOUT (system clock) cycle time (see Note 13)	200	2000	ns
6	$t_{w(COL)}$	CLKOUT low pulse duration	$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(COH)}$	CLKOUT high pulse duration	$0.5t_c$	$0.5t_c+20$	ns
8	$t_{d(COL-A)}$	Delay time, CLKOUT low to address, R/$\overline{W}$, and $\overline{OCF}$ valid		$0.25t_c+40$	ns
9	$t_{v(A)}$	Address valid to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	$0.5t_c - 50$		ns
10	$t_{su(D)}$	Write data setup time to $\overline{EDS}$ high	$0.75t_c - 40$†		ns
11	$t_{h(EH-A)}$	Address, R/$\overline{W}$, and $\overline{OCF}$ hold time from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high	$0.5t_c - 40$		ns
12	$t_{h(EH-D)W}$	Write data hold time from $\overline{EDS}$ high	$0.75t_c+15$		ns
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)	$0.25t_c - 30$		ns
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)	$1.25t_c - 40$		ns
15	$t_{d(EL-DV)}$	Delay time, $\overline{EDS}$ low to read data valid		$t_c - 65$†	ns
16	$t_{(EH-D)R}$	Read data hold time from $\overline{EDS}$ high	0		ns
17	$t_{su(WT-COH)}$	$\overline{WAIT}$ setup time to CLKOUT high	$0.25t_c+75$‡		ns
18	$t_{h(COH-WT)}$	$\overline{WAIT}$ hold time from CLKOUT high	0		ns
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid		$0.5t_c - 70$	ns
20	t_w	Pulse duration; $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	$t_c - 40$†	t_c+40†	ns
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid		$1.5t_c - 75$†	ns
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid		$t_c - 85$	ns
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)	$1.5t_c - 40$†		ns

NOTE 13: t_c = system clock cycle time = $4/f_x$.

† If wait states, PFWait, or the Auto-Wait feature are used, add t_c to this value for each wait state invoked.

‡ If the Auto-Wait feature is enabled, the $\overline{WAIT}$ input may assume a "Don't Care" condition until the third cycle of the access. The $\overline{WAIT}$ signal needs to be synchronized with the high pulse of the CLKOUT signal while still observing the minimum setup time.

external read timing

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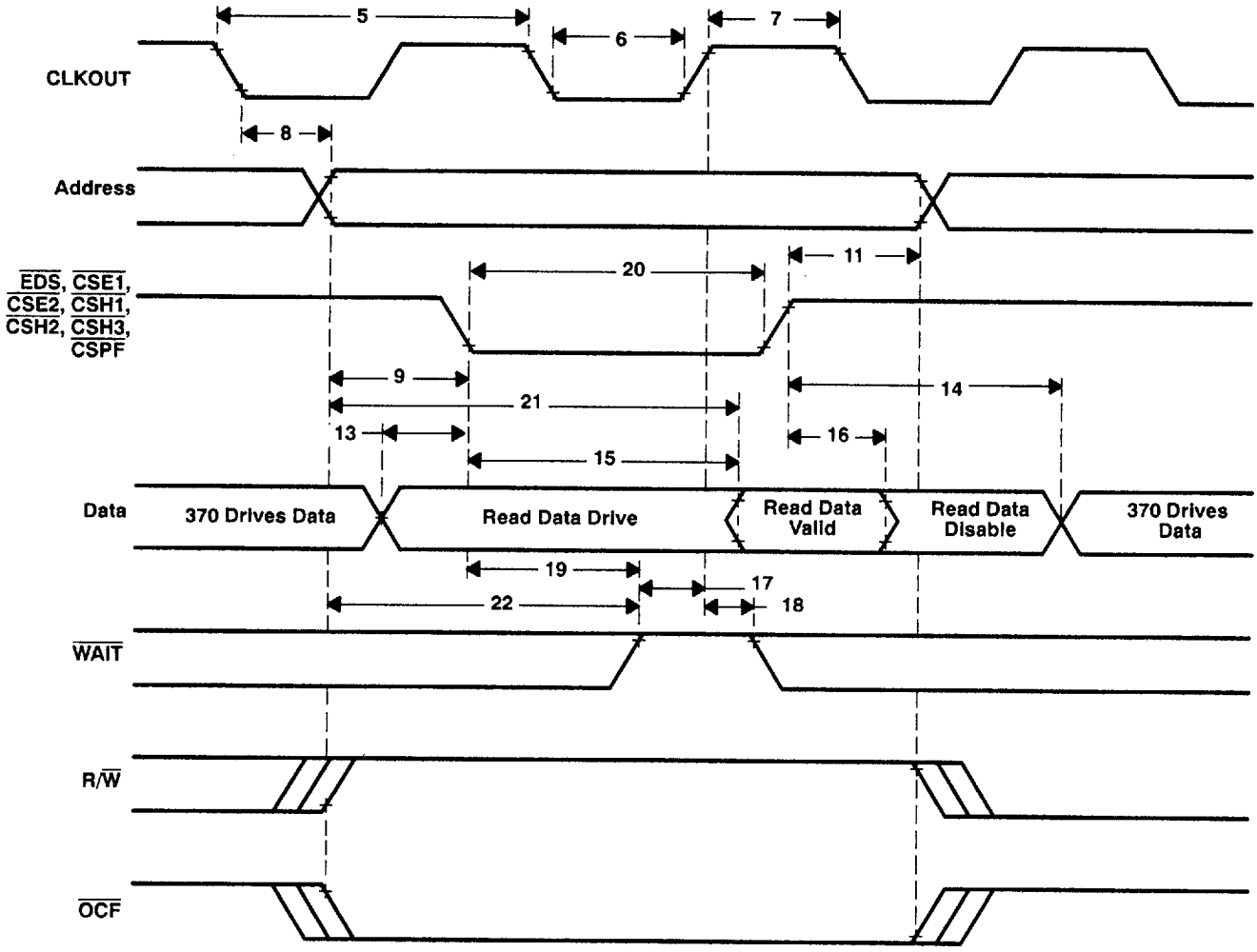
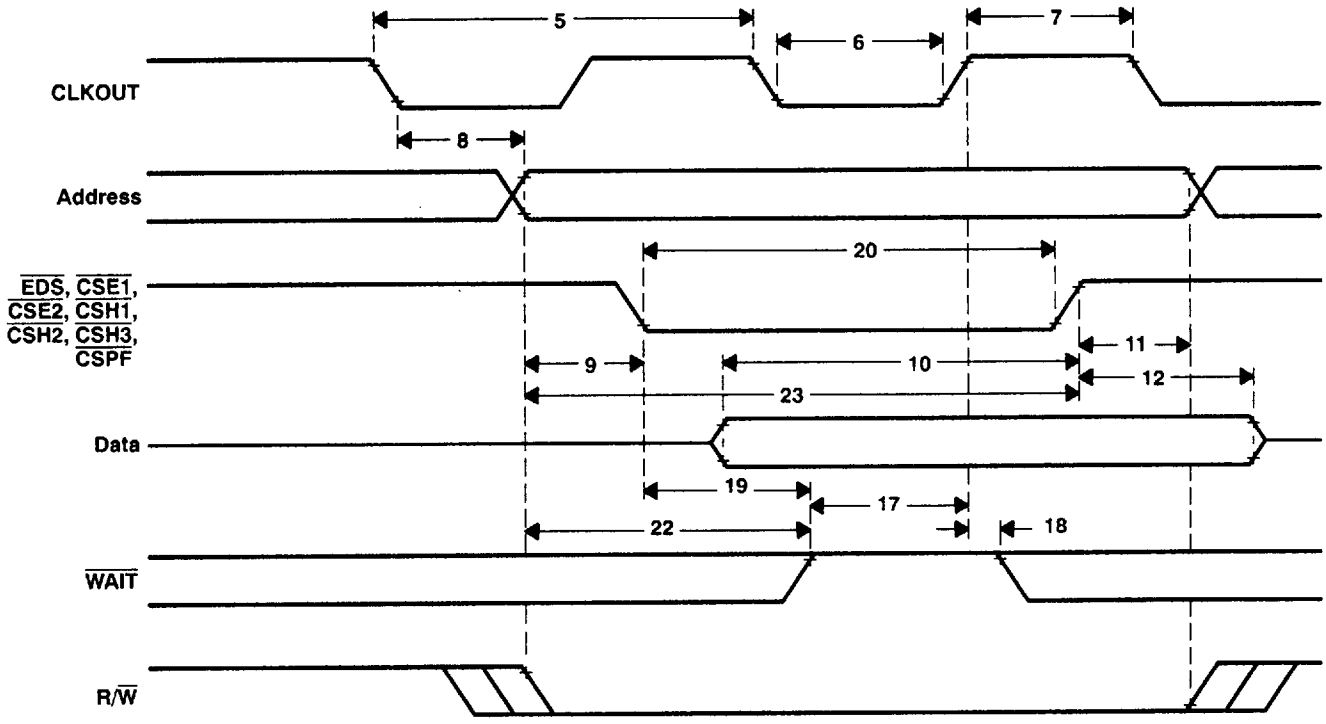


external write timing



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SERIAL COMMUNICATIONS INTERFACE (SCI) INTERNAL CLOCK ISOSYNCHRONOUS MODE I/O TIMING

SCI isosynchronous mode timing characteristics for internal clock (see Note 13)

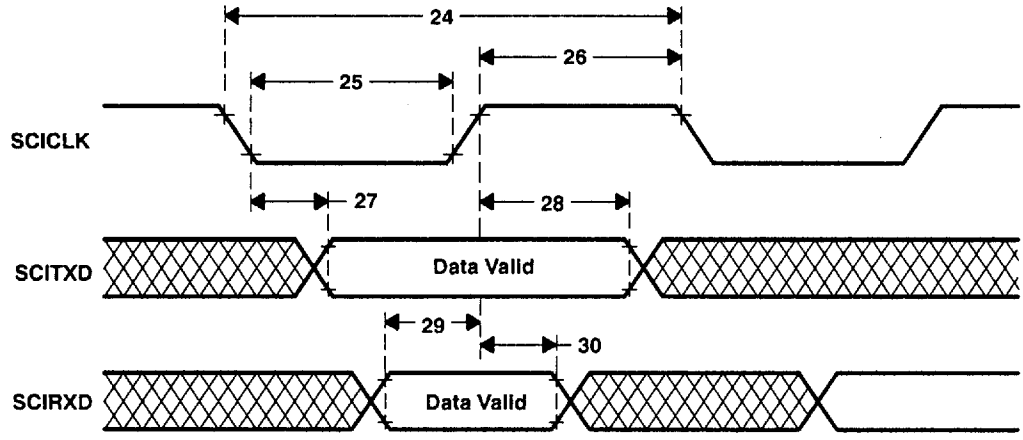
NO.	PARAMETER		MIN	MAX	UNIT
24	$t_{c(SCC)}$	SCICLK cycle time	$2t_c$	$131{,}072t_c$	ns
25	$t_{w(SCCL)}$	SCICLK low pulse duration	$t_c - 45$	$0.5t_{c(SCC)}+45$	ns
26	$t_{w(SCCH)}$	SCICLK high pulse duration	$t_c - 45$	$0.5t_{c(SCC)}+45$	ns
27	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low	−50	50	ns
28	$t_{v(SCCH-TXD)}$	SCITXD data valid after SCICLK high	$t_{w(SCCH)} - 50$		ns

SCI isosynchronous mode timing requirements for internal clock (see Note 13)

NO.	PARAMETER		MIN	MAX	UNIT
29	$t_{su(RXD-SCCH)}$	SCIRXD setup time to SCICLK high	$0.25t_c+145$		ns
30	$t_{v(SCCH-RXD)}$	SCIRXD data valid after SCICLK high	0		ns

NOTE 13: t_c = system clock period time = $4/f_x$.

SCI Isosynchronous mode timing diagram for internal clock



SERIAL COMMUNICATIONS INTERFACE (SCI) EXTERNAL CLOCK ISOSYNCHRONOUS MODE I/O TIMING

SCI isosynchronous mode timing characteristics for external clock (see Note 13)

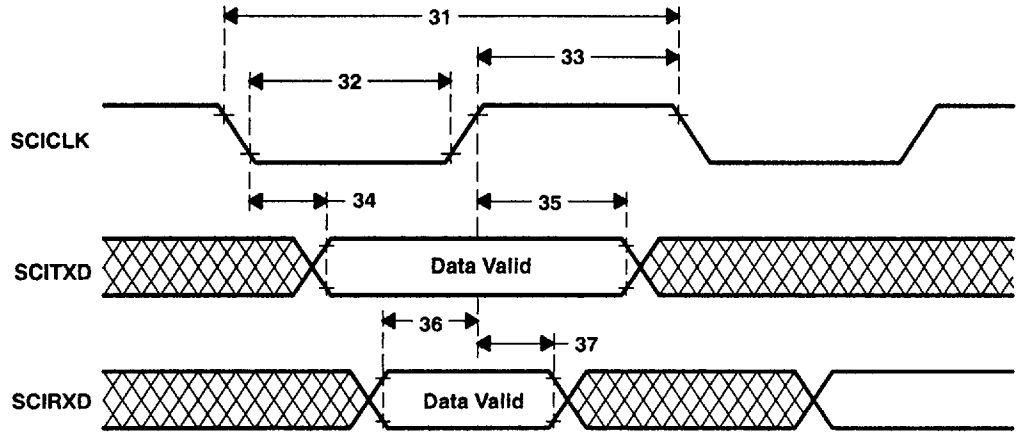
NO.	PARAMETER		MIN	MAX	UNIT
34	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low		$40.25t_c+145$	ns
35	$t_{v(SCCH-TXD)}$	SCITXD data valid after SCICLK high	$t_{w(SCCH)}$		ns

SCI isosynchronous mode timing requirements for external clock (see Note 13)

NO.			MIN	MAX	UNIT
31	$t_{c(SCC)}$	SCICLK cycle time	$10t_c$		ns
32	$t_{w(SCCL)}$	SCICLK low pulse duration	$4.25t_c+120$		ns
33	$t_{w(SCCH)}$	SCICLK high pulse duration	t_c+120		ns
36	$t_{su(RXD-SCCH)}$	SCIRXD setup time to SCICLK high	40		ns
37	$t_{v(SCCH-RXD)}$	SCIRXD data valid after SCICLK high	$2t_c$		ns

NOTE 13: t_c = system clock period time = $4/f_x$.

SCI isosynchronous mode timing diagram for external clock



SERIAL PERIPHERAL INTERFACE (SPI) TIMING

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SPI master external timing characteristics (see Note 13)

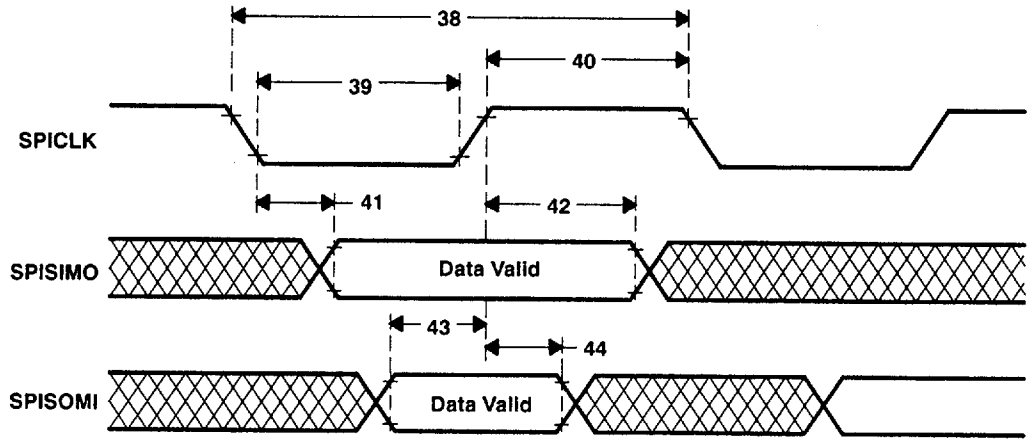
NO.	PARAMETER		MIN	MAX	UNIT
38	$t_{c(SPC)}$	SPICLK cycle time	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)}$	SPICLK low pulse duration	$t_c - 45$	$0.5t_{c(SPC)}+45$	ns
40	$t_{w(SPCH)}$	SPICLK high pulse duration	$t_c - 45$	$0.5t_{c(SPC)}+45$	ns
41	$t_{d(SPCL-SIMOV)}$	Delay time, SPISIMO valid after SPICLK low (Polarity = 1)	−50	50	ns
42	$t_{v(SPCH-SIMO)}$	SPISIMO data valid after SPICLK high (Polarity = 1)	$t_{w(SPCH)} - 50$		ns

SPI master external timing requiremtnts (see Note 13)

NO.	PARAMETER		MIN	MAX	UNIT
43	$t_{su(SOMI-SPCH)}$	SPISOMI setup time to SPICLK high (Polarity =1)	$0.25t_c+150$		ns
44	$t_{v(SPCH-SOMI)}$	SPISOMI data valid after SPICLK high (Polarity =1)	0		ns

NOTE 13: t_c = system clock period time = $4/f_x$.

SPI master external timing



NOTE 14: The diagram above is for Polarity = 1. SPICLK is inverted from above diagram when Polarity = 0.

SERIAL PERIPHERAL INTERFACE (SPI) TIMING

SPI master external timing characteristics (see Note 13)

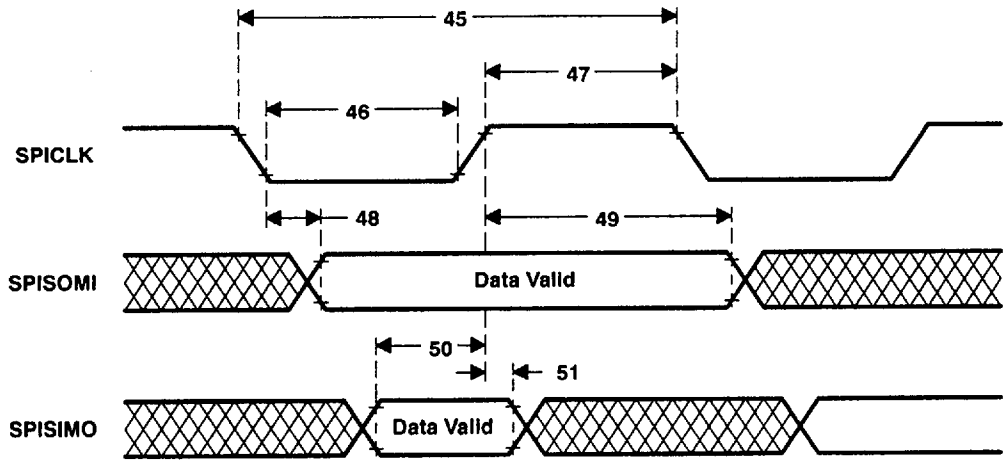
NO.	PARAMETER		MIN	MAX	UNIT
48	$t_{d(SPCL-SOMIV)S}$	Delay time, SPISOMI valid after SPICLK low (Polarity = 1)		$3.25t_c + 125$	ns
49	$t_{v(SPCH-SOMI)S}$	SPISOMI data valid after SPICLK high (Polarity =1)	$t_{w(SPCH)S}$		ns

SPI slave external timing requirements (see Note 13)

NO.			MIN	MAX	UNIT
45	$t_{c(SPC)S}$	SPICLK cycle time	$8t_c$		ns
46	$t_{w(SPCL)S}$	SPICLK low pulse duration	$4t_c - 45$	$0.5t_{c(SPC)S}+45$	ns
47	$t_{w(SPCH)S}$	SPICLK high pulse duration	$4t_c - 45$	$0.5t_{c(SPC)S}+45$	ns
50	$t_{su(SIMO-SPCH)S}$	SPISIMO setup time to SPICLK high (Polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)S}$	SPISIMO data valid after SPICLK high (Polarity = 1)	$3t_c+100$		ns

NOTE 13: t_c = system clock period time = $4/f_x$.

SPI slave external timing



NOTES: 14. The diagram above is for Polarity = 1. SPICLK is inverted from above diagram when Polarity = 0.
15. As a slave, the SPICLK pin is used as the input for the serial clock, which is supplied from the network master.

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A/D Converter

The A/D Converter has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. The purpose is to enhance A/D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A/D analog stage. All A/D specifications will be given with respect to V_{SS3} unless otherwise noted.

Resolution ..... 8 bits (256 values)
Monotonic ..... Yes
Output conversion code ..... 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \geq V_{ref}$)
Conversion time (excluding sample time) ..... $164t_c$

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		$V_{CC} - 0.3$		$V_{CC} + 0.3$	
V_{SS3}	Analog ground	$V_{SS} - 0.3$		$V_{SS} + 0.3$	V
V_{ref}	Non-V_{CC3} reference (See Note 16)	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

NOTE 16: V_{ref} must be stable, within ± 1/2 LSB of the required resolution, during the entire conversion time.

operating characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Absolute accuracy (see Note 17)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V			±1	LSB
	Differential/integral linearity error (see Notes 17 and 18)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V			±0.5	LSB
I_{CC3}	Analog supply current	Converting			2	mA
		Non-Converting			5	µA
I_I	Input current, AN0–AN7	0 V ≤ V_I ≤ 5.5 V			2	µA
	V_{ref} input charge current				1	mA
Z_{ref}	Source impedance of V_{ref}	XTAL2/CLKIN ≤ 12 MHz			24	kΩ
		12 MHz < XTAL2/CLKIN ≤ 20 MHz			10	kΩ

NOTES: 17. Absolute resolution = 20 mV. At V_{ref} = 5 V, this is 1 LSB. As V_{ref} decreases, LSB size decreases and thus absolute accuracy and differential/integral linearity errors in terms of LSBs increases.
18. Excluding quantization error of 1/2 LSB.

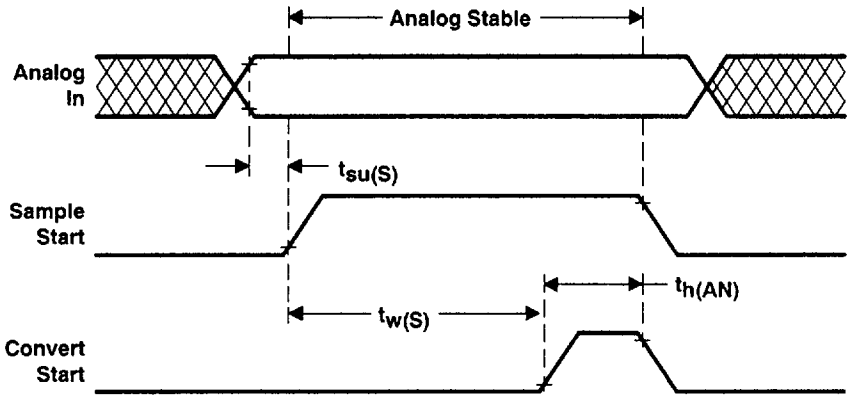
The A/D module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined such that high impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the A/D Control Register (ADCTL) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START) of the ADCTL is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

analog timing requirements

		MIN	NOM	MAX	UNIT
$t_{su(S)}$	Analog input setup to sample command	0			ns
$t_{h(AN)}$	Analog input hold from start of conversion	$18t_c$			ns
$t_{w(S)}$	Duration of sample time per kilohm of source impedance (see Note 19)	1			μs/kΩ

NOTE 19: The value given is valid for a signal with a source impedance greater than 1 kΩ. If the source impedance is less than 1 kΩ, use a minimum sampling time of 1 μs.

analog timing



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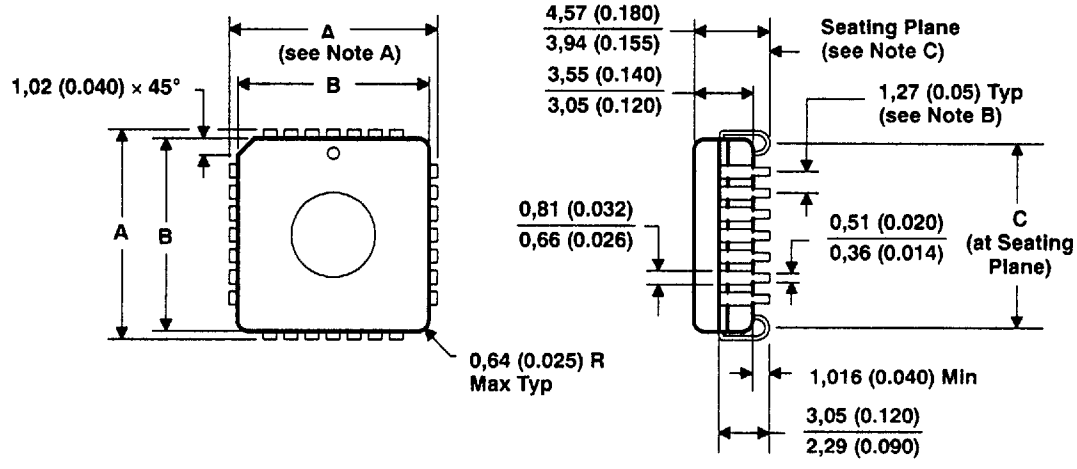
MECHANICAL DATA

68-lead FZ cerquad chip carrier package

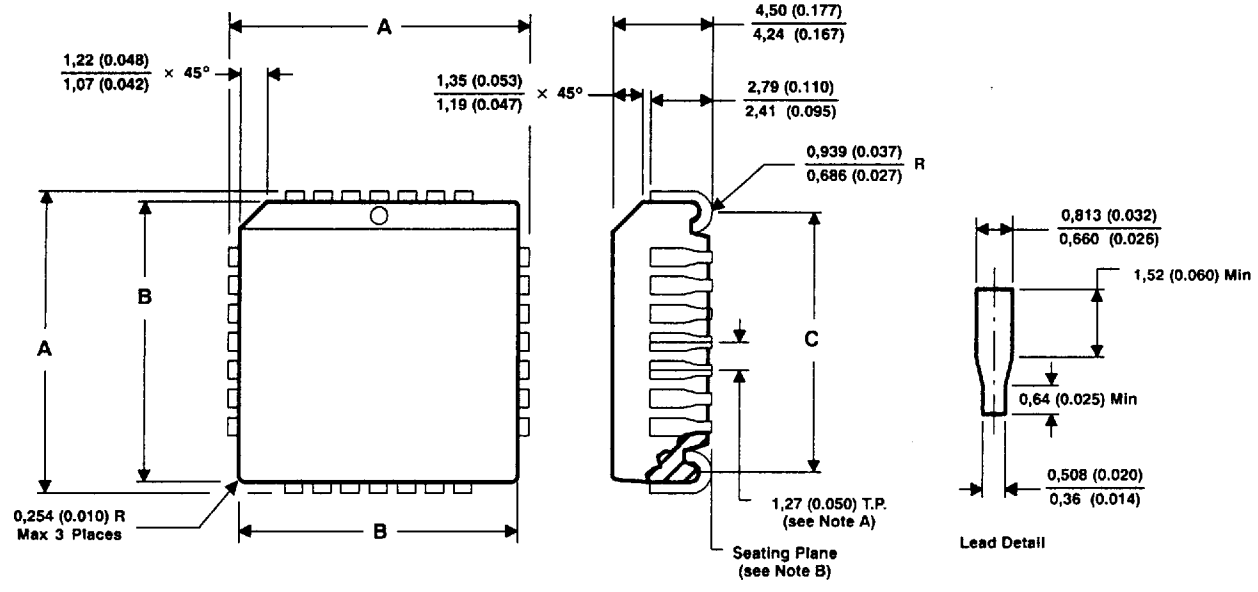


JEDEC OUTLINE	NO. OF TERMINALS	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
M0-087AA	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10,92 (0.430)
M0-087AB	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 0.610)	16,00 (0.630)
M0-087AD	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23,11 (0.910)	23,62 (0.930)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Center line of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar with 0,15 (0.006).

68-pin plastic leaded chip carrier package (FN suffix)



JEDEC OUTLINE	NO. OF TERMINALS	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
M0-047AB	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10,92 (0.430)
M0-047AC	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 0.610)	15,90 (0.630)
M0-047AE	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23,11 (0.910)	23,62 (0.930)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
B. The lead contact points are planar within 0,101(0.004).