User's Guide

TPS92520EVM-133 Dual 1.6-A Synchronous Buck LED Driver Evaluation Module

ABSTRACT

This user's guide describes the specifications, board connection description, characteristics, operation, and use of the TPS92520-Q1, dual 1.6-A synchronous buck LED driver evaluation module (EVM). A complete schematic diagram, printed circuit board layouts, and bill of materials are included in this document.

Table of Contents

List of Figures

Copyright © 2021 Texas Instruments Incorporated

List of Tables

Copyright © 2021 Texas Instruments Incorporated

Trademarks

LaunchPad™ is a trademark of Texas Instruments.
Microsoft® and .NET Framework® are registered trademarks of MIcrosoft Corporation.
All trademarks are the property of their respective owners.

Copyright © 2021 Texas Instruments Incorporated

General Texas Instruments High Voltage Evaluation (TI HV EMV) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you must immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

Copyright © 2021 Texas Instruments Incorporated

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

Copyright © 2021 Texas Instruments Incorporated

1 Description

This user's guide describes the specifications, board connection description, characteristics, operation, and use of the TPS92520-Q1, dual 1.6-A synchronous buck LED driver evaluation module (EVM). The TPS92520-Q1 device implements an adaptive on-time average current mode control and is designed to be compatible with shunt FET dimming techniques and LED matrix manager-based dynamic beam headlamps. The adaptive on-time control provides near constant switching frequency that can be set between 100 kHz and 2.2 MHz. Inductor current sensing and closed-loop feedback enables better than ±4% accuracy over wide input voltage, output voltage and ambient temperature range.

Additional features include wide input voltage range (4.5 V to 65 V), programmable switching frequency, programmable analog and PWM dimming techniques, advanced SPI programmable diagnostic and fault protection featuring: cycle-by-cycle switch current limit, bootstrap undervoltage, LED open, LED short, thermal warning and thermal shutdown. An onboard 10-bit ADC samples critical input parameters required for system health monitoring and diagnostics. Complete schematic diagrams, printed circuit board layouts, and bill of materials are included in this document.

1.1 Typical Applications

This document outlines the operation and implementation of the TPS92520-Q1 as dual-synchronous buck constant current (CC) LED driver with the specifications listed in Table 2-1. For applications with a different input voltage range or different output voltage range, see the *TPS92520-Q1 4.5-V to 65-V Dual 1.6-A Synchronous Buck LED Driver with SPI Control Data Sheet*. The LEDMCUEVM-132 Development Tool controls the TPS92520EVM-133 evaluation board. The LEDMCUEVM-132 is available on TI website. Alternatively, any SPI controller board can control the TPS92520EVM-133. After the LED MCU EVM board is obtained from the TI website, the board must be programmed according to the instructions provided in this design guide. The program instructions are provided in Section 5.

1.2 Warnings

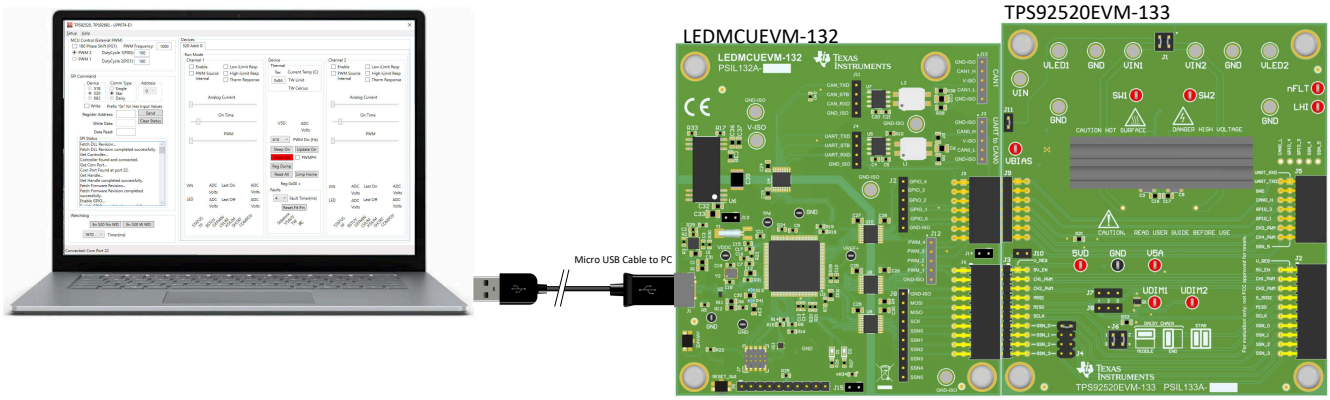
Observe the following precaution when using the TPS92520EVM-133 evaluation module.

Caution hot surface. Contact may cause burns. Do not touch.

1.3 Connector Description

Table 1-1 describes the connectors and Table 1-2 lists the test points on the EVM and how to properly connect, set up, and use the TPS92520EVM-133.

Figure 1-1 shows the connection diagram and the default jumper locations of the TPS92520EVM-133.



Copyright © 2021 Texas Instruments Incorporated

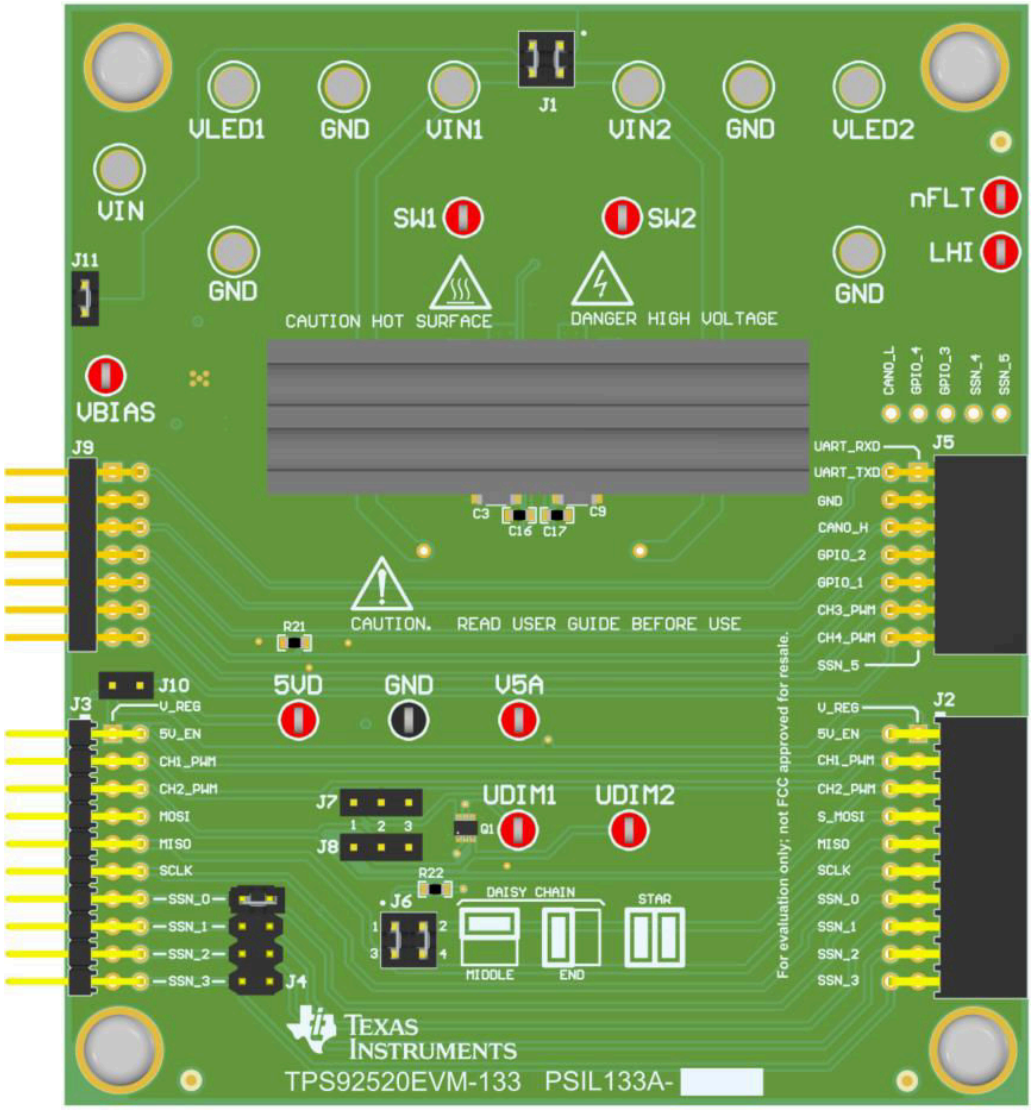


Figure 1-1. Connection Diagram of Computer, USB Cable, LEDMCUEVM-132, and TPS92520EVM-133.

Table 1-1. Connector Descriptions

Connector	Function	Description
J3	SPI control from the LEDMCUEVM-132	J2 and J3 allow attachment for SPI control of the TPS92520-Q1 to the TI LED MCU, part number LEDMCUEVM-132. J3 is connected to the LEDMCUEVM-132. J2 is connected other EVMs used in star or daisy chain configurations.
J2		
J9	Additional control signals to EVM	J9 and J5 are CAN, UART, GPIO, PWM, and SSN5 signals that come form LEDMCUEVM-132 by J9 and are passed through to other EVMs by J5.
J5		
J1	VIN1 and VIN2 connections	J1 configures how VIN1 and VIN2 are connected to each other or to VIN. No jumpers separates VIN1, VIN2, and VIN. A jumper from pins 2 to 4 connects VIN1 to VIN2. Jumpers from pin 1 to 2 and pin 3 to 4 connect VIN1, VIN2, and VIN all together (this setup is the default configuration).
J6	SPI configuration	J6 allow for the ability to setup the hardware into a daisy chain configuration with both a middle device and end device in the chain. The default configuration is a star configuration (pin 1 and 3 are jumpered and pin 2 and 4 are jumpered) where all devices are controlled by an independent SSN signals and must be selected based on J4 settings.
J10	V_REG jumper	J10 is a jumper provided to share VREG from LEDMCUEVM-132 with other SPI controlled EVM, in case a digital supply is needed by the EVM, leave this jumper open because an onboard supply is provided on this EVM.

Copyright © 2021 Texas Instruments Incorporated

Table 1-1. Connector Descriptions (continued)

Connector	Function	Description
J11	VIN connection to 5V regulator	J11 is loaded by default which allows for VIN to power the 5-V regulator. Removing J11 allow for the connection of the 5-V regulator by external supply to VBIAS test point to do performance testing such as measuring input current of the regulator.
J7	UDIM1 jumper	J7 and J8 are jumpers to allow for PWM signals to be applied to the two channels by the UDIM1 and UDIM2. When the jumpers are removed (default configuration) the PWM outputs can be generated from register setting of the TPS92520 or by applying a signal directly to the UDIM pins. If pins 1 and 2 are shunted on J7 and J8 then a non-inverted PWM signals from the LEDMCUEVM-132 controller board is connected to the UDIM pins and controls the PWM dimming via the GUI. When the jumpers are populated from pin 2 to 3 then the PWM signals from LEDMCUEVM-132 are inverted. The PWM signals can be used to disable the associated channels.
J8	UDIM2 jumper	
J4	SSN configuration jumper	J9 allows configuration of the SSN chip select line, when multiple chips on the same SPI bus are used. By default, evaluation module shunt connect pin 7 and 8 of J4, which is SSN0 of the LEDMCUEVM-132. Moving the shunt location changes the SSN that is used.

Table 1-2. Test Points

Test Point	Description
GND (TP15, TP16, TP17, TP18, TP19)	Larger metal turrets and test points allow for multiple connection to grounds across the board.
VIN (TP4)	The VIN test point allows for voltage and current measurement of the external power supply applied to the evaluation board for the 5V regulator assuming J1 is configured properly.
VIN1 (TP3)	The VIN1 test point allows for voltage and current measurement of the power applied to the VIN1 pin of the TPS92520-Q1 assuming J1 is configured properly.
VIN2 (TP5)	The VIN2 test point allows for voltage and current measurement of the power applied to the VIN2 pin of the TPS92520-Q1 assuming J1 is configured properly.
LHI (TP8)	The LHI test point is the LED current reference set point for both Limp-home and standalone mode for the TPS92520-Q1. Setting voltages below 148 mV disables both channels and setting the voltage above 200mV enables both channels in limp home and standalone mode.
nFLT (TP7)	The nFLT test point can be used to monitor if a fault has occurrence in the TPS92520-Q1. When a fault occurs, nFLT voltage level goes low. Read Faults and Diagnostics section of the *TPS92520-Q1 data sheet* to determine which faults trigger the nFLT indication and how to clear the fault.
VLED1 (TP6)	The VLED1 test point allows for connection of the LED loads to channel-1 output. Large turrets allow for multiple connections for voltage measurements.
VLED2 (TP12)	The VLED2 test point allows for connection of the LED loads to channel-2 output. Large turrets allow for multiple connections for voltage measurements.
SW1 (TP9)	The SW1 test point allows for observing the switch node for channel 1 during operation with an oscilloscope.
SW2 (TP13)	The SW2 test point allows for observing the switch node for channel 2 during operation with an oscilloscope.
VBIAS (TP1)	VBIAS test point connects directly to the input of the linear regulator that generates the 5V supply used by the TPS92520-Q1. The test point can be used to monitor the input voltage or used to connect to an external supply for both voltage and current measurements assuming J11 is unloaded.
5VD (TP10)	5VD test point connects directly to the V5D digital pin of the TPS92520-Q1. This test point can be used to monitor the voltage or used to supply the power directly to the V5D pin assuming J11 is disconnected and nothing is powering the 5V bus. Note if doing current measurements then R10 connects 5VD rail to V5A which consumes power but can be separated by removing R10 and supply V5A externally.
V5A (TP11)	V5A test point connects directly to V5A pin of the TPS92520-Q1. This test point can be used to monitor the voltage or current used to supply the power directly to V5A pin assuming R10 has been removed. By default V5D and V5A are shorted together and the supply is provided by the 5VD supply.
UDIM1 (TP2)	UDIM1 test point allows for the direct connection of the UDIM1 pin of the TPS92520-Q1. UDIM1 test point allows for external PWM dimming signals to control channel 1 assuming J7 is unloaded. This test point can also be used to monitor the PWM signal generated from the LEDMCUEVM-132 for channel 1 assuming J7 is loaded.
UDIM2 (TP14)	UDIM2 test point allows for the direct connection of the UDIM2 pin of the TPS92520-Q1. UDIM2 test point allows for external PWM dimming signals to control channel 2 assuming J8 is unloaded. This test point can also be used to monitor the PWM signal generated from the LEDMCUEVM-132 for channel 2 assuming J8 is loaded.

Copyright © 2021 Texas Instruments Incorporated

2 Performance Specifications

Table 2-1 provides the EVM electrical performance specifications.

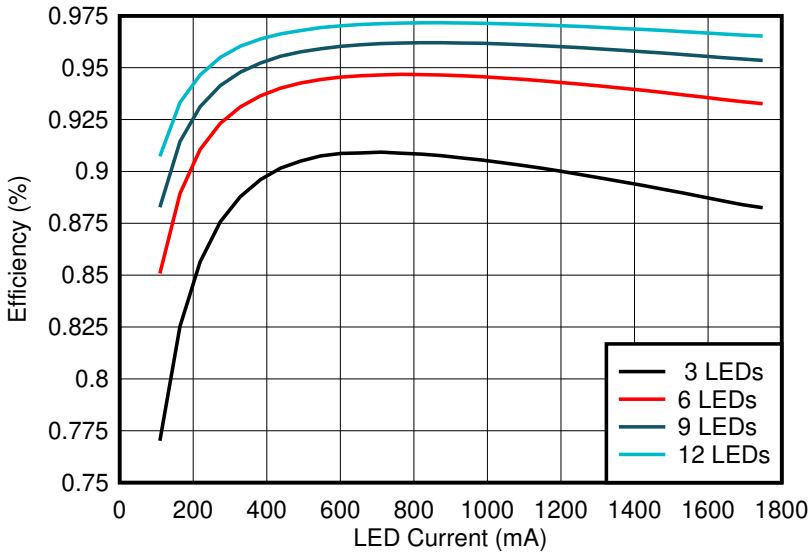
Table 2-1. TPS92520EVM Performance Specifications

Parameter	Description	Min	Typ	Max	Units
Input Characteristics					
Voltage, V_{IN}	The EVM is designed to operate at above 40 V, but can be setup to operate at lower input voltages if J11 is not loaded and the VBIAS test point is connected to an external supply that is less than 40 V or attached to VIN test point if VIN is less than 40 V.	4.5	50	65	V
Maximum Input Current, I_{IN}				4	A
Output Characteristics					
Output Voltage, V_{OUT}	Maximum voltage configured by the output voltage divider and programmable by the SPI	V_{IN}		60	V
Maximum Output Current, I_{OUT}	Total output current per channel			1.6	A
Maximum Output Power, P_{OUT}	Total output power			120	W
Systems Characteristics					
Switching frequency	Switching Frequency (f_{SW}) Range	100		2,200	kHz
Peak efficiency				96	%
Operating temperature		–40	25	125	°C

Copyright © 2021 Texas Instruments Incorporated

3 Performance Data and Typical Characteristic Curves

Figure 3-1 illustrates the efficiency results for the TPS92520EVM-133 versus output power for different input voltage V_{IN}.

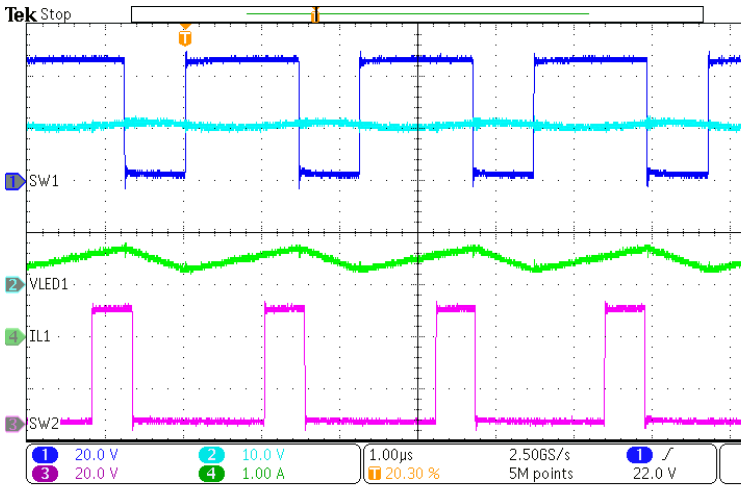


Conditions: V_{IN} 60 V, f_{SW} = 437 kHz

Figure 3-1. Efficiency vs LED Current

3.1 1.5A CC BUCK SW-Node Voltage Waveform

Figure 3-1 shows the switch node voltage waveforms of the channel 1 and channel 2 of the TPS92520EVM-133 dual channel BUCK LED driver. The switch node (SW1 and SW2) of the two channels that are completely independent of each other. SW1 and SW2 are not in phase and are not 180 degrees out of phase. The switching frequency, input voltage, and out LED current setpoints can also be set independently on each channel.



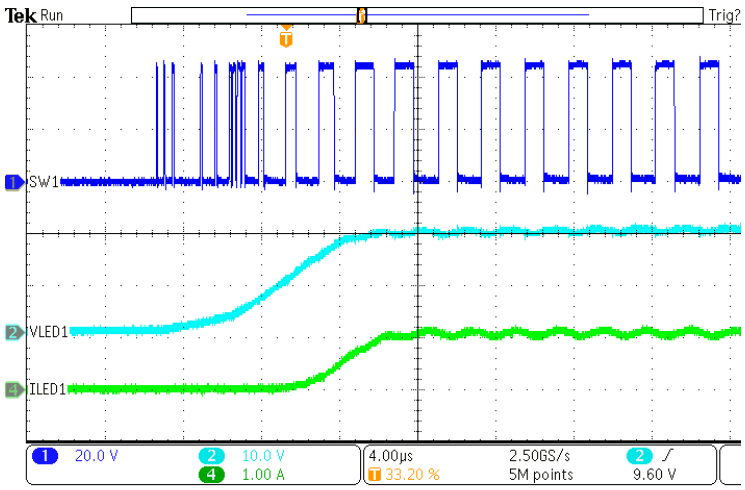
V_{IN} = 48 V, V_{LED1} = 30 V, V_{LED2} = 10 V

Figure 3-2. Dual-Channel Buck SW-Node Voltage

Copyright © 2021 Texas Instruments Incorporated

3.2 Start-up Waveforms

Figure 3-3 shows the start-up waveforms for channel 1 (V_{LED1} and I_{LED1}) of the TPS92520EVM-133 dual-channel buck LED driver settings set to 1 A I_{LED1} with 6 LEDs .

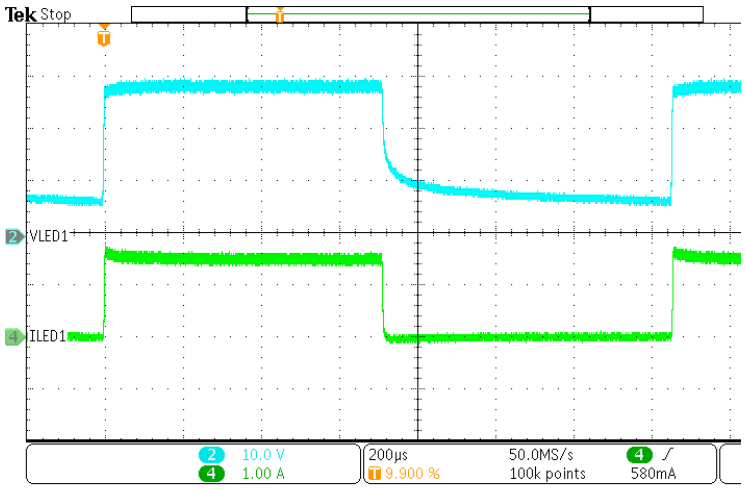


V_{IN} = 48 V, V_{LED1} = 20 V, I_{LED1} = 1.0 A

Figure 3-3. Soft-Start Waveforms

3.3 PWM Dimming

Figure 3-4 shows the load transient on the output of the TPS92520EVM-133 LED buck driver. The output LED string controlled by the PWM dimming registers at 50% duty cycle at 610 Hz PWM frequency. The V_{LED} waveform (channel 2 of the osope) and the I_{LED} waveform (channel 4 of the oscope) shows the resulting undershoot and overshoot.



V_{IN} = 48 V, V_{LED1} = 28 V, I_{LED1} = 1.5 A

Figure 3-4. 1.6-A Buck LED Driver Load Transient

4 Schematic, PCB Layout, and Bill of Materials

This section contains TPS92520EVM-133 schematics, PCB layouts, and bill of materials (BOM).

Copyright © 2021 Texas Instruments Incorporated

4.1 Schematic

Figure 4-1 and Figure 4-2 illustrate the TPS92520EVM-133 schematic.

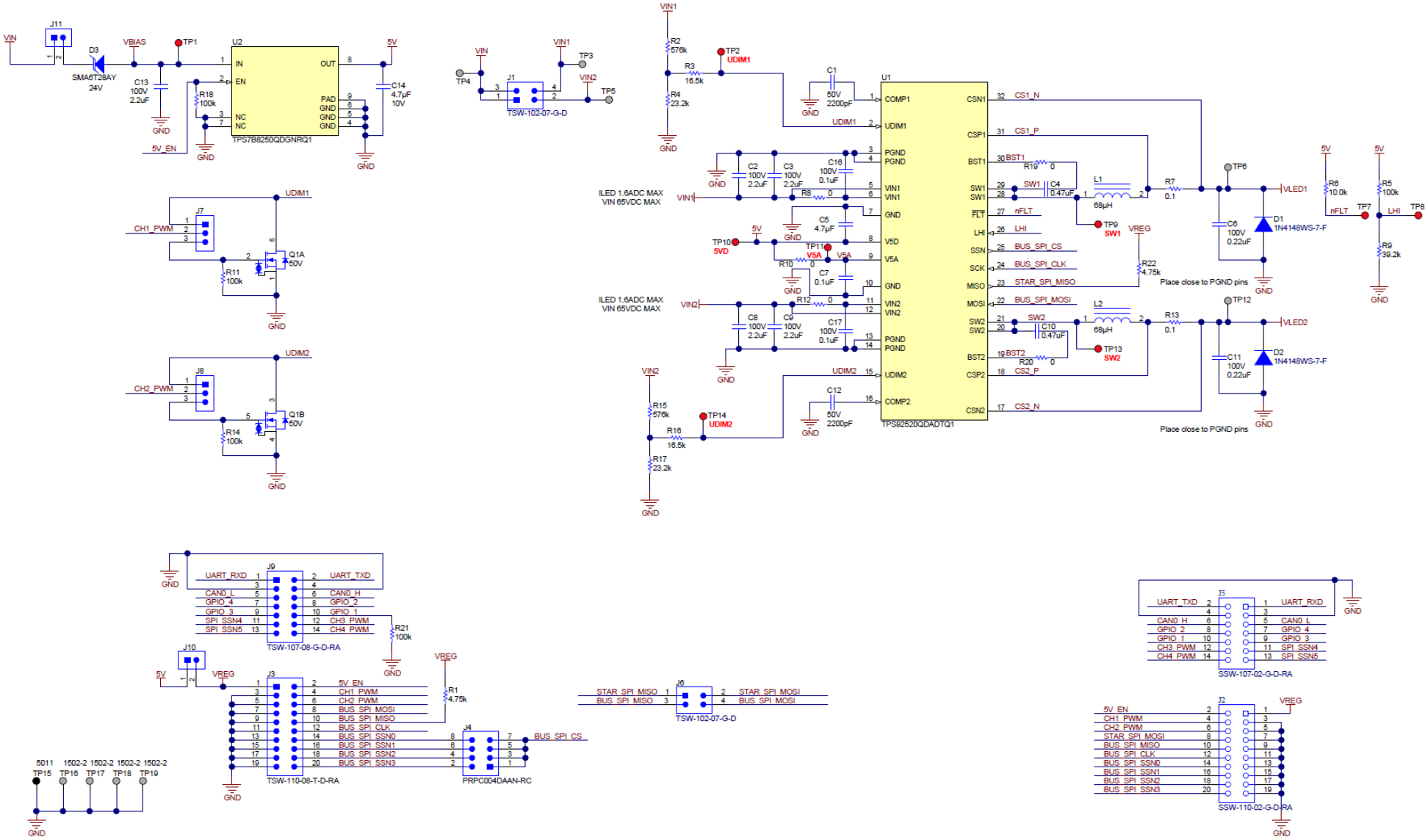
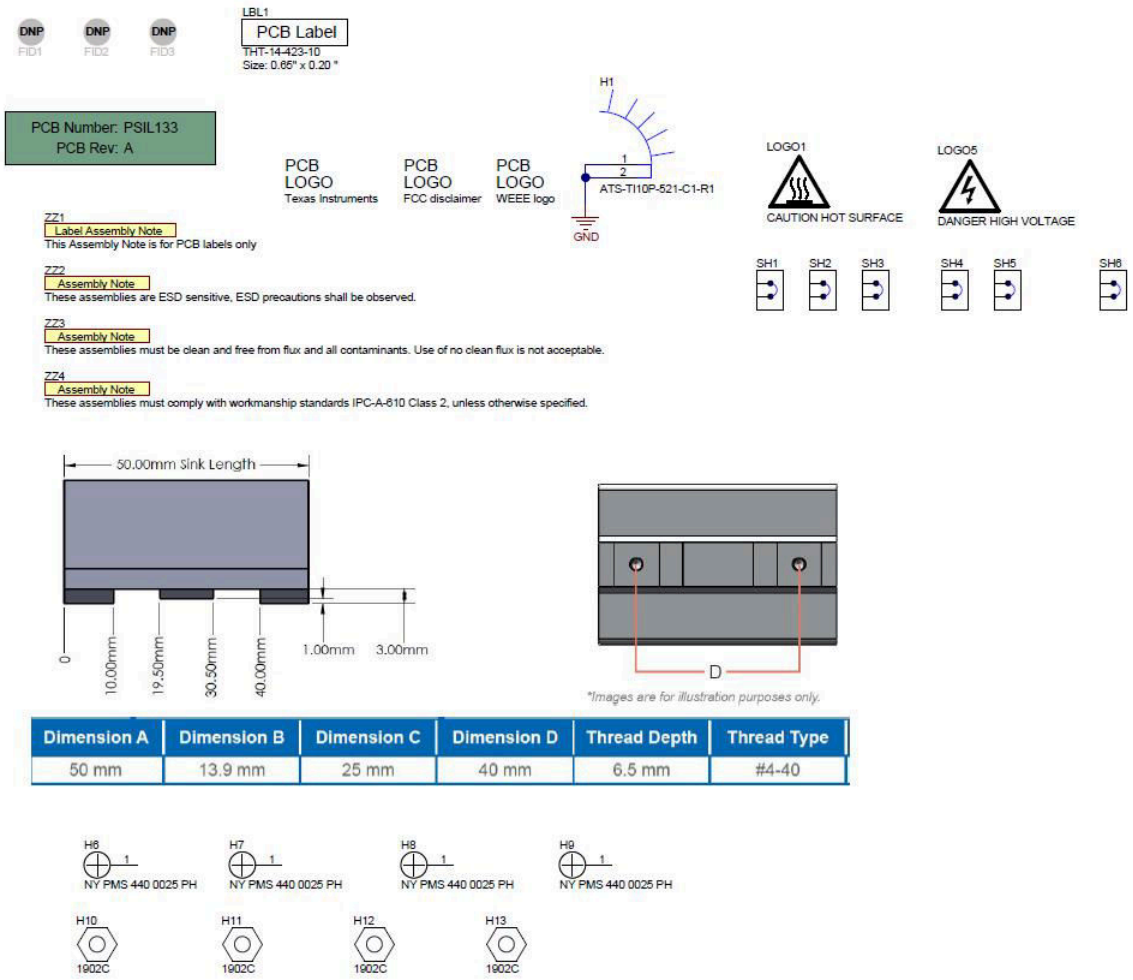


Figure 4-1. TPS92520EVM-133 Schematic - Page 1

Copyright © 2021 Texas Instruments Incorporated



Dimension A	Dimension B	Dimension C	Dimension D	Thread Depth	Thread Type
50 mm	13.9 mm	25 mm	40 mm	6.5 mm	#4-40

Figure 4-2. TPS92520EVM-133 Schematic - Page 2

Copyright © 2021 Texas Instruments Incorporated

4.2 Layout

The TPS92520EVM-133 is a 4-layer board. Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7 illustrate the assembly, the top, the inner-layer1, the inner-layer2 and the bottom side of the TPS92520EVM-133 PCB layout. The Inner-layer 1 is a ground plane and there is no routing on this layer.

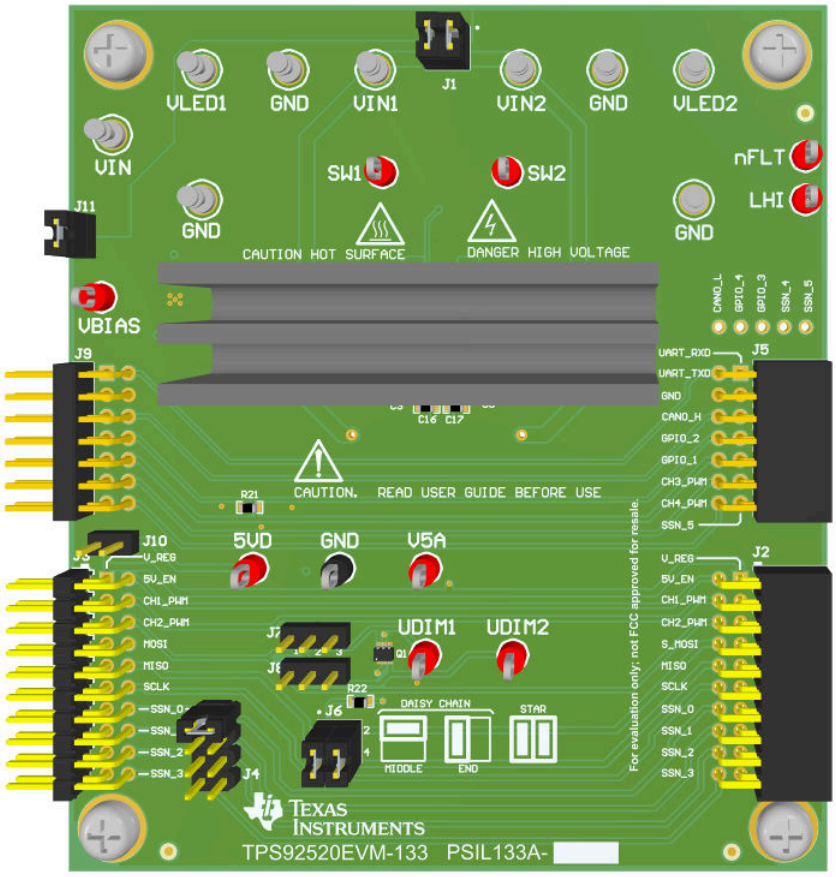


Figure 4-3. TPS92520EVM-133 Assembly Drawing

Copyright © 2021 Texas Instruments Incorporated

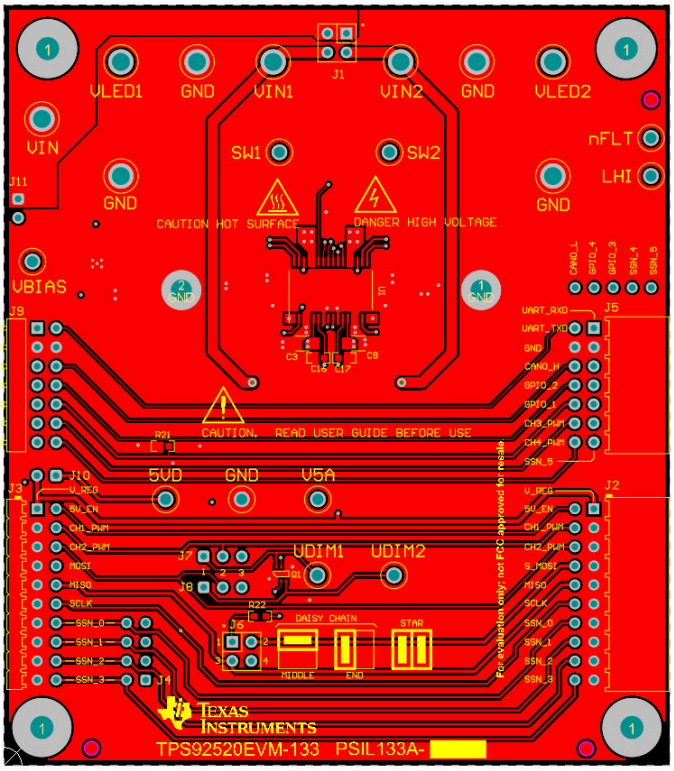


Figure 4-4. TPS92520EVM-133 Top Layer and Top Overlay (Top View)

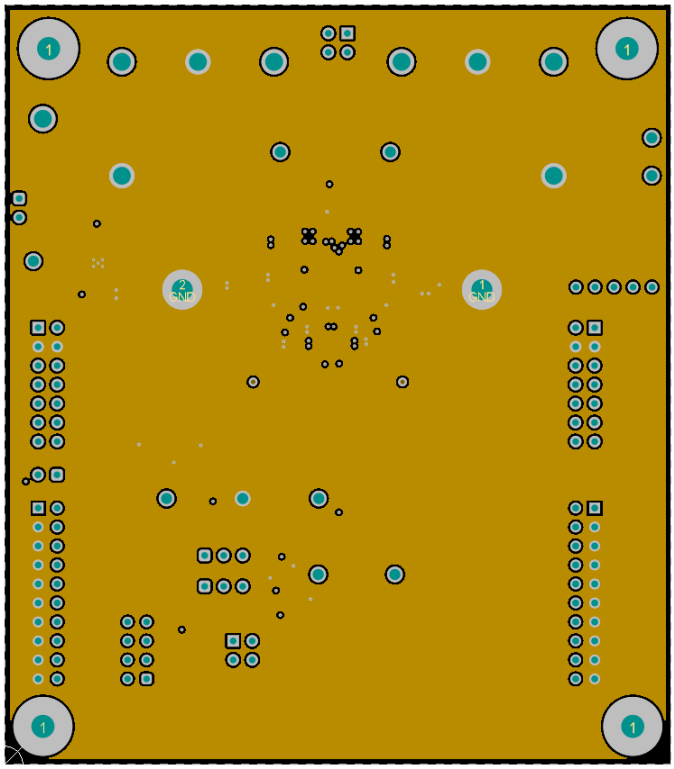


Figure 4-5. TPS92520EVM-133 Inner-Layer 1

Copyright © 2021 Texas Instruments Incorporated

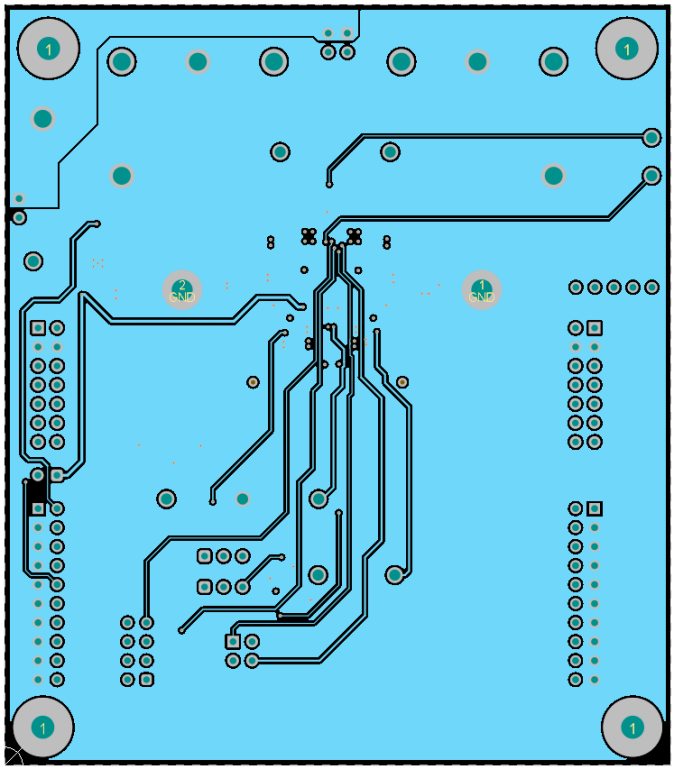


Figure 4-6. TPS92520EVM-133 Inner-Layer 2

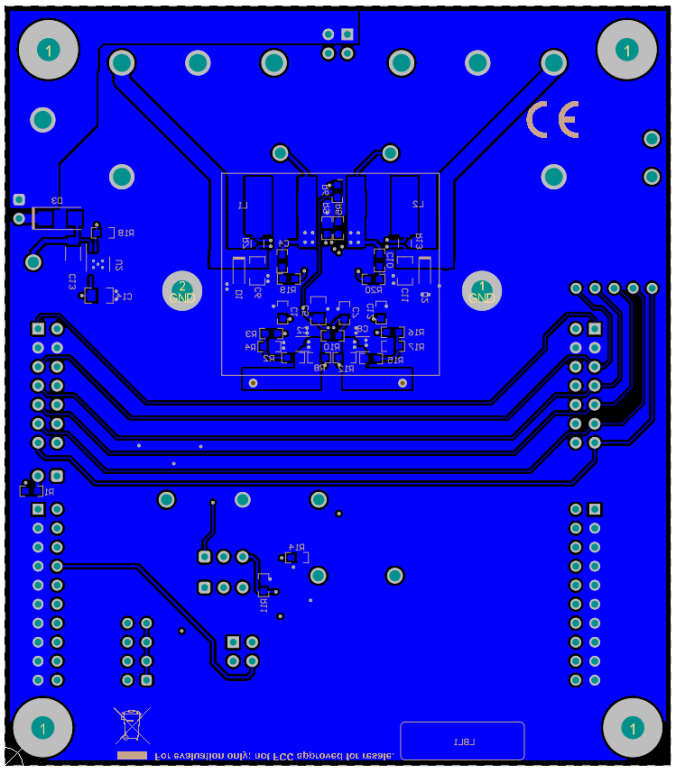


Figure 4-7. TPS92520EVM-133 Bottom Layer and Bottom Overlay (Bottom View)

Copyright © 2021 Texas Instruments Incorporated

4.3 Bill of Materials

Table 4-1 lists the TPS92520EVM-133 bill of materials.

Table 4-1. TPS92520EVM-133 Bill of Materials

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
C1, C12	2	2200 pF	CAP, CERM, 2200 pF, 50 V, ±5%, C0G/NP0	0603	GRM1885C1H222JA01D	MuRata
C2, C3, C8, C9	4	2.2 µF	CAP, CERM, 2.2 uF, 100 V, ±20%, X7S, AEC-Q200 Grade 1	1206	CGA5L3X7S2A225M160AB	TDK
C4, C10	2	0.47 µF	CAP, CERM, 0.47 uF, 25 V, ±10%, X7R, AEC-Q200 Grade 1	0603	CGA3E3X7R1E474K080AB	TDK
C5	1	4.7 µF	CAP, CERM, 4.7 µF, 16 V, ±10%, X7R, AEC-Q200 Grade 1	0805	CGA4J3X7R1C475K125AE	TDK
C6, C11	2	0.22 µF	CAP, CERM, 0.22 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1	0805	CGA4F3X7S2A224M085AE	TDK
C7, C16, C17	3	0.1 µF	CAP, CERM, 0.1 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1	0603	CGA3E3X7S2A104K080AB	TDK
C13	1	2.2 µF	CAP, CERM, 2.2 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1	0603	CGA5L3X7S2A225K160AB	TDK
C14	1	4.7 µF	CAP, CERM, 4.7 µF, 10 V, ±5%, X7R, AEC-Q200 Grade 1	0805	C0805C475J8RACAUTO	Kemet
D1, D2	2	75 V	Diode, Switching, 75 V, 0.15 A, AEC-Q101	SOD-323	1N4148WS-7-F	Diodes Inc
D3	1	24 V	Diode, TVS, Uni, 24 V, 44.3 Vc, AEC-Q101	SMA	SMA6T28AY	STMicroelectronics
H1	1		HEAT SINK FOR TI MOD, 50x13.9mm		ATS-TI10P-521-C1-R1	Advanced Thermal Solutions
H6, H7, H8, H9	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead		NY PMS 440 0025 PH	B&F Fastener Supply
H10, H11, H12, H13	4		Standoff, Hex, 0.5"L #4-40 Nylon		1902C	Keystone
J1, J6	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Semtec
J2	1		Receptacle, 2.54mm, 10x2, Gold, R/A, TH	Receptacle, 2.54mm, 10x2, R/A, TH	SSW-110-02-G-D-RA	Semtec
J3	1		Header, 2.54mm, 10x2, Tin, R/A, TH	Header, 2.54mm, 10x2, R/A, TH	TSW-110-08-T-D-RA	Semtec
J4	1		Header, 2.54mm, 4x2, Gold, TH	Header, 2.54mm, 4x2, TH	PRPC004DAAN-RC	Sullins Connector Solutions
J5	1		Receptacle, 100mil, 7x2, Gold, R/A, TH	Receptacle, 7x2, 2.54mm, R/A, TH	SSW-107-02-G-D-RA	Semtec

Copyright © 2021 Texas Instruments Incorporated

Table 4-1. TPS92520EVM-133 Bill of Materials (continued)

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
J7, J8	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Semtec
J9	1		Header, 100mil, 7x2, Gold, R/A, TH	7x2 R/A Header	TSW-107-08-G-D-RA	Semtec
J10, J11	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
L1, L2	2	68 µH	Inductor, Shielded, Metal Composite, 68 µH, 1.8 A, 0.316 ohm, SMD	SMD	SPM6545VT-680M-D	TDK
Q1	1	50 V	MOSFET, 2-CH, N-CH, 50 V, 0.305 A, AEC-Q101	OT-363	DMN5L06DWK-7	Diodes Inc.
R1, R22	2	4.75 kΩ	RES, 4.75 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06034K75FKEA	Vishay-Dale
R2, R15	2	576 kΩ	RES, 576 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW0603576KFKEA	Vishay-Dale
R3, R16	2	16.5 kΩ	RES, 16.5 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060316K5FKEA	Vishay-Dale
R4, R17	2	23.2 kΩ	RES, 23.2 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060323K2FKEA	Vishay-Dale
R5, R11, R14, R18, R21	5	100 kΩ	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW0603100KFKEA	Vishay-Dale
R6	1	10.0 kΩ	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060310K0FKEA	Vishay-Dale
R7, R13	2	0.1 Ω	RES, 0.1, 1%, .5 W, AEC-Q200 Grade 0	0805	KRL1220E-M-R100-F-T5	Susumu Co Ltd
R8, R10, R12, R19, R20	5	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06030000Z0EA	Vishay-Dale
R9	1	39.2 kΩ	RES, 39.2 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060339K2FKEA	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6		Shunt, 2.54 mm, Gold, Black	2x1, 2.54mm	60900213421	Wurth Elektronik
TP1, TP2, TP7, TP8, TP9, TP10, TP11, TP13, TP14	9		Test Point, Miniature, Red, TH	TH	5010	Keystone
TP3, TP4, TP5, TP6, TP12, TP16, TP17, TP18, TP19	9		Terminal, Turret, TH, Double	TH	1502-2	Keystone
TP15	1		Test Point, Multipurpose, Black, TH	Turret	1502-2	Keystone
U1	1		4.5 to 65-V Input Dual 1.6-A Synchronous Buck LED Driver with SPI Control	DAD0032A	TPS92520QDADTQ1	Texas Instruments
U2	1		300mA High-Voltage Ultra-Low-Iq Low-Dropout (LDO) Regulator	DGN0008D	TPS7B8250QDGNRQ1	Texas Instruments

Copyright © 2021 Texas Instruments Incorporated

5 Software

This section describes the installation of the GUI software, the necessary drivers to operate the TPS92520EVM-133.

5.1 Demonstration Kit Software Installation for LEDMCUEVM-132 Board

5.1.1 Installation Overview

This section is a summary of the installation steps. To see step-by step instructions with screen shots, see Section 5.2.

1. Click on *TPS92518, 520, 682 LaunchPad™ Evaluation Software Installer.exe*
2. Right click, and choose **Run As Administrator**
3. Click **yes** when *Windows Account Control* asks to allow the program to make changes to the computer
4. Click **I Agree** to the installation license terms and install in the recommended location

Installation will take a few minutes, as it may need to install Microsoft® .NET Framework®. If the installer asks if you wish to reboot after installing Microsoft .NET, you must click **Restart Later** and allow the driver installation to complete.

After running the *TPS92518, 520, 682 LaunchPad Evaluation Software Installer.exe*, the evaluation software window appears as shown in Figure 6-7.

5.2 Step-by-Step Installation Instructions

This section shows the detailed installation instructions with screen shots.

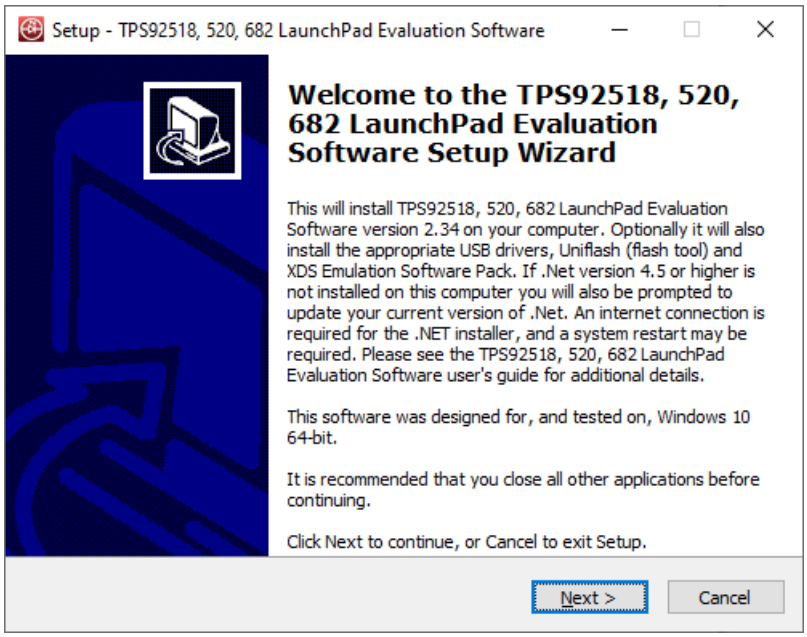


Figure 5-1. Setup Screen 1

Click **Next >** to install.

Copyright © 2021 Texas Instruments Incorporated

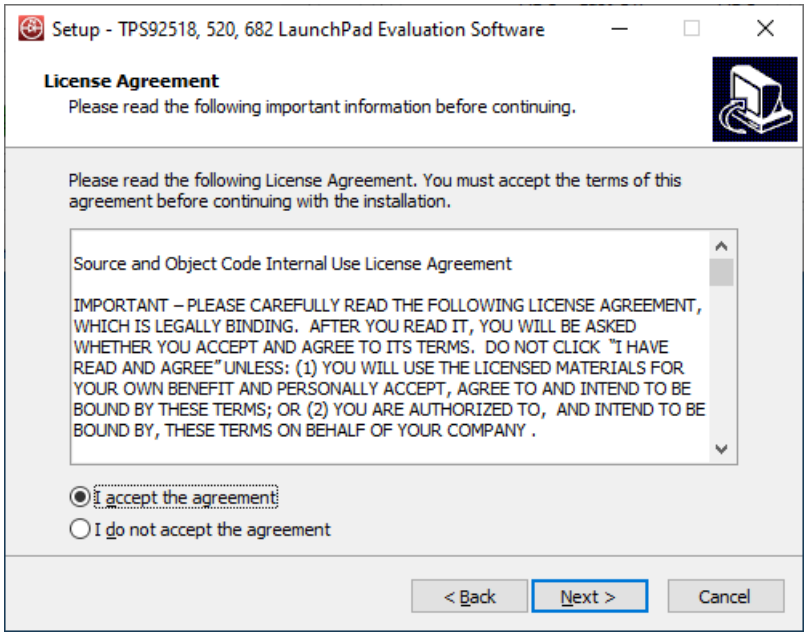


Figure 5-2. Setup Screen 2

Click **Next >** to accept the License Agreement.

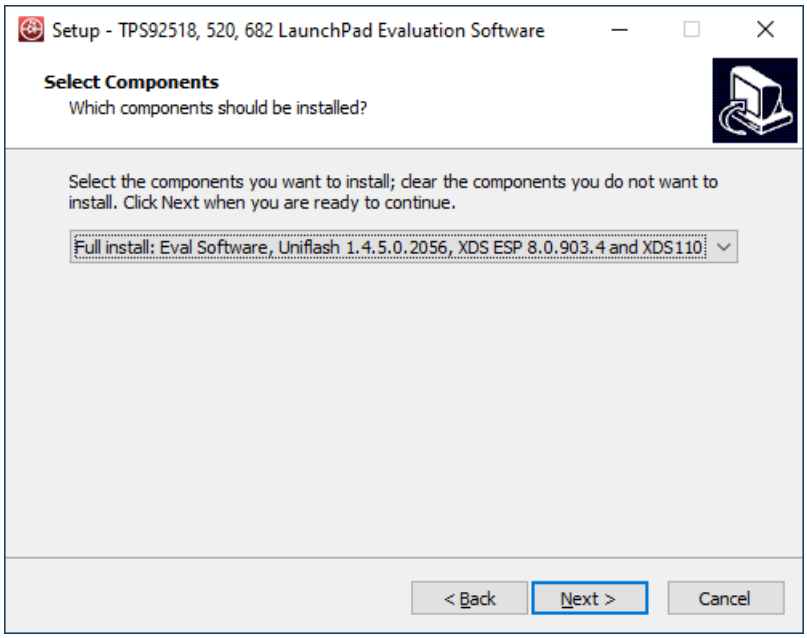


Figure 5-3. Setup Screen 3

Select **Full Install** and click **Next >** to install the evaluation software, the UniFlash, and the required XDS drivers. Full installation for both Windows 10 and 7 are provided.

Copyright © 2021 Texas Instruments Incorporated

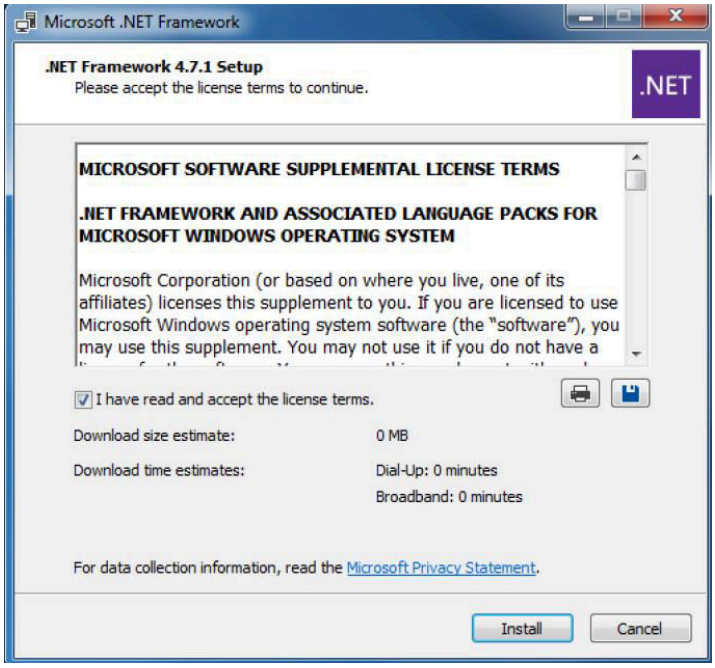


Figure 5-4. Setup Screen 4

If .NET Framework 4.5 or higher does not exist on the computer, the .NET Framework installation begins. Installation of .NET Framework will take several minutes. If .NET Framework 4.5 or higher exists on the computer, the installation jumps to the XDS driver installation.

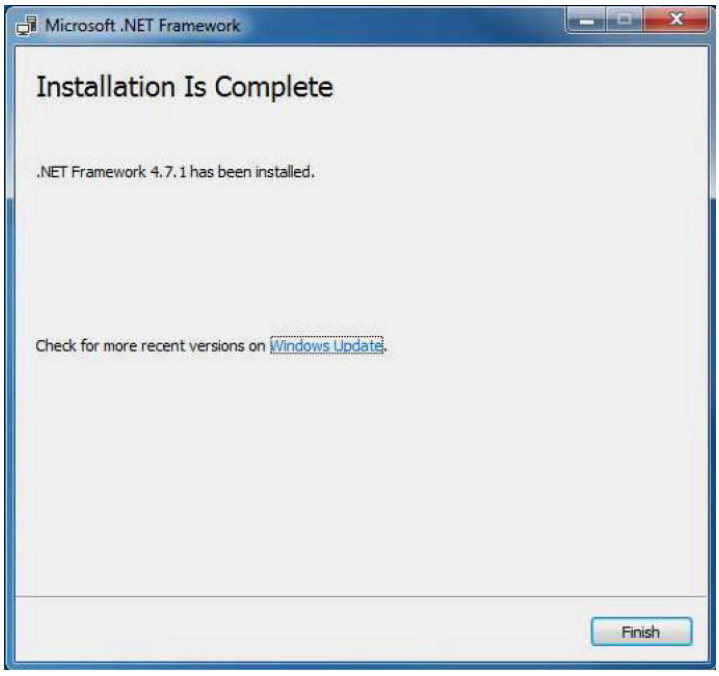


Figure 5-5. Setup Screen 5

A window appears indicating the completion of the .NET Framework installation.

Copyright © 2021 Texas Instruments Incorporated

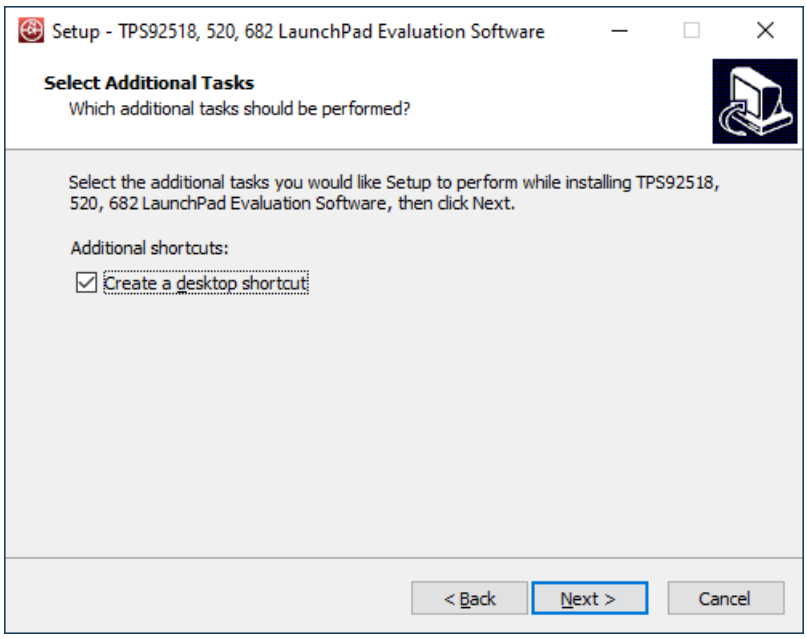


Figure 5-6. Setup Screen 6

Click next to proceed.

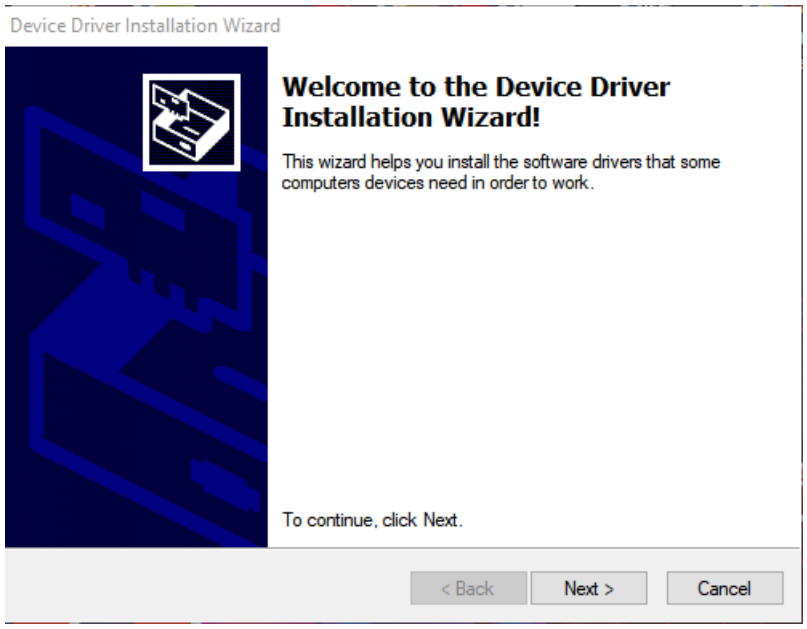


Figure 5-7. Setup Screen 7

Click the **Next >** button to install the XDS driver.

Copyright © 2021 Texas Instruments Incorporated

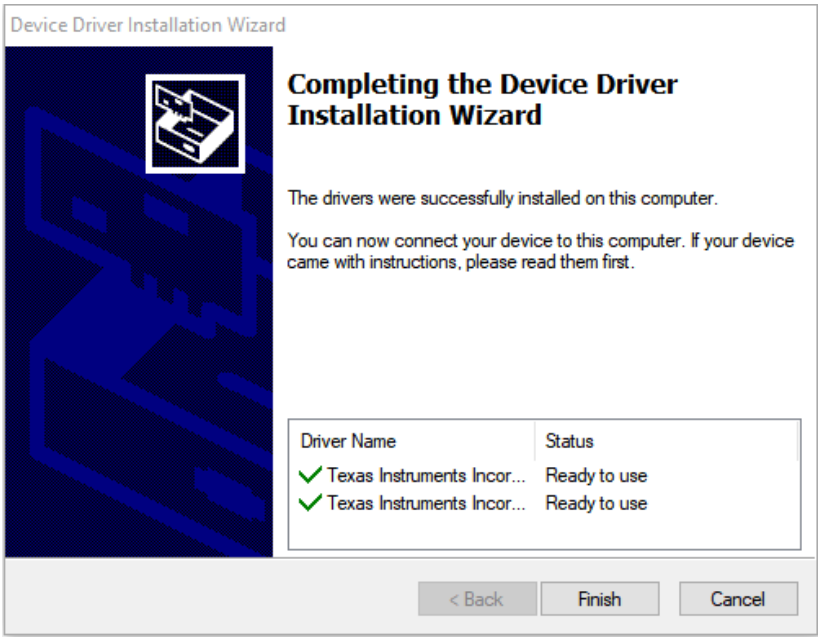


Figure 5-8. Setup Screen 8

The completion of the XDS driver installation is shown in Figure 5-8.

The TI-Emulators installation starts at this point. This will install the necessary drivers for running the application. In the next few steps as shown in Figure 5-9, Figure 5-10 and Figure 5-11 click **Next >** to perform the installation.

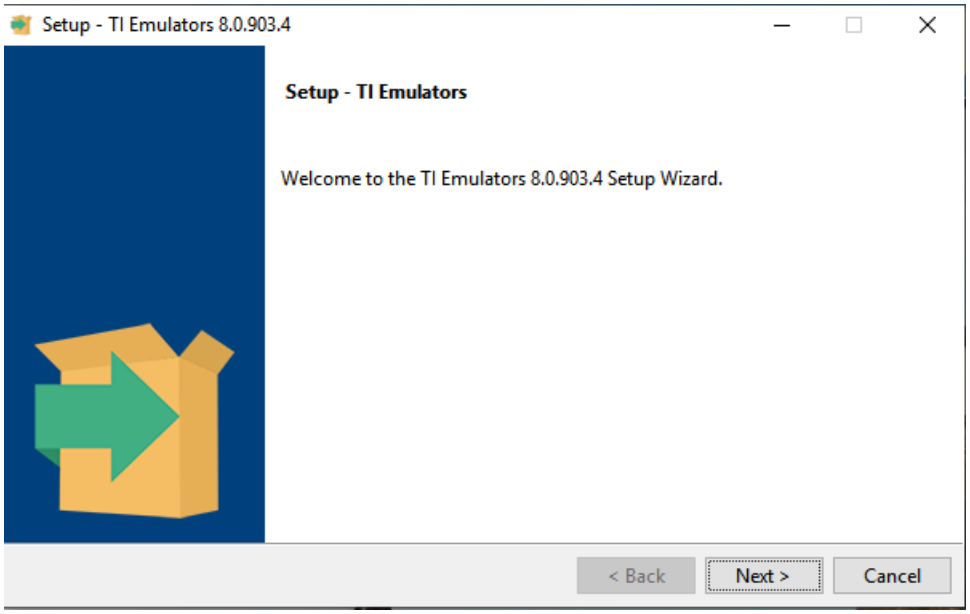


Figure 5-9. Setup Screen 9

Copyright © 2021 Texas Instruments Incorporated

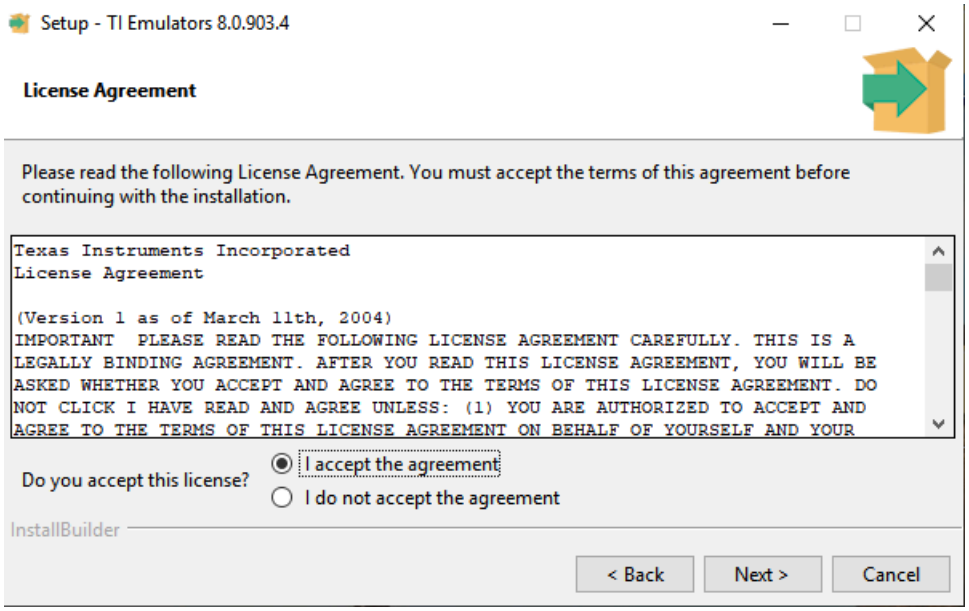


Figure 5-10. Setup Screen 10

Accept the license agreement in Figure 5-10.

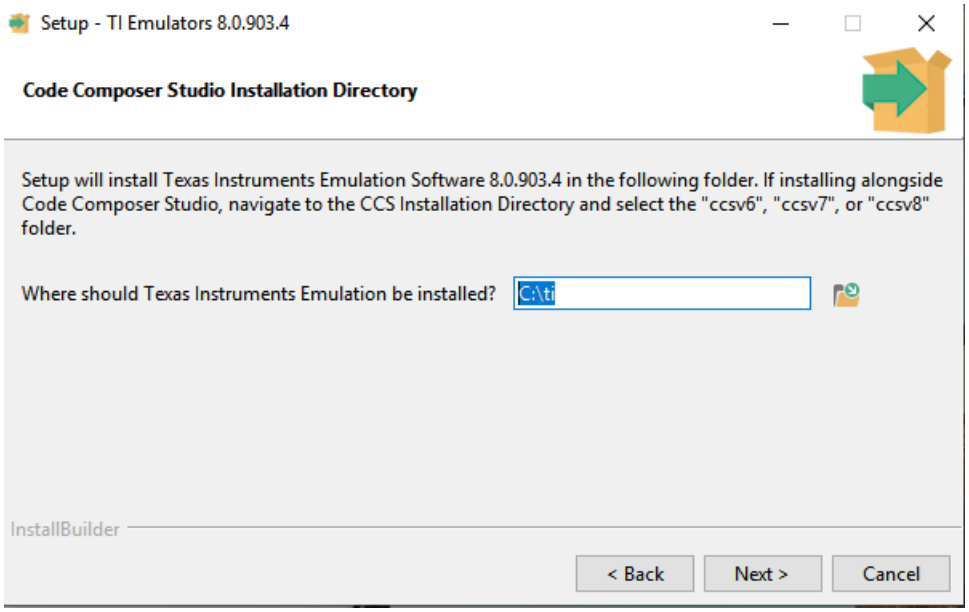


Figure 5-11. Setup Screen 11

Copyright © 2021 Texas Instruments Incorporated

In the next few windows click **Next >**, and if prompted by Windows Security about software installation as shown in Figure 5-12, select **Install**.

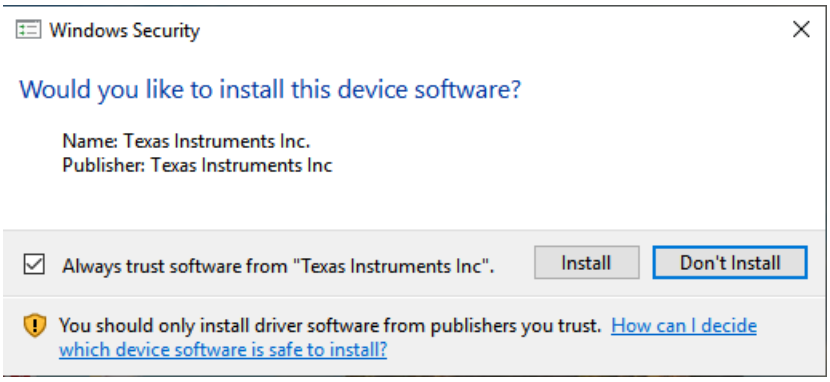


Figure 5-12. Setup Screen 12

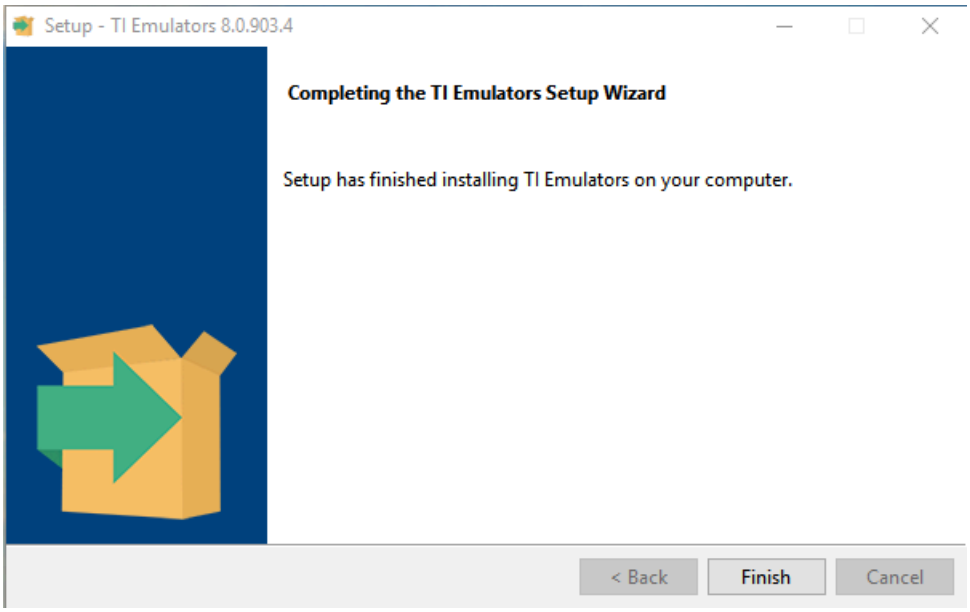


Figure 5-13. Setup Screen 13

The screen showing the completion of the TI Emulators installation is shown in Figure 5-13. Click on **Finish** to move to the next step.

Copyright © 2021 Texas Instruments Incorporated

The UniFlash installation starts at this point. UniFlash is required to program the LaunchPad. In the next few steps as shown in Figure 5-14, Figure 5-15 and Figure 5-16 click **Next >** to proceed and start the installation.

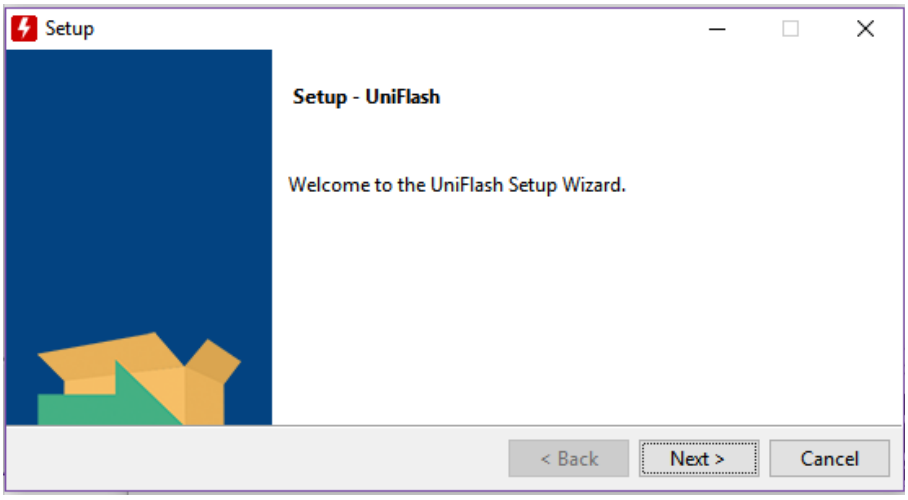


Figure 5-14. Setup Screen 14

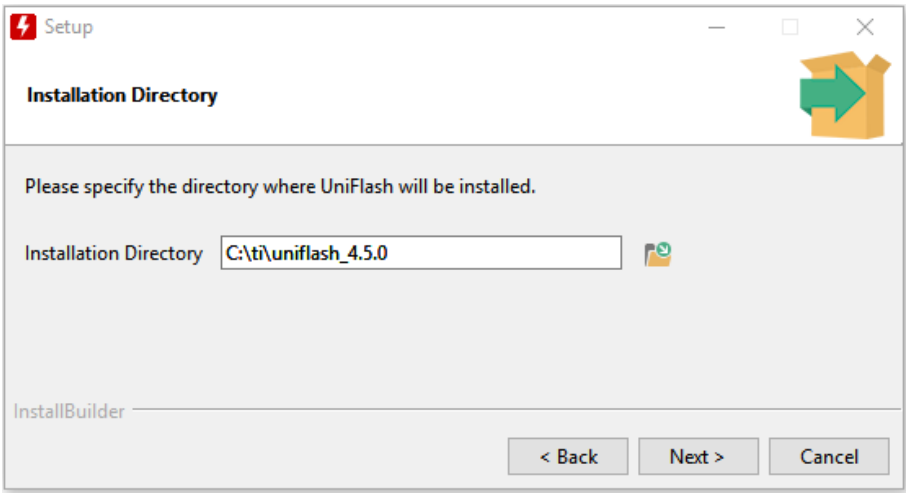


Figure 5-15. Setup Screen 15

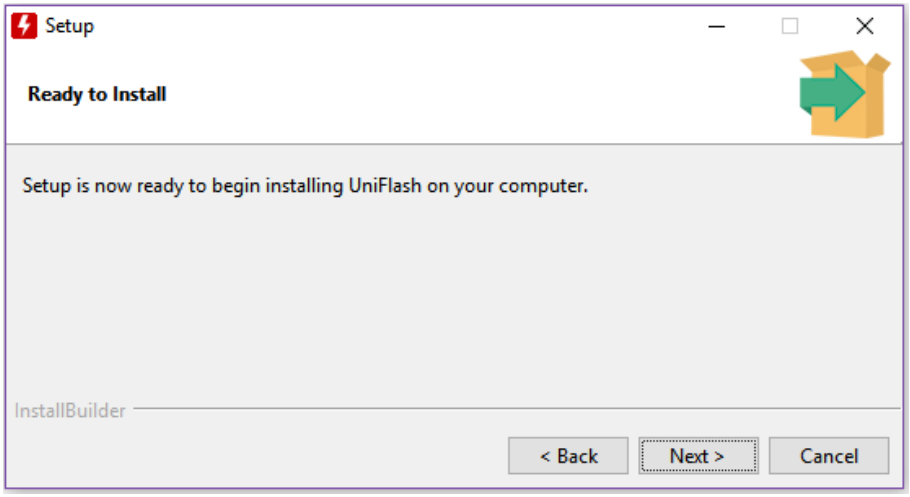


Figure 5-16. Setup Screen 16

Copyright © 2021 Texas Instruments Incorporated

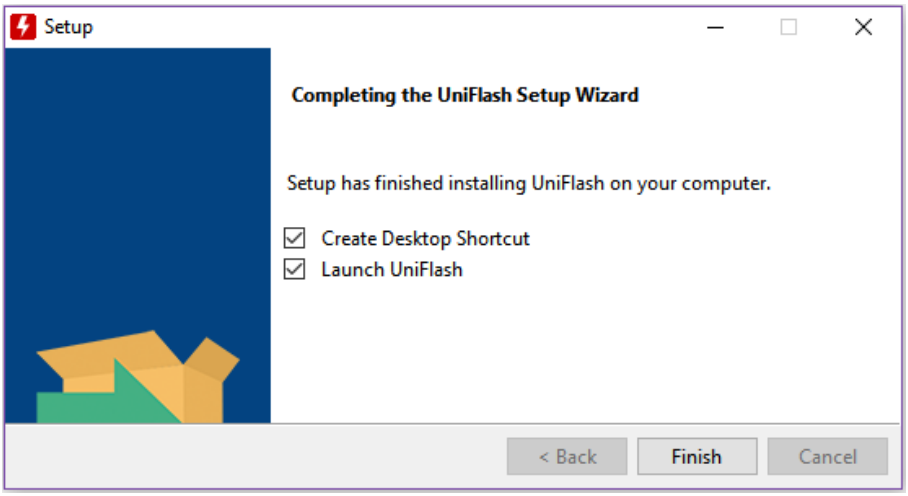


Figure 5-17. Setup Screen 17

When UniFlash installation is complete, click **Finish** to launch the UniFlash and program the LaunchPad.

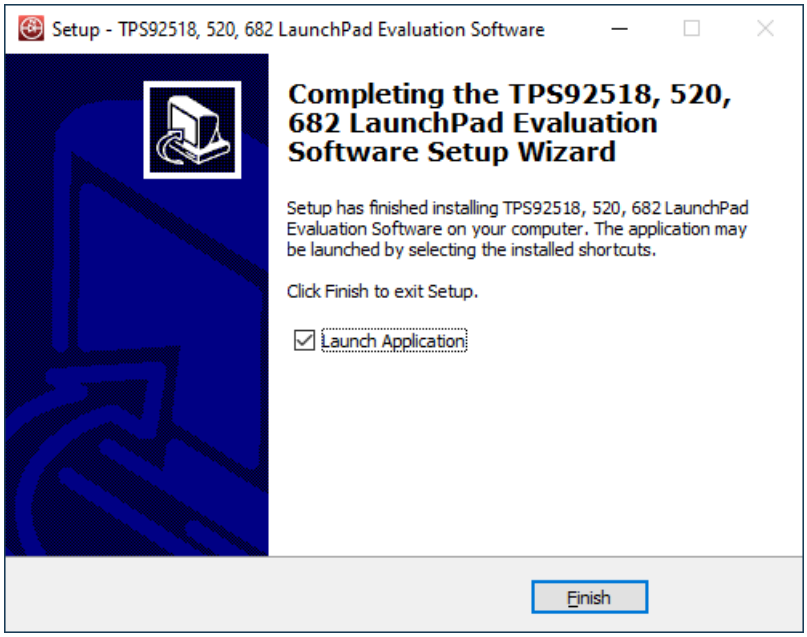


Figure 5-18. Setup Screen 18

Figure 5-18 shows the completion of the TPS92520-Q1 Evaluation Software . Un-check the **Launch Application** and click **Finish**.

Copyright © 2021 Texas Instruments Incorporated

5.3 Installation Error Recovery

If the screen shown in Figure 5-19 appears, use the following steps to install an unsigned driver one time.

1. Click **Start** and select **Settings**
2. Click **Update and Security**
3. Click **Recovery**
4. Click **Restart Now** under **Advanced Startup**
5. Click **Troubleshoot**
6. Select **Advanced Options**
7. Select **Startup Settings**
8. Click **Restart**
9. On the **Startup Settings** screen, press F7 during reboot to disable driver signature enforcement. The host computer restarts.
10. Repeat the entire re-installation process
11. A message appears informing that installing .NET failed. Close that window and continue.
12. Double-click **Install unsigned drivers**

After restarting a second time, the host computer resets. The reset requires all drivers to be digitally signed the next time a default installation executes, unless these steps are repeated.

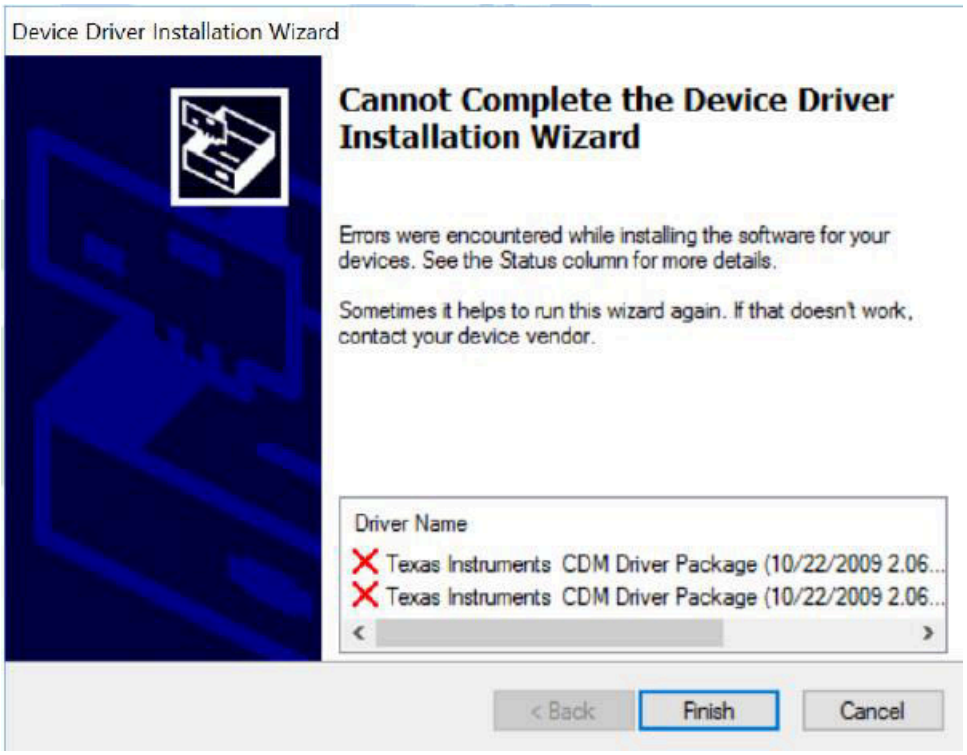


Figure 5-19. Setup Screen 19

Copyright © 2021 Texas Instruments Incorporated

5.4 Checking for Updates

This section shows the detailed instructions for checking if there is an update and how to install it. Run the TPS92518, 520, 682 LaunchPad Evaluation Software and go to the **Help** menu, see Figure 5-20.

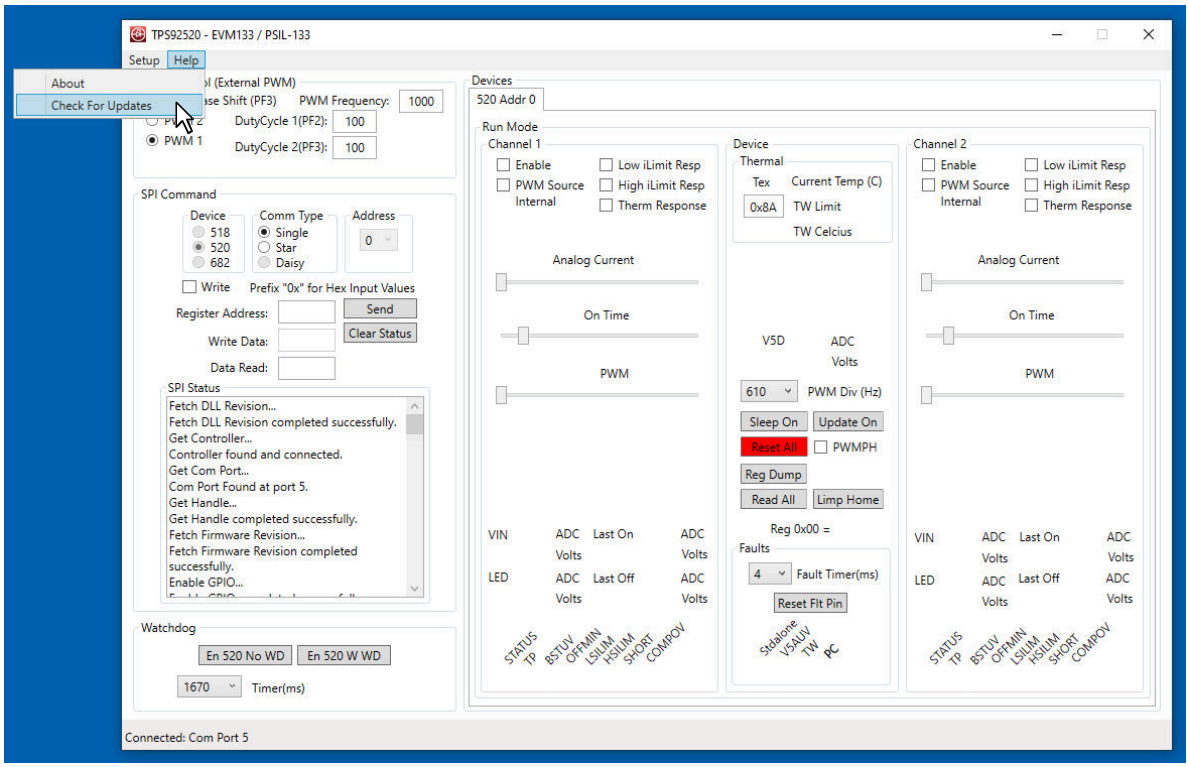


Figure 5-20. Help Menu and Checking for Updates

Click **Check for Updates >** to run updater.

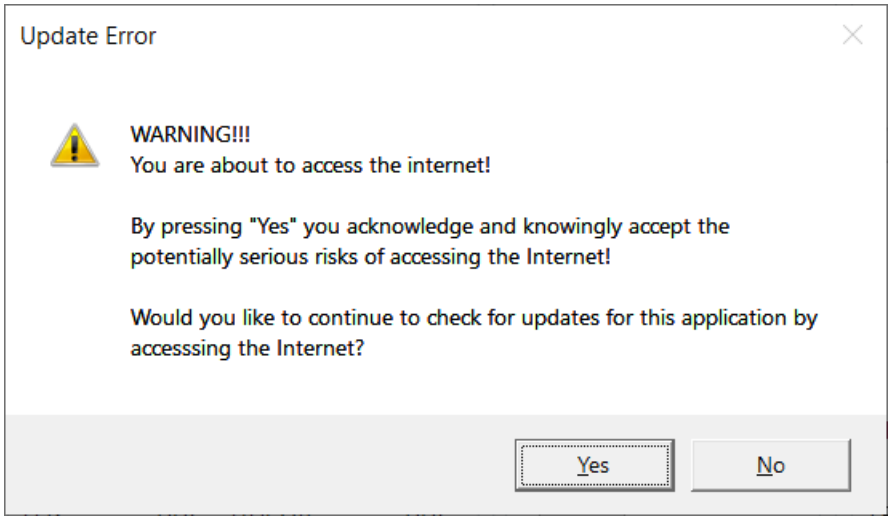


Figure 5-21. Update Screen 1

Click **Yes >** to accept risks for accessing the Internet.

Copyright © 2021 Texas Instruments Incorporated

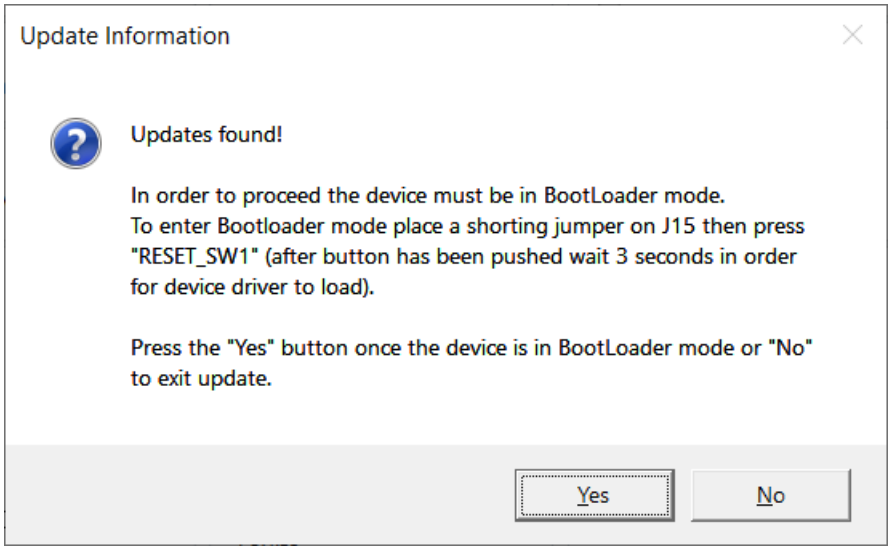


Figure 5-22. Update Screen 2

Go to the LEDMCUEVM-132 (PSIL-132) and locate J15 and **RESET_SW1**. Install shorting jumper at J15 locations as seen and then press the **RESET_SW1** as seen in Figure 5-23. This action places the MCU in Bootloader mode.

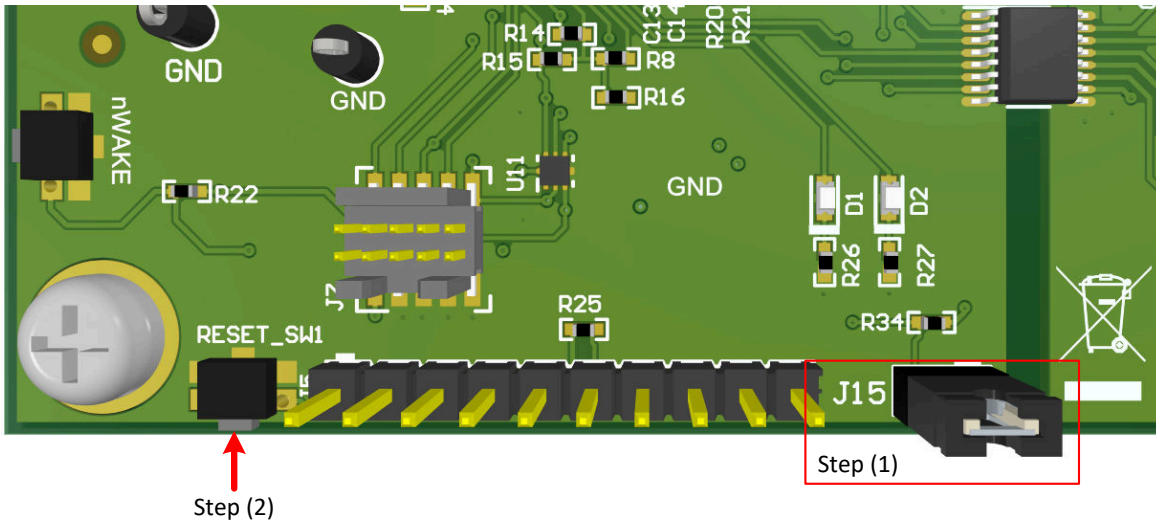


Figure 5-23. J15 Jumper and RESET_SW1 Switch for Bootloader Mode

Copyright © 2021 Texas Instruments Incorporated

Click **Yes >** to run the updater. The LPP Updater will run and once finished will ask if you would like to re-launch the GUI applications.

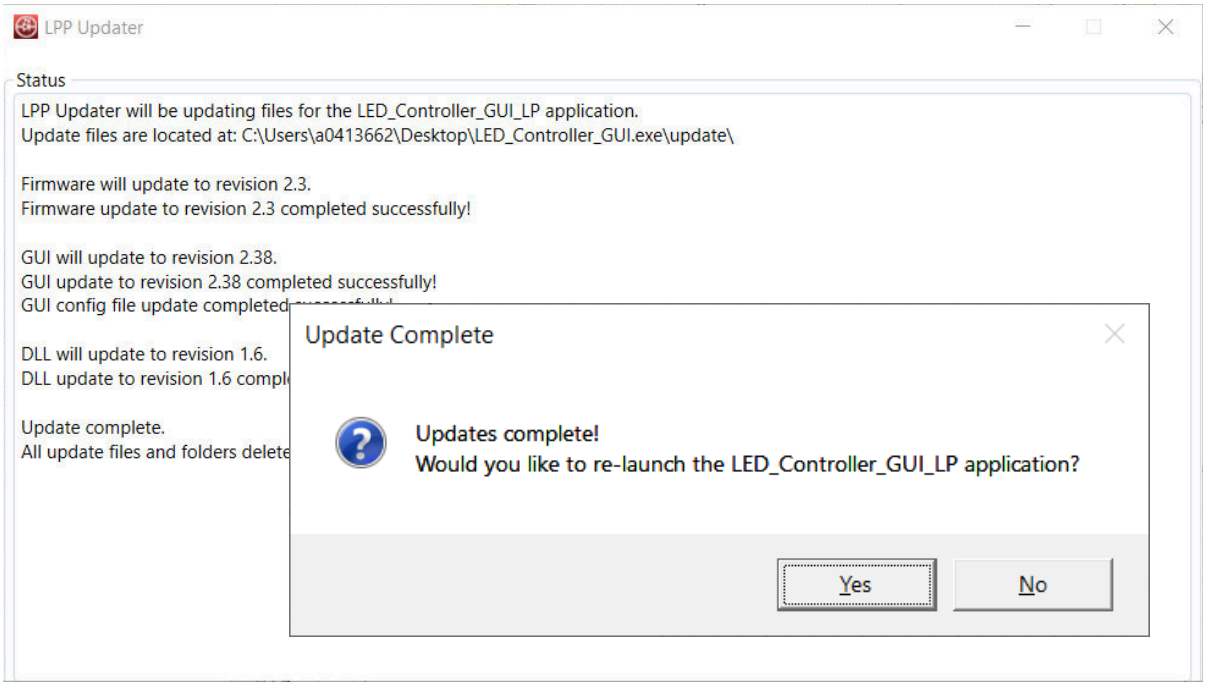


Figure 5-24. Setup Screen 5

Click **Yes >** to re-launch GUI.

A window appears indicating the the LEDMCUEVM-132 must be changed from bootloader mode to normal mode. This is accomplished by removing the shorting jumper from J15 then pressing the "RESET_SW1" switch and wait 3 seconds to ensure device drivers reload, see Figure 5-26.

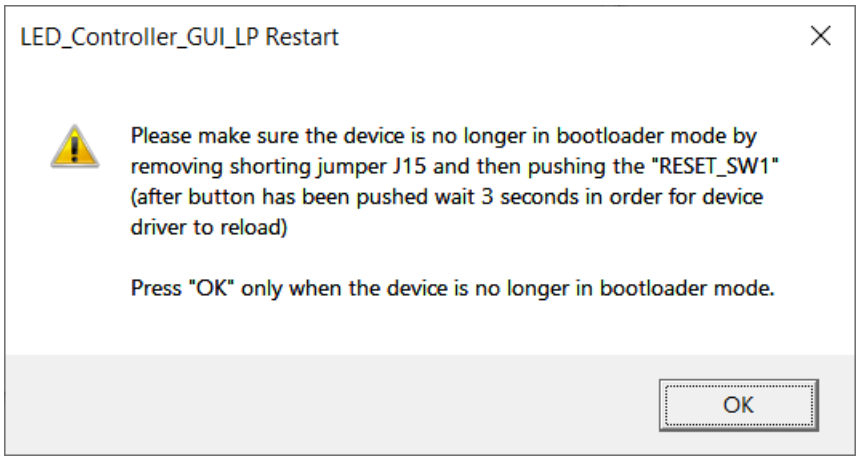


Figure 5-25. Setup Screen 6

Copyright © 2021 Texas Instruments Incorporated

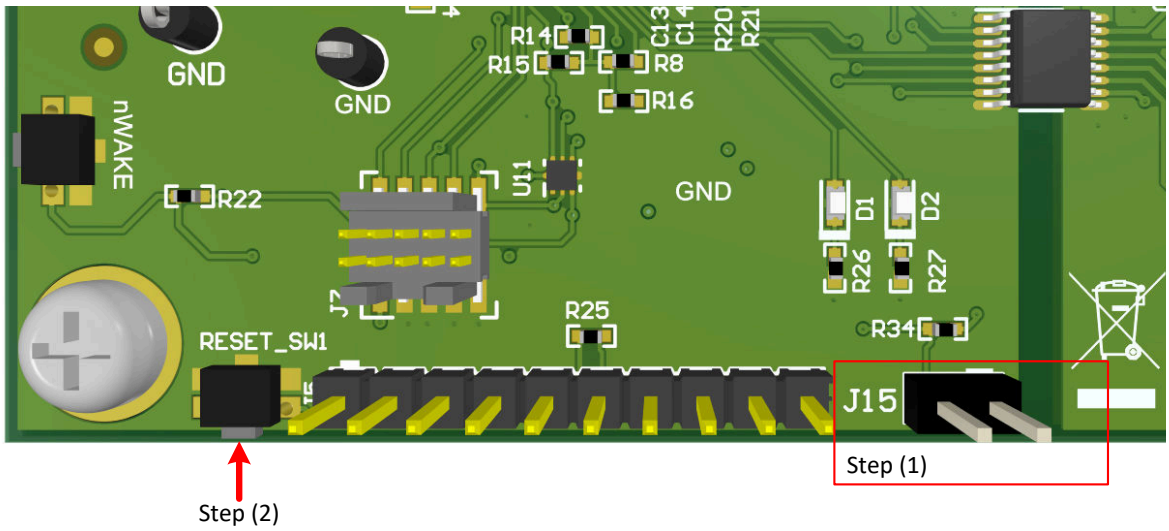


Figure 5-26. 15 Jumper and RESET_SW1 Switch for Normal Mode

Click the **OK >** button to restart the GUI.

Copyright © 2021 Texas Instruments Incorporated

6 TPS92520EVM-133 Power Up and Operation

To start the EVM operation, connect the header J9 on TPS92520EVM-133 to the header J9 on the LEDMCUEVM-132, and the header J3 to the header J6, as shown in Figure 6-1.

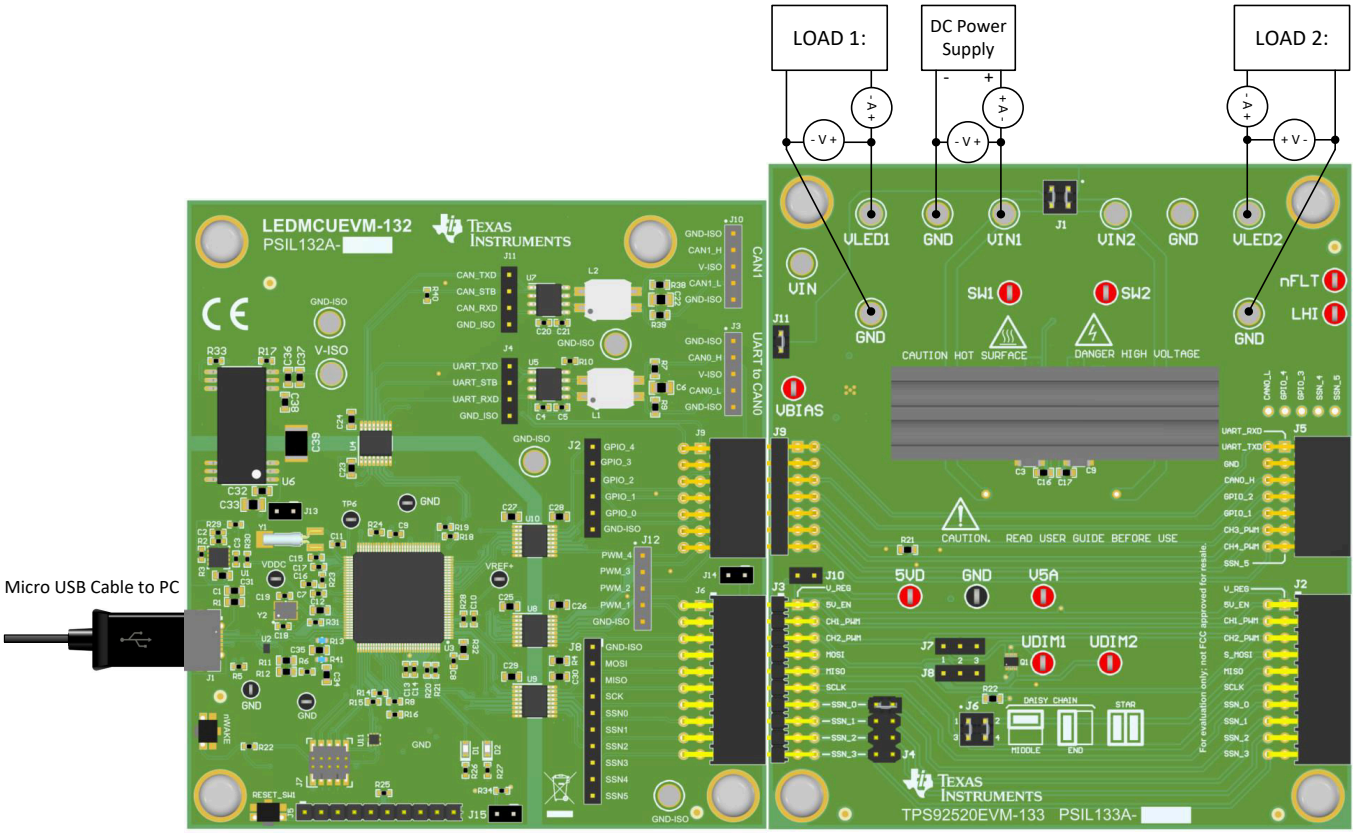


Figure 6-1. LEDMCUEVM-132 Connection to TPS92520EVM-133

Apply power (48 V) to the TPS9250EVM-133 board (terminal J1). Connect a resistive or a current sink load such as LEDs or diodes to the output of the EVM (terminal J2). The load must not exceed maximum output current of 1.6 A and the maximum output power of 120 W for two-channel operation. The following steps then provide the necessary setup to enable and turn on the TPS92520EVM-133.

The TPS92520EVM-133 board is setup such that the onboard linear regulator's (U2) input is connected to VIN through J11 and a series zener diode (D3) which reduced the input voltage to the linear's input below 40 V at a VIN of 65 V. The zener helps spread power dissipation between the linear and the zener and protects the linear from being exposed to voltages greater than 40 V.

Copyright © 2021 Texas Instruments Incorporated

6.1 Power Up and Operation at VINx < 40 V

To operate the TPS92520EVM-133 with less than 40 V, then J11 must be removed and the VBIAS test point (TP1) needs to be connected to VIN, assuming that it is below 40 V, or can be connected to an external power supply.

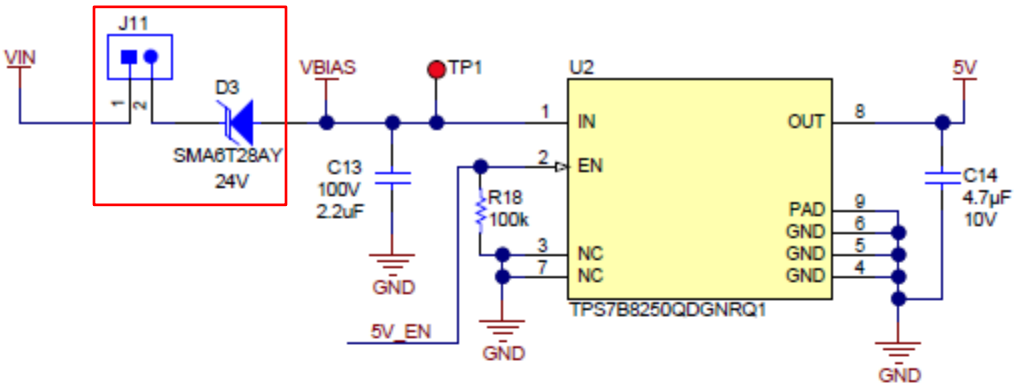


Figure 6-2. Input Voltage Selection Circuit Based on Operating Input Voltage

The TPS92520-Q1 can be setup with a resistor divider that sets the UVLO rising and falling. See the *TPS92520-Q1 data sheet* for additional information. Table 6-1 shows the V_{UDIM} rising and falling specifications from the data sheet. Always check the data sheet to verify no changes have occurred since publication.

Table 6-1. UDIMx and UVLO Specifications

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
PWM DIMMING and PROGRAMMABLE UVLO INPUT (UDIMx)						
$V_{UDIMx(EN)}$	UDIM input threshold sensed inductor current ripple	Rising		1.22	1.27	V
		Falling	1.075	1.120		V

The UVLO feature using a resistor divider on UDIM pins is described and outlined in the Figure 6-3 and Equation 1. See the data sheet for additional information.

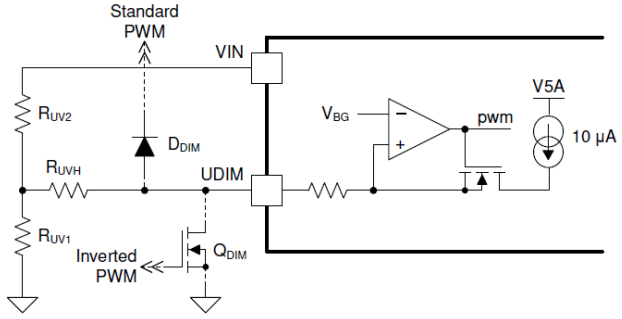


Figure 6-3. TPS92520-Q1 Diagram for UVLO Rising and Falling

$$V_{IN(RISE)} = V_{UDIM(RISE)} \times \left(\frac{R_{UV1} + R_{UV2}}{R_{UV1}}\right) \quad (1)$$

The TPS92520EVM-133 is setup such that each channel has a UVLO rising of 31.5 V. See Figure 6-4.

Copyright © 2021 Texas Instruments Incorporated

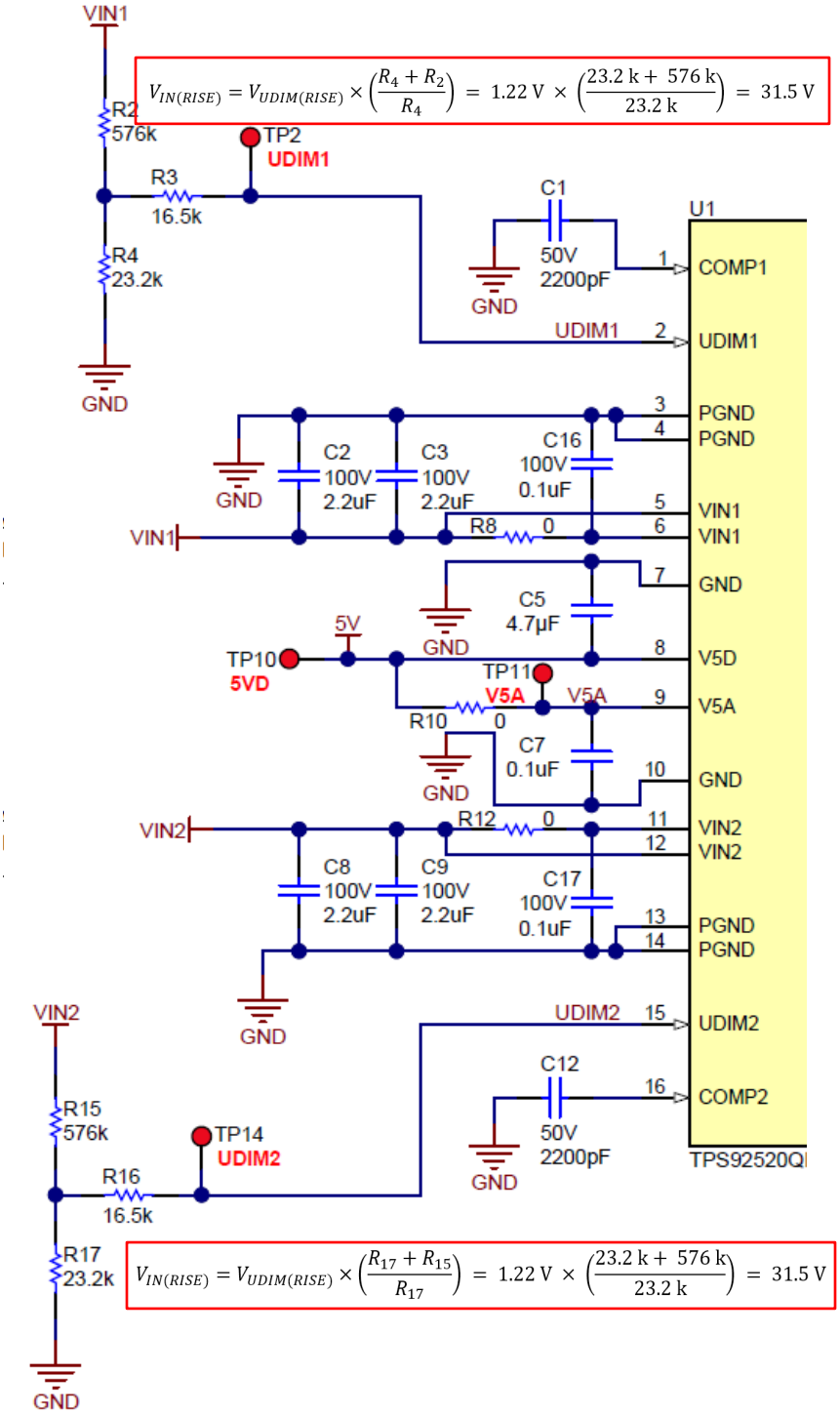


Figure 6-4. TPS92520EVM-133 UVLO Rising Schematic and Calculations

If the UVLO rising and falling needs to be disabled, then connect UDIM1 (TP2) and UDIM2 (TP14) to V5D. If the TPS92520EVM-133 is to be used below 40 V then see Figure 6-5.

Copyright © 2021 Texas Instruments Incorporated

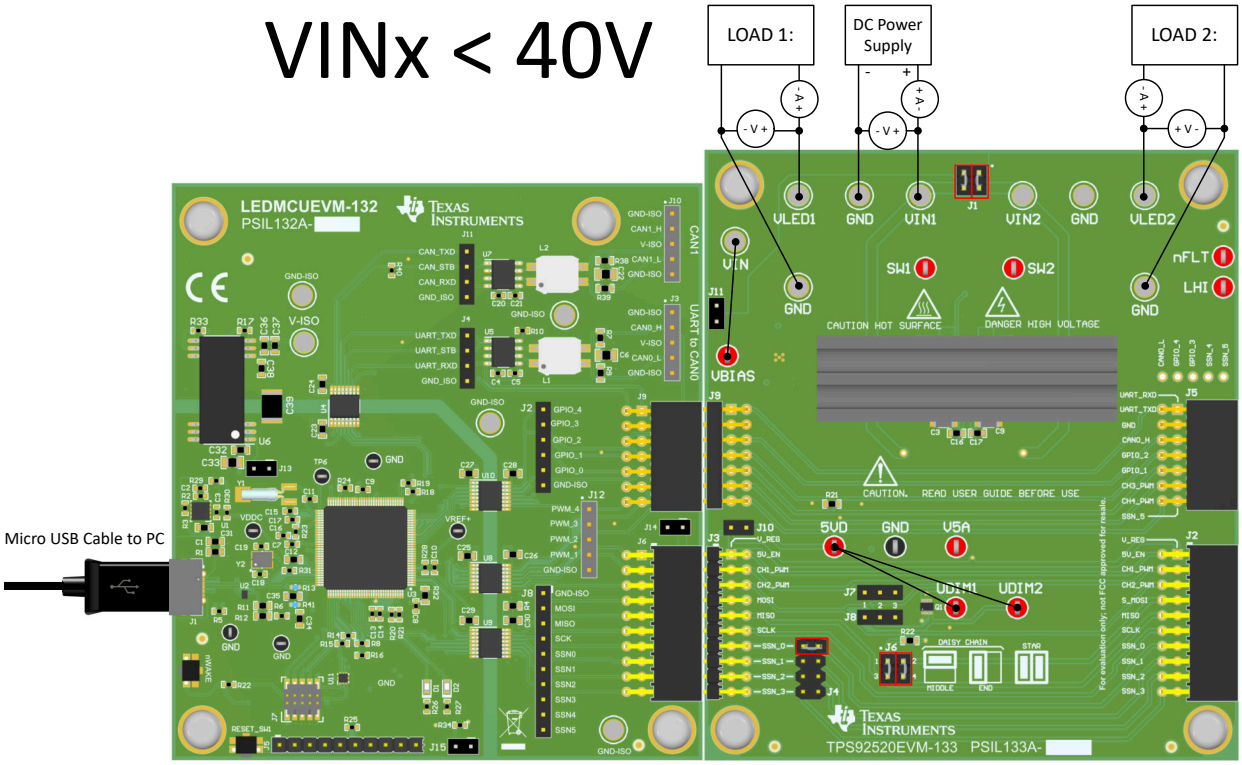


Figure 6-5. Connections for Operating the TPS92520EVM-133 at VINs Less Than 40 V and Having UVLO Disabled

Note that if UDIMx is attached to V5D, then only the internal PWM settings can be used. The other option is to adjust UVLO rising by changing R4 for channel 1 and R17 for channel 2 using the equation for $V_{IN(RISE)}$, which allows using external PWM dimming, see Figure 6-6.

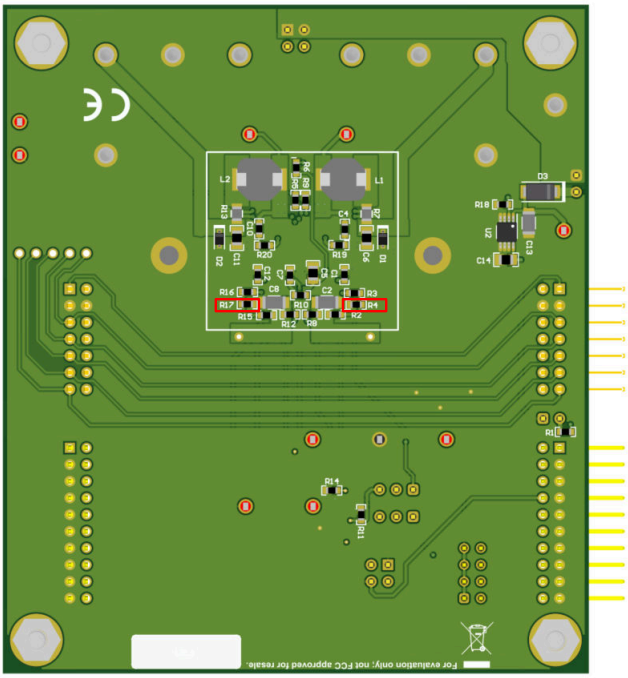


Figure 6-6. Bottom Side of TPS92510EVM-132 With UVLO Resistors of UDIM for Channel 1 and 2

Copyright © 2021 Texas Instruments Incorporated

6.2 MCU Control Window

Run the program **LED_Controller_GUI_LP.exe**, located at the *":\Texas Instruments\TPS92518, 520, 682 LaunchPad Evaluation Software"*, to start the GUI. The window shown in Figure 6-7 opens.

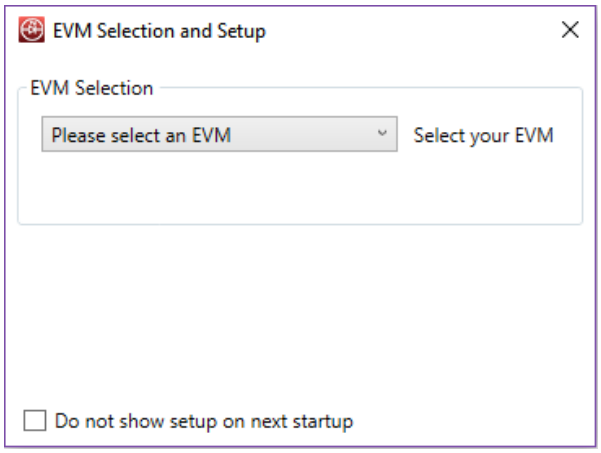


Figure 6-7. GUI Setup Screen 1

Click on the EVM selection option to select the TPS92520 - EVM133 - PSIL133.

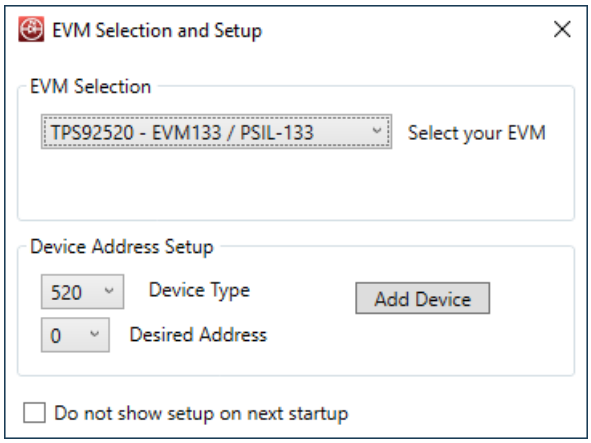


Figure 6-8. GUI Setup Screen 2

Select "0 for Desired Address (which is the default jumper setting, but can be changed). Click on Add Device.

Copyright © 2021 Texas Instruments Incorporated

The GUI will start up and show 4 separate windows (MCU Control, SPI Command, Watchdog, and Devices), see Figure 6-9.

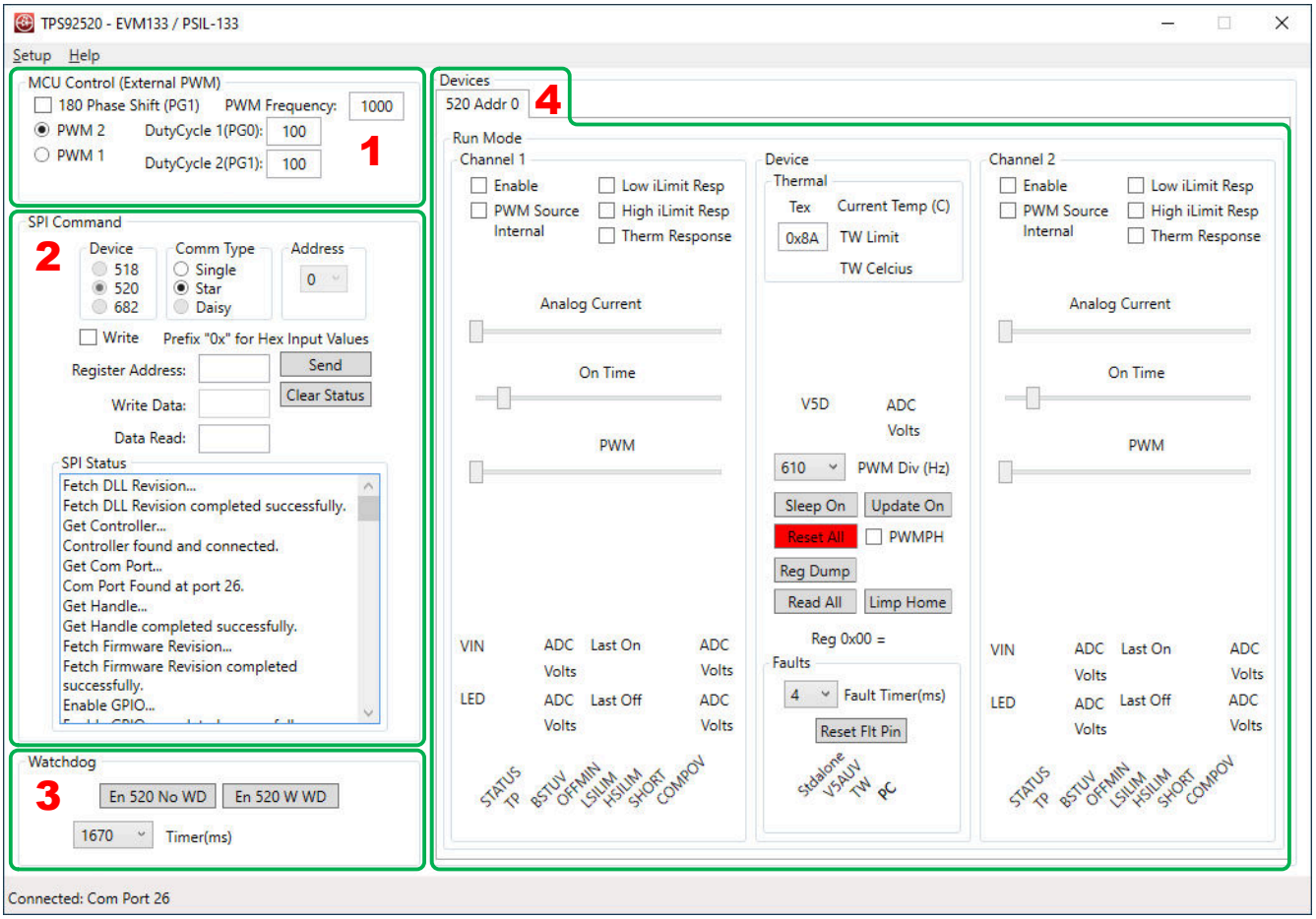


Figure 6-9. TPS92520 - EVM133 GUI Start-up Screen

The MCU Control window allows external control of the PWM dimming using the LEDMCUEVM-132 connections to the TPS92520EVM-133. PWM control is available for each channel with frequency and duty cycle control for frequencies and duty cycles that are not covered by the register settings. PWM control also allows for 180 degree phase shift in between channels if desired. For example, if a PWM signal of 4 kHz was desired, they can use this feature.

PWM 1 is the first PWM generator from the MCU and controls Duty Cycle 1 at PF2 pin of MCU and Duty Cycle 2 at PF3 pin of the MCU. PWM 2 is the second PWM generator from the MCU and controls Duty Cycle 1 at PG0 pin of the MCU and Duty Cycle 2 at GP1 pin of the MCU. PWM 1 generator signals connects to PWM1 (PF2) and PWM2 (PF3)on the TPS92520EVM-133 board. Therefore, the PWM 1 button must be selected when using the external that is controlled by the LEDMCUEVM-132.

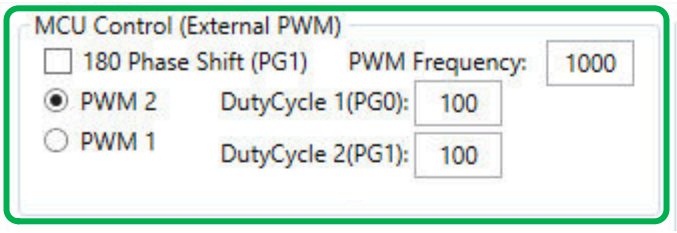


Figure 6-10. MCU Control (External PWM) Window

There are two jumpers that need to be selected to use this feature. J7 and J8 are not loaded with shorting jumpers by default and they allow for the direct connection of the external PWM from the LEDMCUEVM-132 by

Copyright © 2021 Texas Instruments Incorporated

placing a shorting jumper from pins 1 and 2 of J7 and J8. If the inversion of those PWM signals can be achieved by placing a shorting jumper across pins 2 and 3 of J7 and J8, see Figure 6-11.

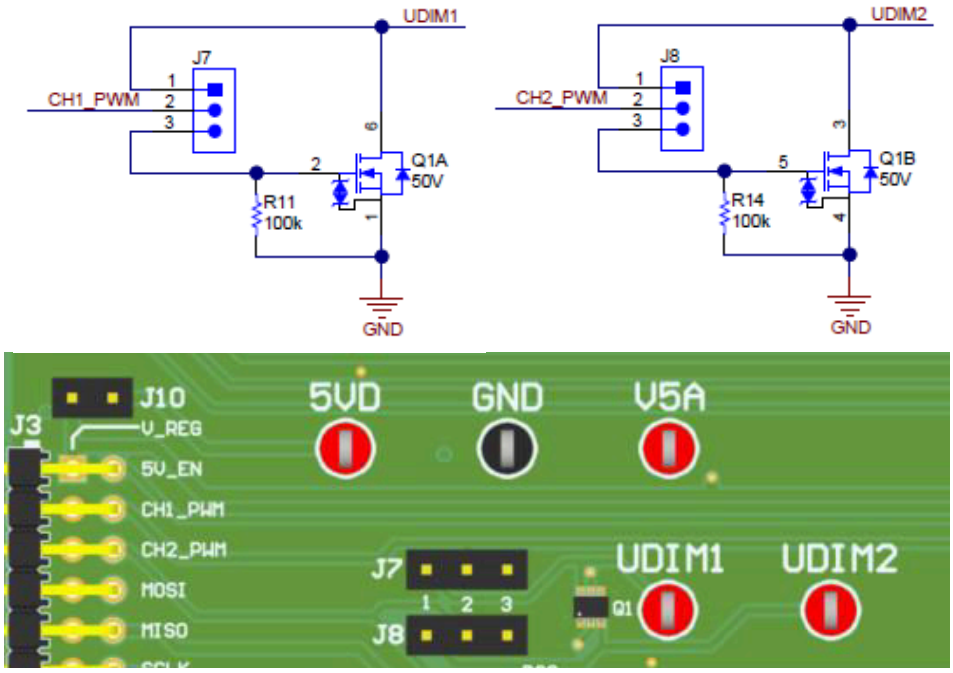


Figure 6-11. External PWM Hardware

Copyright © 2021 Texas Instruments Incorporated

6.3 SPI Command Window

The SPI command box allows register *read* and *write* actions and it also records the SPI status sequentially.

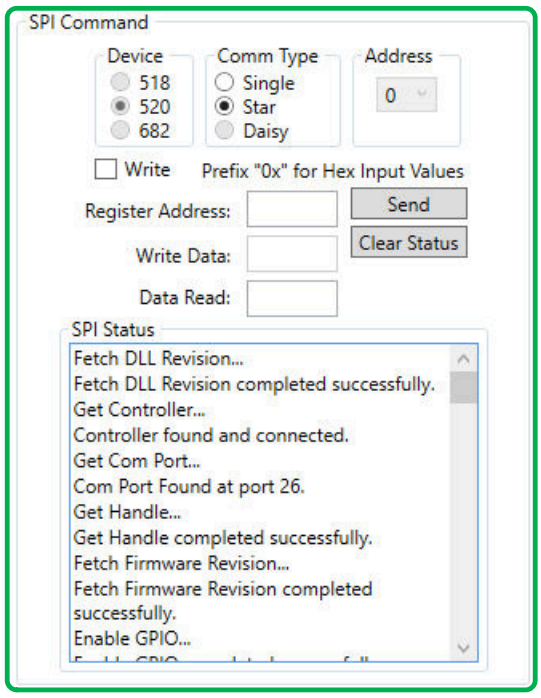


Figure 6-12. SPI Command Window

To ensure a connection from the board to the TPS92520-Q1 exists, perform the following steps as shown in Figure 6-12.

1. Write the register address eleven (0x11h), which is the CH1TON register, in the *Register Address* box: 0x11.
2. Double-click **Send**.

Copyright © 2021 Texas Instruments Incorporated

The default value of 0x07 for the register 11 will be shown in the SPI Status window, see Figure 6-13.

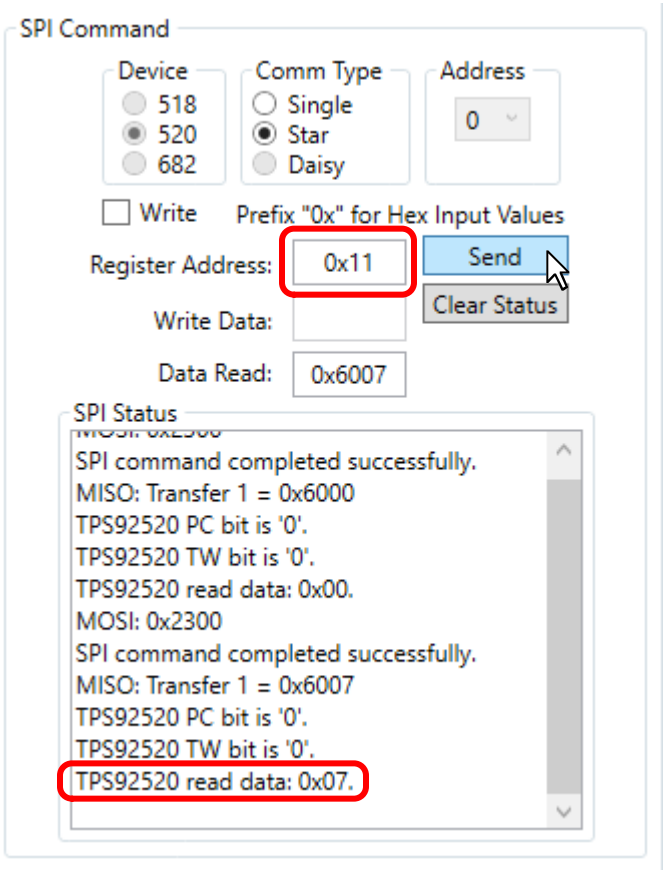


Figure 6-13. SPI Read Example

To write data to associated register address:

- Click the check box next to **Write**
- Write the desired data in the box next to **Write Data:** as shown in Figure 6-14.

Copyright © 2021 Texas Instruments Incorporated

- Click **Send**.

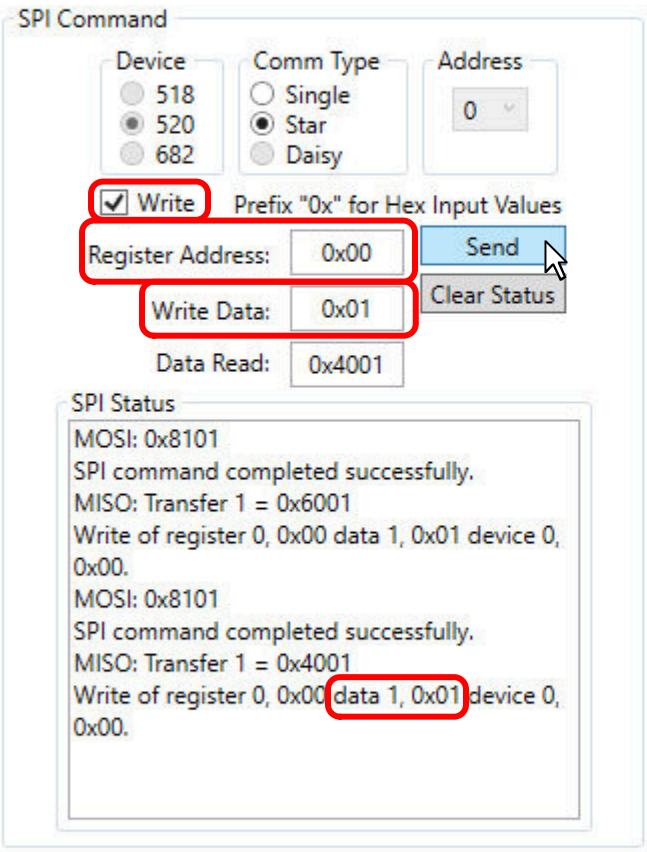


Figure 6-14. SPI Write Example

6.4 Watchdog Window

The Watchdog window allows you select either no watchdog timer or a watchdog timer along with the available timer lengths, which is by default 1.67 seconds.

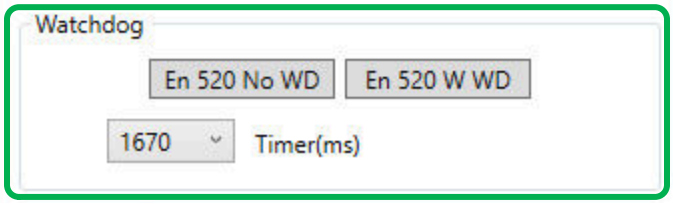


Figure 6-15. Watchdog Settings Window

Single click the "En 520 No WD" button. The button must be selected whenever using the EVM for general operation unless standalone mode wants to be initiated at startup, see Figure 6-16.

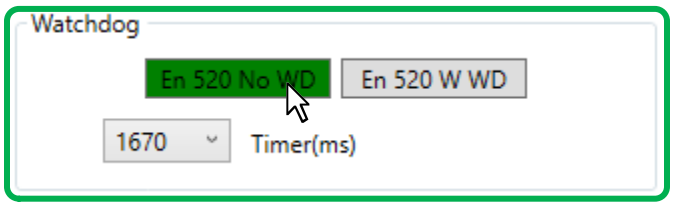


Figure 6-16. No Watch Dog Timer is Enabled

Copyright © 2021 Texas Instruments Incorporated

The GUI will automatically do read all the registers after the "En 520 No WD" button has been selected, which deselects the CMWEN bit, see figure Figure 6-17.

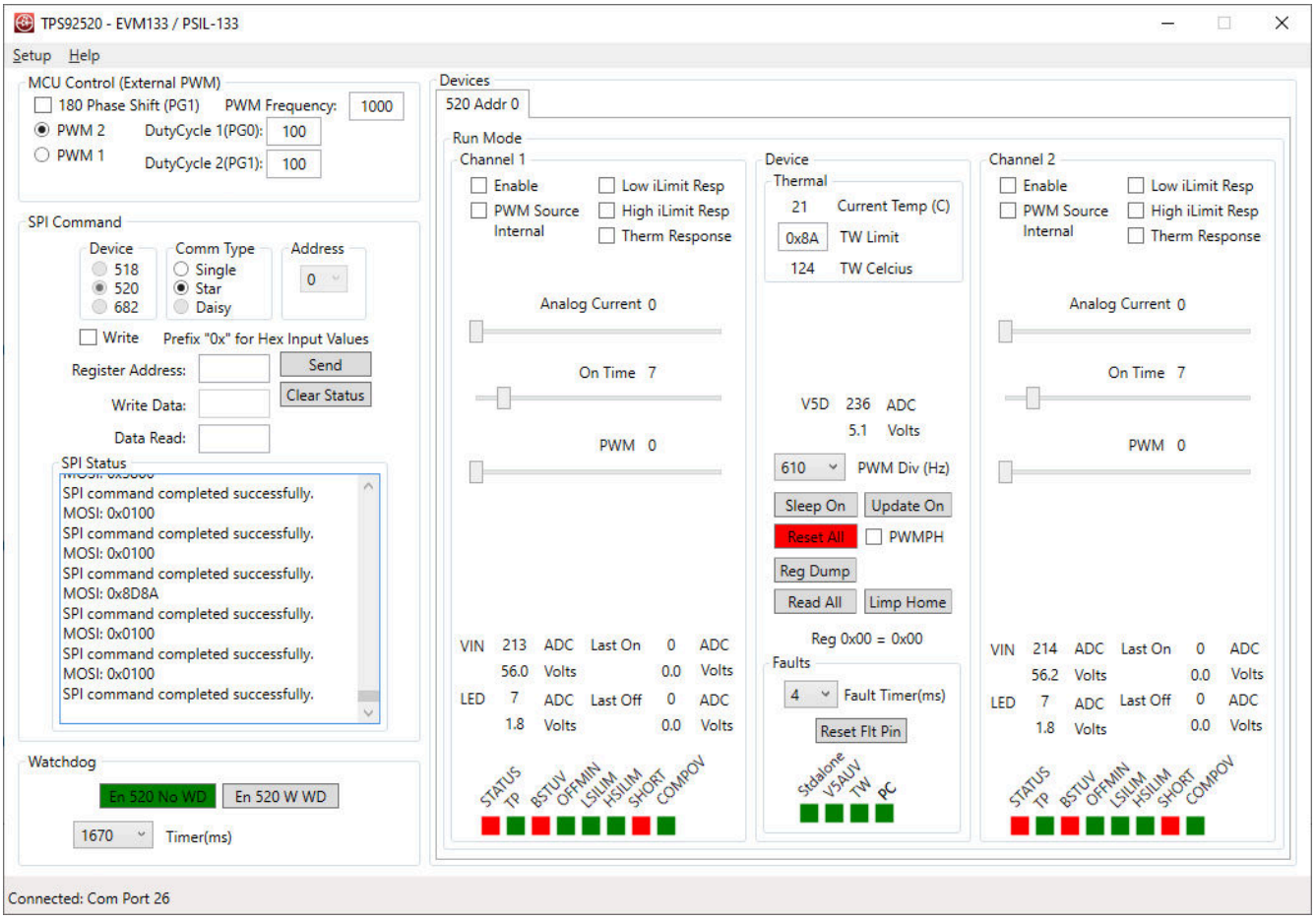


Figure 6-17. GUI After the "En 520 No WD" Button is Selected

Copyright © 2021 Texas Instruments Incorporated

6.5 GUI Devices Window

The device command window will not do any reads of the device until the **En 520 No WD** button has been selected and the watch dog timer has been disabled, see Figure 6-18 .

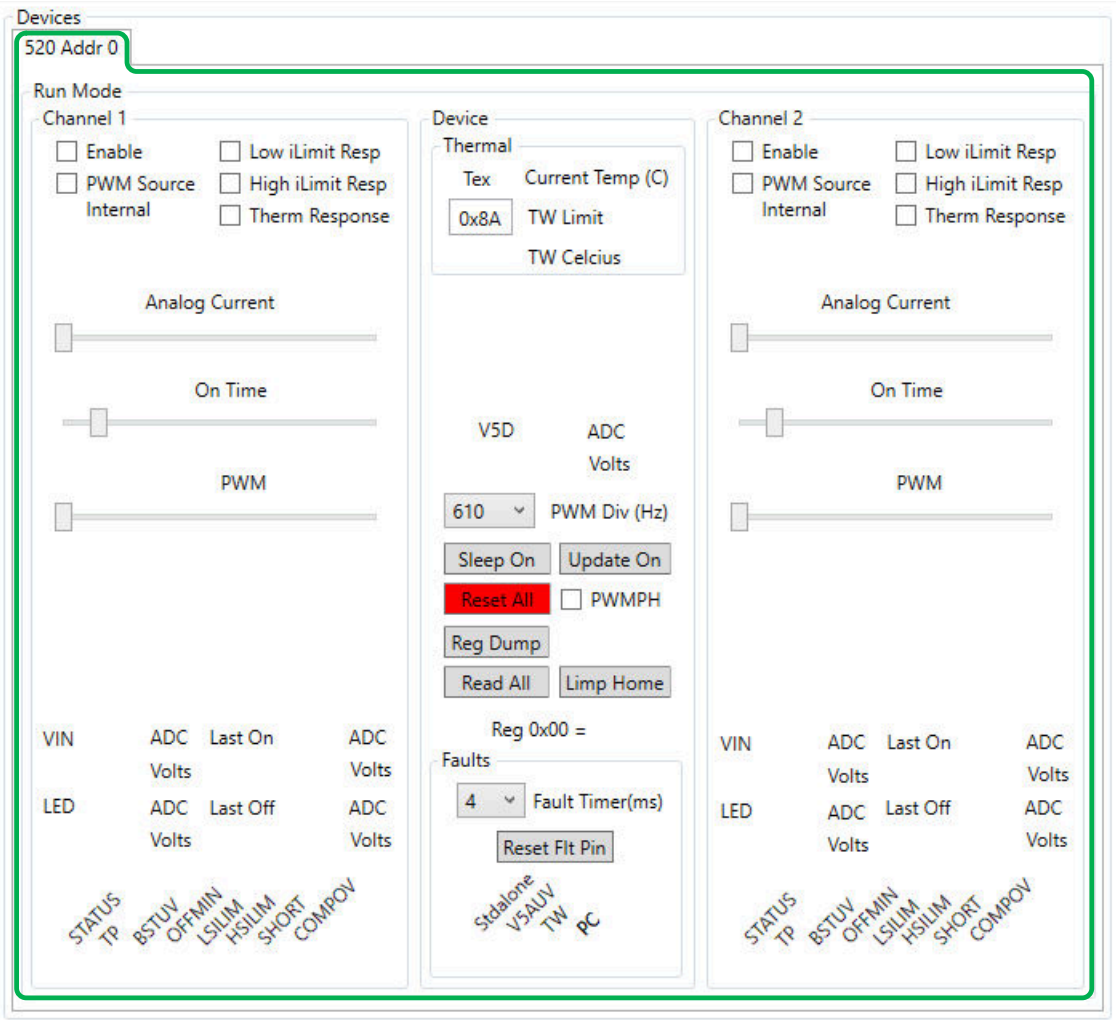


Figure 6-18. Device Command Window

Once the **En 520 No WD** has been selected, the GUI will perform an initial read of all the registers and load the information into the device command window, shown in Figure 6-19. Note that **SHORT**, **BSTUV**, and **STATUS** are flagged red because those faults conditions have occurred. The **SHORT** fault condition occurs because the output is off and no current is driving the LEDs and the voltage at the output is less than 2.45 V on the CSP pin, which indicates a **SHORT** condition. **BSTUV** fault indicates that the bootstrap supply is lower than 2.95 V, which is correct because the booststrap voltage is created when the output is turned on and the switch node is pulled to ground to charge the booststrap capacitor to drive the high-side FET. **STATUS** fault indicates that a fault has occurred and is the logic OR of the fault bits for that channel.

Copyright © 2021 Texas Instruments Incorporated

The GUI is split up into different sub windows for each the **Devices**. There can be multiple tabs (Devices) and each tab will be for a specific device at at specific SPI address. Figure 6-19 shows the TPS92520 (520) as the device and the address (Addr) is 0.

Figure 6-19. Devices Window After Watchdog is Disabled

There are sub-windows for each channel (**Channel 1** and **Channel 2**) and the **Device** sub-window for shared features. The **Device** window covers features for the device such as thermal, faults, fault timer settings, PWM frequency, limp home mode, 5VD measurements, fault resets, sleep mode, and register reads. Each channel window sets the LED current (Analog Current), switching frequency (On Time), the PWM duty cycle (PWM), PWM source (Internal or External UDIM pin), fault response settings, and if the channel is enabled or not. The channel windows also have information about input voltage (V_{IN}) and output LED voltage (LED) measurements. There are also the associated status information such as fault flags that are tied to each channel.

Copyright © 2021 Texas Instruments Incorporated

6.5.1 Channel 1 or 2 Sub-Window: Settings, Measurements, and Faults

The **Channel Sub-Window** is broken down into basic features and settings set by selecting boxes or slide, measurements of V_{IN} and LED, and fault status boxes (see Figure 6-20).

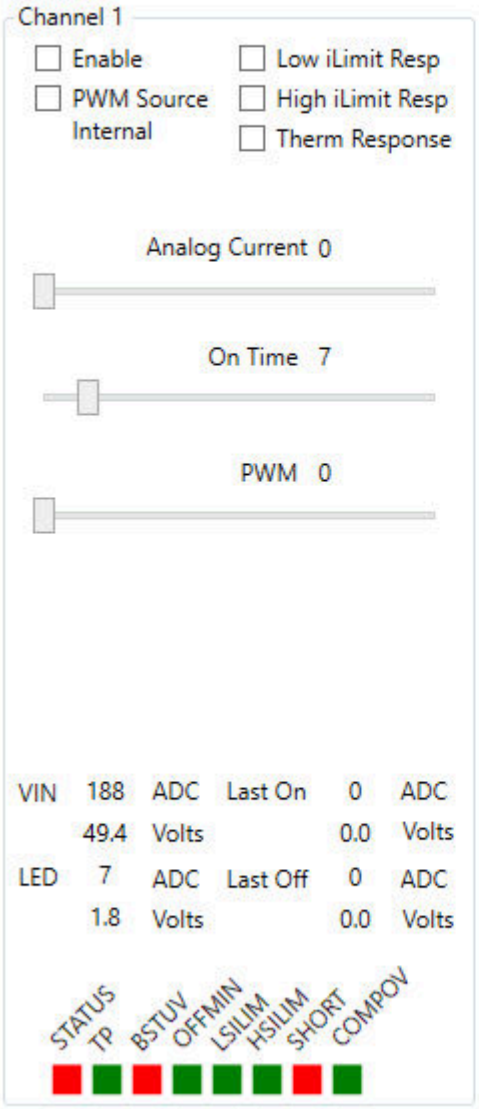


Figure 6-20. Channel 1 Window - Configurations, Measurement, and Fault Window

There are three slide bars that can be adjusted. The **Analog Current** bar sets the CHxIADJ registers to control the reference voltage (V_{IADJ}) used for setting the LED current of that channel. It has a decimal value from 0 to 1023, which coincides with voltage from 0 to 2.45 V to the V-I Converter, see the *LED Current Regulation and Error Amplifier* section of the *TPS92520-Q1 data sheet* for additional information. The current setpoint is also a function of the selected current sense resistor. The TPS92520EVM-133 uses a 100-mΩ resistor and to get 1 A at the output then slide bar must be move to 586 (decimal value), see Figure 6-21.

Figure 6-21. Analog Current Slide Bar

The **On Time** slide adjust CHxTON registers which controls the switching frequency of the constant current LED buck driver, see Figure 6-22. The default value is 7 (decimal) which coincides with a 437-kHz switching

Copyright © 2021 Texas Instruments Incorporated

frequency. The switching frequency ranges from 100 kHz to 2,200 kHz, see the *Switching Frequency and Adaptive On-Time Control* section of the *TPS92520-Q1 data sheet* for detailed calculations. The EVM is optimized to operate at the default switching frequency.

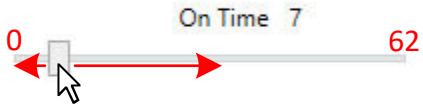


Figure 6-22. On Time Slide Bar for Changing Switching Frequency

The **PWM** slide adjusts the internal 10 bit PWM duty cycle (CHxPWM registers) from 0 to 1023, which coincides with 0 (off) and 1023 (full ON), see Figure 6-23. For example, if you want to operate at a 50% duty cycle slide the bar to 512 (decimal value), which is half of the full scale of 1024 or 50%. The **PWM Source Internal** box much be selected for the PWM slide bar setting to be implemented. The **PWM Source Internal** box sets the CHxINTPWM bit high and enables the use of the internal PWM registers to generate the PWM function for that channel.

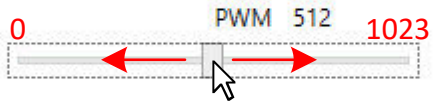


Figure 6-23. Internal PWM Duty Cycle Slide Bar

The **Enable** box set the CHxEN bit to 1 for that channel, which means the associated channel is turned on, see Figure 6-24.

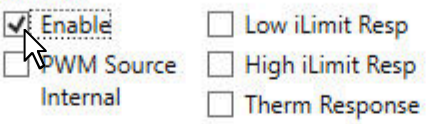


Figure 6-24. Channel Feature Selection Boxes

The **PWM Source Internal** controls the CHxINTPWM register. If the box is selected then the device uses the register settings for **PWM** slide bar to determine the PWM duty cycle and uses the PWMDIV register to set the PWM frequency. Note that the PWM frequency (PWMDIV register) sets the frequency for both channels. If this box is not selected then then the device does PWM dimming based on the signal seen on the UDIM x pins for each respective channel. The frequency and duty cycle are independent.

The *Low iLimit Resp*, **High iLimit Resp**, and **Therm Response** buttons coincide with setting the device to auto-restart after a fault time (IFT register setting) has elapsed or if it will latch off when the fault occurs. If box is selected then the device will latch off when the fault occurs and then reset the EN bit to the default of 0 (off) and will only continue to run when the EN bit is set to 1 (enabled).

Each channel window also reads the input voltage (V_{IN}) and the output LED voltage (LED) at the CSNx pin for each respective channel using the internal ADC of the device. **VIN** is a reading of the CHxVIN registers and **LED** is a reading of CHxVLED registers, see Figure 6-25.

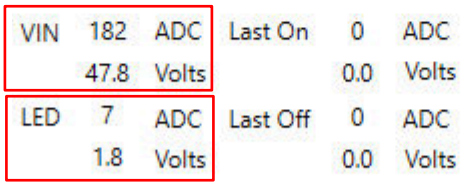


Figure 6-25. VIN and LED Voltage Measurements From Internal ADC

At the bottom of the channel window are several boxes, that are either red or green, that indicate the status of specific warnings or faults, see Figure 6-26. The **STATUS** box reads the CHxSTATUS bit and is logic OR of

Copyright © 2021 Texas Instruments Incorporated

all the fault bits for that channel with the exception of the overtemperature thermal warning bit. The "TP" box reads the CHxTP bit and indicates overtemperature thermal protection for that channel. The BSTUV box reads the CHxBSTUV bit and indicates the boostrap undervoltage fault condition where the BSTx voltage is less than 2.95 V. The OFFMIN box reads the CHxOFFMIN bit and indicates if the maximum duty cycle of that channel has been reached. The LSILIM box reads the CHxLSILM bit and indicates that the low-side switch current limit fault has occurred on that channel, which is 1.5 A typical. The HSILIM box reads the CHxHSILIM bit and indicates that the high-side switch current limit fault has occurred on that channel, which is 2.7 A typical. The SHORT box reads the CHxSHORT bit and indicates output short circuit fault on that channel, which means the CSPx pin is less than 2.45 V. The COMPOV box reads the CHxSHORT bit for each channel and indicates that an overvoltage condition on the COMPx pin, which indicates the COMPx pin is greater than 3.2 V.

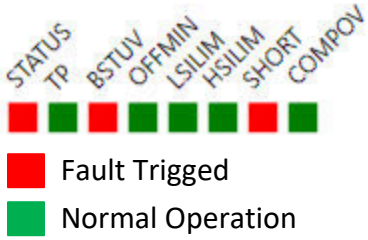


Figure 6-26. Status Indicators for Channels

6.5.2 Device Sub-Window: Shared Device Settings, Measurements, Register Info, and Limp Home

Copyright © 2021 Texas Instruments Incorporated

The **Device** window show a variety of measurements, faults, and settings for the device that are not specific to a channel, see Figure 6-27.

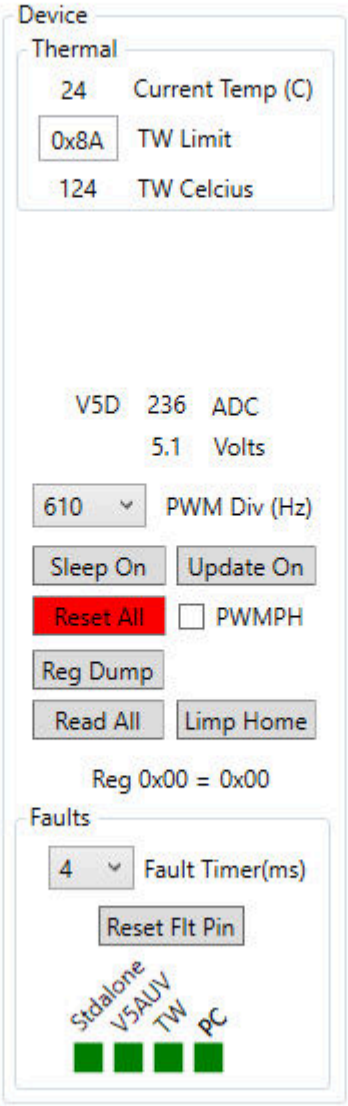


Figure 6-27. Device Window - Channel and Systems Voltage Measurements

The **Thermal** window, Figure 6-28, shows the **Current Temp** which is a reading of the TEMPL/H registers. The **TW Limit** is a setpoint for the thermal warning limit that is defined in the TWLMT register. If the **Current Temp** exceeds the **TW Limit** then the TW bit is set. The **Device** window also shows the measured voltage of the V5D pin using the internal ADC.

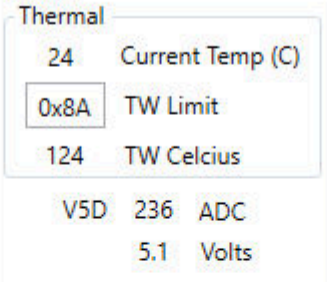


Figure 6-28. Temperature, V5D Measurement, and TW Setpoint

The pull-down menu for **PWM Div (Hz)** selects the PWM frequency that is to be used by both channels if the **PWM Source Internal** box is selected for that channel. The **SLEEP** button sets the SLEEP bits such that it goes

Copyright © 2021 Texas Instruments Incorporated

into a low-power mode yet still keeps all the register information. The **Limp Home** button opens up a window with the limp home settings, see the *Limp Home Mode Window* section. The **Update** button initiates the polling of all the registers and continually refreshes the GUI with the information from the EVM. It is important to note that when using the **Update** mode, that faults can occur and be visually missed because the register reads clear the faults in the polling cycle. The **Read All** button performs a single read of all the registers and updates the GUI. The *Reg Dump* button does a read of all the registers and creates a .txt file with all the register information in the local drive at C:\Texas Instruments\TPS92518, 520, 682 LaunchPad Evaluation Software location. The **Reset All** button put the TPS92520-Q1 to its factory default settings.

Figure 6-29. Internal PWM Frequency Set-Point, Sleep Mode, Reading Registers, and Limp Home Mode

The **Faults** window, see Figure 6-30, allow for the selection of the Fault Timer duration in ms, which is set by the IFT bits. The **Reset Flt Pin** button clears the FPINRST bit and release the nFLT pin. The **Stdalone** box indicates that the STANDALONE bit is set and is in stand alone mode. The **V5AUV** box indicates that an under voltage fault has occurs at the V5A pin. The **TW** box indicates an overtemperature thermal warning fault has occurred. The **PC** box indicates that the PC (power cycle) bit is set, which happens at power up and is considered a fault. The PC bit must be cleared by reading the STATUS3 register and must be cleared before the channels can be enabled. There are several faults that if triggered must be read before operation can continue and they are covered in the **Faults** window.

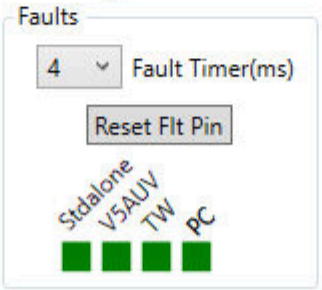


Figure 6-30. Fault Timer, Flags, and Resetting of Faults

Copyright © 2021 Texas Instruments Incorporated

6.6 Limp Home Mode Window

The TPS92520-Q1 enters the limp home mode of operation after detecting three consecutive watchdog timeout events or when the LHSW bit is set high in the SYSCFG1 register. The limp home mode is programmed by a variety of registers that sets the operational setpoint. By selecting the **Limp Home** button in the **Devices** Window it will open up the **Limp Home Mode** window. The main **Limp Home Mode** window now appears as shown in Figure 6-31. This window include three sub-windows (**Channel 1**, **Channel 2**, and **Device**). The channel windows have three slide bars that control **Analog Current**, **On Time** (switching frequency), and **PWM** (internal PWM duty cycle). This is setup similarly to the **Run Mode** windows and adjusts the LHxIADJ registers, the LHxTON registers, and the LHxPWM registers set-points. Similar to the Channel windows in the Run Mode it also has selection boxes for **Enable**, **PWM Source**, **PWM 100%**, **Low iLimit Resp**, **High iLimit Resp**, and **Therm Response**.

Device: The window shows a fault timer that is selectable in ms. A check box sets whether the limp home mode reference point is generated from the LHxIADJ registers for each channel or if the input voltage at the LHI pin sets the reference voltage for both channels. See the *Detailed Description* section of the *TPS92520-Q1 data sheet* for more detailed information. The **Limp Mode On** button sets the LHSW bit in the SYSCFG1 register. This allows to turn on the setting put into the limp home registers without having to go through the conditions that cause the device to go into limp home mode.

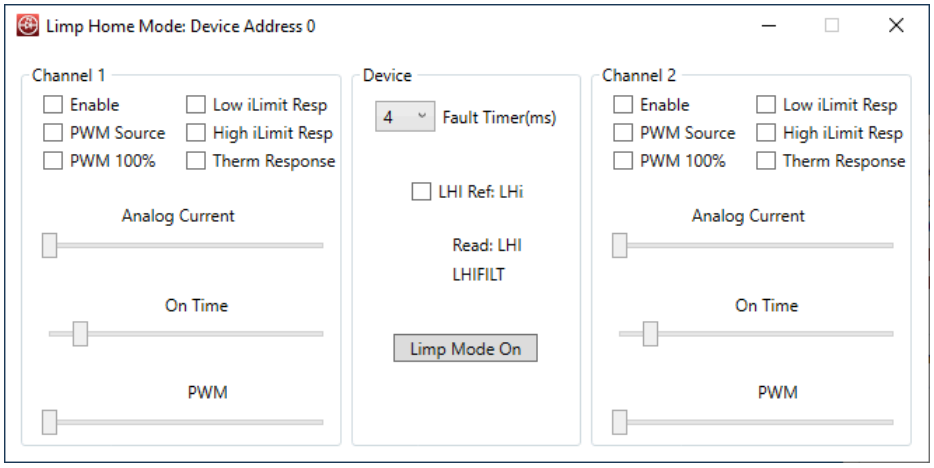


Figure 6-31. GUI, Limp Home Mode Window

An example limp home mode is as follows. The Channels are enabled using the enable box. The PWM source box is enabled and it sets the PWM duty cycle references to the slide bar for **PWM**, which is the internal PWM duty cycle control. The PWM duty cycle is set to 512 out of 1024 scale and is therefore a 50% duty cycle. The **On Time** slide bar is set to 7, which is the approximately 440-kHz switching frequency. **Analog Current** is set to

Copyright © 2021 Texas Instruments Incorporated

300, which sets the board to output to approximately 519 mA. The **Fault Timer** is set to 4 ms. The LHI **Ref: LHi** box is not selected; therefore the reference for limp home is internal.

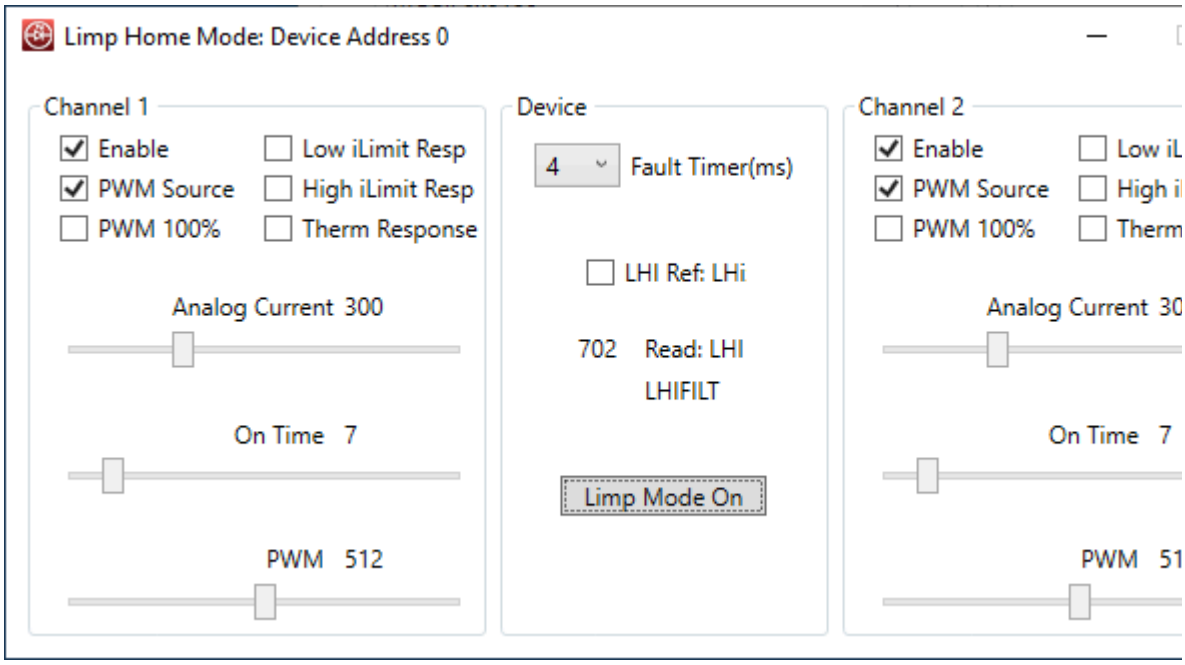


Figure 6-32. Example Limp Home Mode Settings

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (September 2021)	Page
• Updated Table 1-1 and Table 1-2	6
• Updated Table 2-1	9
• Added information to clarify how to use EVM at input voltages less than 40 V	33

Copyright © 2021 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated