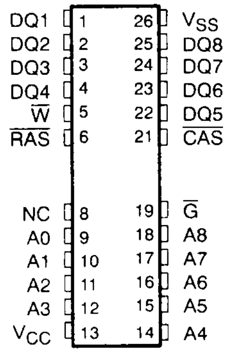
- **131 072 × 8 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MAX)
'48C128/C138-70	70 ns	25 ns	40 ns	130 ns
'48C128/C138-80	80 ns	25 ns	40 ns	150 ns
'48C128/C138-10	100 ns	30 ns	45 ns	180 ns

- **TMS48C128 — Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **TMS48C138 — Write-Per-Bit Operation**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 24/26-lead 300-Mil-Wide Surface Mount (SOJ) Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

DJ Package†
(Top View)



†The package is shown for pinout reference only.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
$\overline{G}$	Data-Output Enable
NC	No Connect
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS48C128 and the TMS48C138 series are high-speed, 1 048 576-bit dynamic random-access memories organized as 131 072 words of eight bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 413 mW operating and 11 mW standby on 80 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a − 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS48C128 and TMS48C138 are offered in a 300-mil 24/26-lead plastic surface mount SOJ (DJ suffix) package. This package is characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 256 columns specified by column addresses A0 through A7 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS48C128 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{CAA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CAP} (access time from rising edge of $\overline{CAS}$).

write-per-bit operation (TMS48C138)

The $\overline{W}$ pin selects the write-per-bit option. The TMS48C138 is equipped with two modes of write operations. If $\overline{W}$ is held low on the falling edge of $\overline{RAS}$ (during a random access operation), the write-per-bit mode is enabled. When $\overline{RAS}$ has latched the write-per-bit mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the latter of $\overline{CAS}$ or $\overline{W}$ (for early write operation, $\overline{W}$ can remain low for the entire $\overline{RAS}$ low period). If a 0 is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will be inhibited and data will not be written from that I/O. If a 1 is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, then the write circuits for that particular I/O will not be inhibited and data will be written from that I/O.

Important: The write-per-bit operation is selected only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, the write-per-bit function is not enabled and the write operation is identical to a standard ×4 or ×8 DRAM, with all I/Os being written by the data appearing on the DQ pins when the latter of $\overline{W}$ or $\overline{CAS}$ is brought low.

Table 1. State When $\overline{RAS}$ Falls

$\overline{W}$	DQ1-DQ8	MODE
1	X	Write enable at DQ1-DQ8
0	1	Write to DQ enabled
0	0	Write to DQ disabled

address (A0 through A8)

Seventeen address bits are required to decode 131 072 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched on to the chip by the row-address strobe ($\overline{RAS}$). Then eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the first column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1-DQ8)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{CAA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

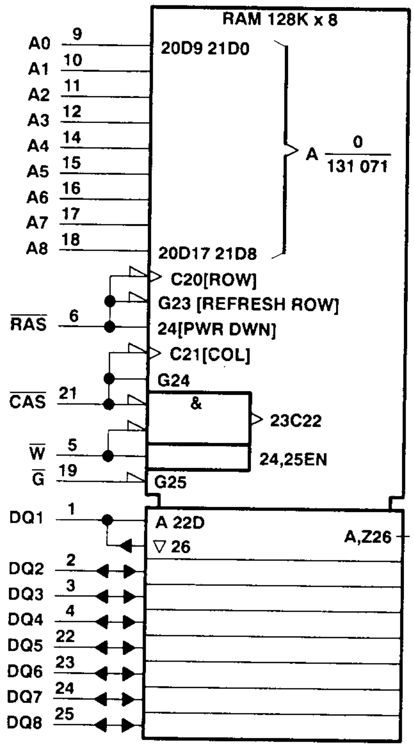
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power-up

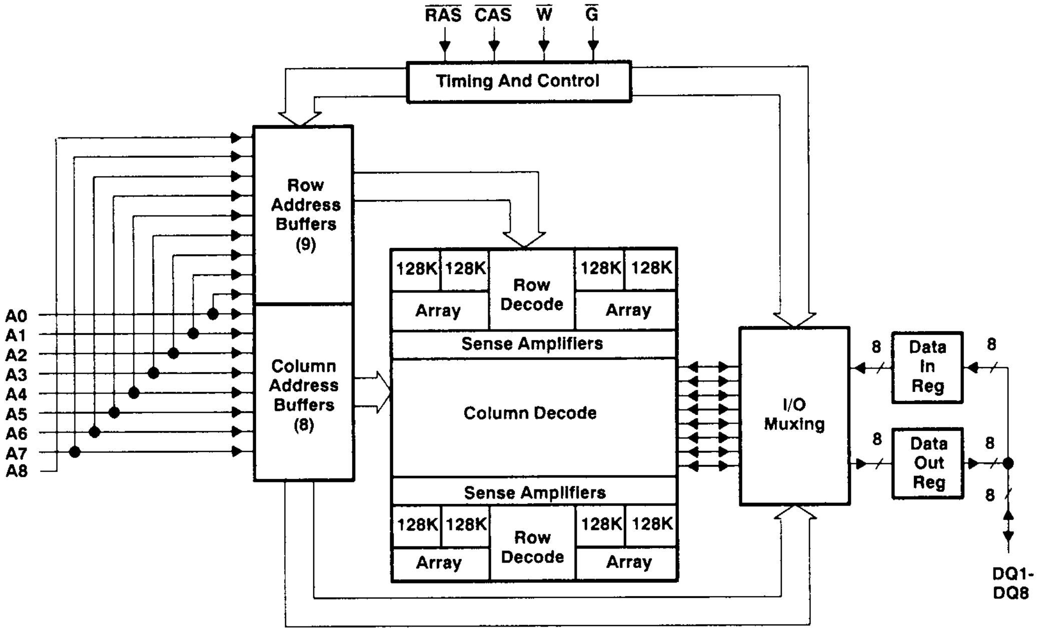
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1)	– 1 V to 7 V
Voltage range on V_{CC}	– 1 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1†		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

† Characterized at 5.5 V V_{CC}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	$V_I = 0$ to 5.8 V, $V_{CC} = 5$ V, All other pins = 0 to V_{CC}		± 10		± 10		± 10	μA
I_O	Output current (leakage)	$V_O = 0$ to V_{CC}, $V_{CC} = 5.5$ V, $\overline{CAS}$ high		± 10		± 10		± 10	μA
I_{CC1}	Read/write cycle current	t_{RWC} = minimum, $V_{CC} = 5.5$ V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = 2.4$ V		2		2		2	mA
I_{CC3}	Average refresh circuit ($\overline{RAS}$-only or CBR)	t_{RWC} = minimum, $V_{CC} = 5.5$ V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		75		65	mA
I_{CC4}	Average page current	t_{PC} = minimum, $V_{CC} = 5.5$ V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		60		50		45	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
$C_{i(G)}$	Input capacitance, output-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		25		25		30	ns
t_{CAA}	Access time from column address		40		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{GAC}	Access time from $\overline{G}$ low		25		25		30	ns
t_{CAP}	Access time from column precharge		45		45		50	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	20	0	20	0	25	ns
t_{GOFF}	Output disable time after $\overline{G}$ high (see Note 4)	0	20	0	20	0	25	ns

NOTE 4: t_{OFF} and t_{GOFF} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	130		150		180		ns
t_{WC}	Write cycle time	130		150		180		ns
t_{RWC}	Read-write/read-modify-write cycle time	185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	50		50		55		ns
t_{PCM}	Page-mode read-modify-write cycle time	105		105		120		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 8)	25	10 000	25	10 000	30	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	100	10 000	ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	100	100 000	ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		20		25		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		12		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		10		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 11)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	55		60		70		ns

Continued next page.

NOTES:
5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5) (concluded)

		'48C128-70 '48C138-70		'48C128-80 '48C138-80		'48C128-10 '48C138-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{GH}	$\overline{G}$ command hold time	20		20		25		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		25		30		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	55		55		65		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	22	55	25	70	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	17	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	40		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	40		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	100		110		135		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	70		70		80		ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to DQ in low-Z	0		0		0		ns
t_{GDD}	Delay time, $\overline{G}$ high before data at DQ	20		20		25		ns
t_{GSR}	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	25		25		30		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	15		20		25		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	0		0		0		ns
t_{WBS}	Write-per-bit setup time	0		0		0		ns
t_{WBH}	Write-per-bit hold time	10		10		10		ns
t_{WDS}	Write-per-bit selection setup time	0		0		0		ns
t_{WDH}	Write-per-bit selection hold time	10		10		10		ns
t_{REF}	Refresh time interval		8		8		8	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
14. Read-modify-write operation only.
15. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

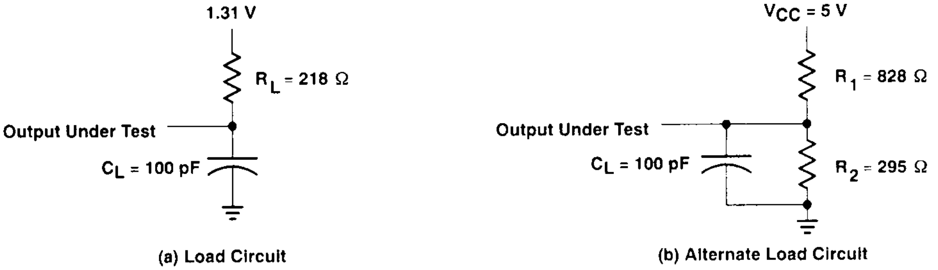
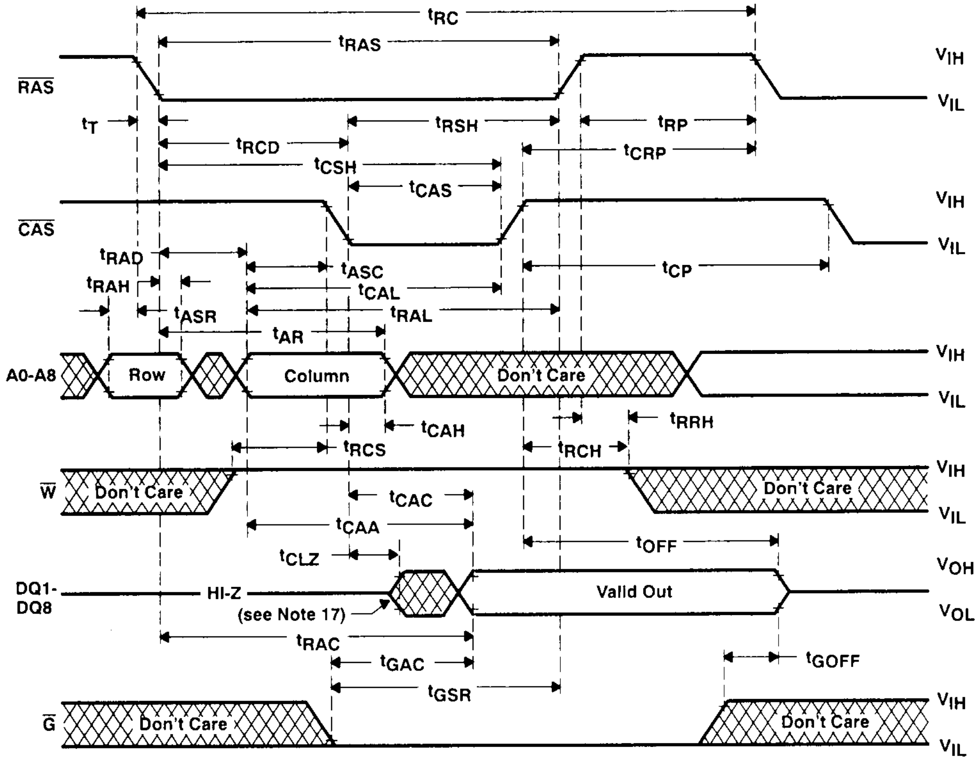


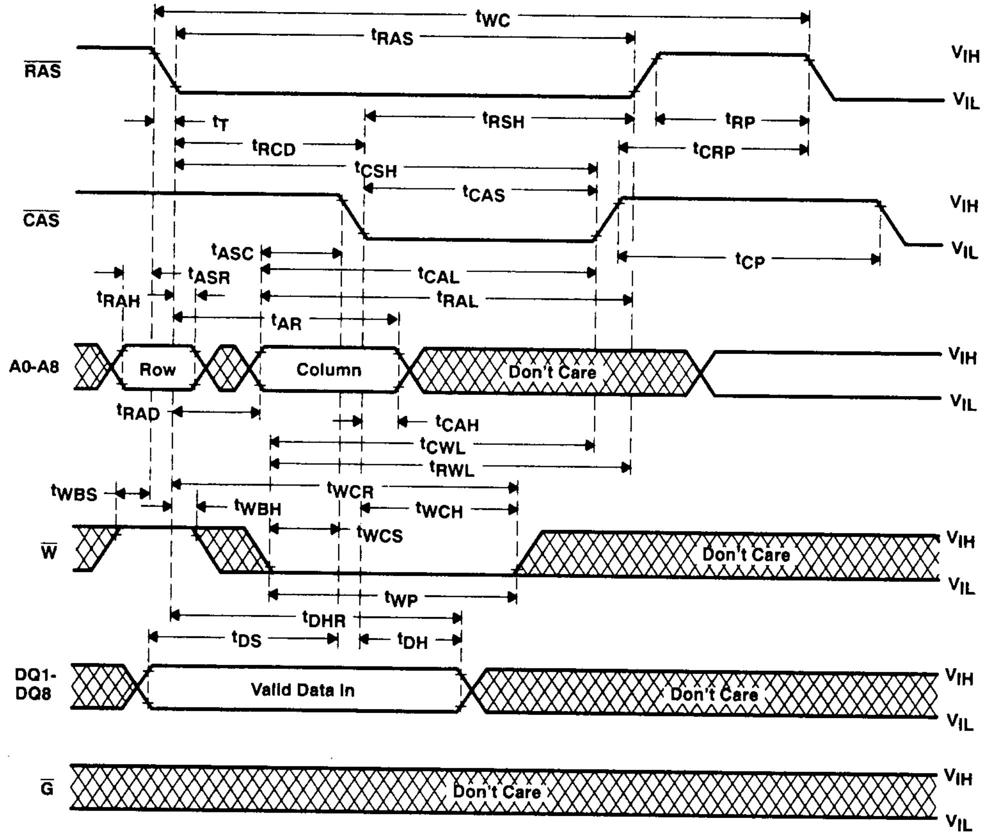
Figure 1. Load Circuits For Timing Parameters

read cycle timing



NOTE 17: Output may go from high impedance to an invalid data state prior to the specified access time.

early write cycle timing



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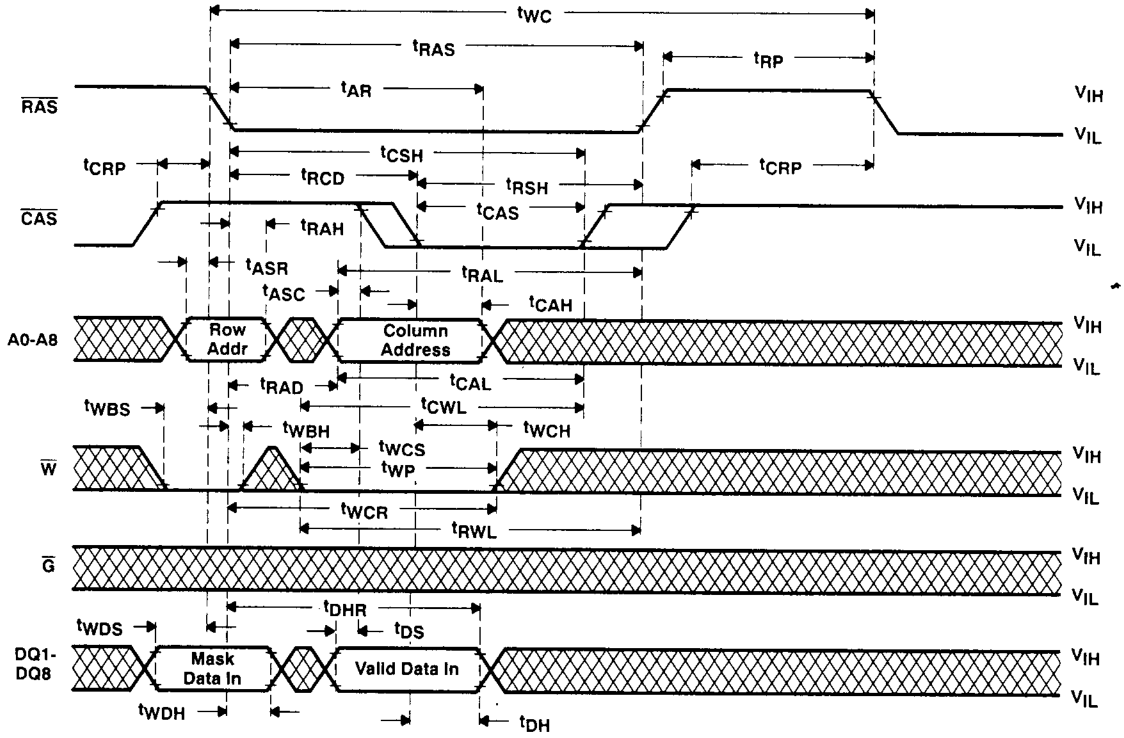
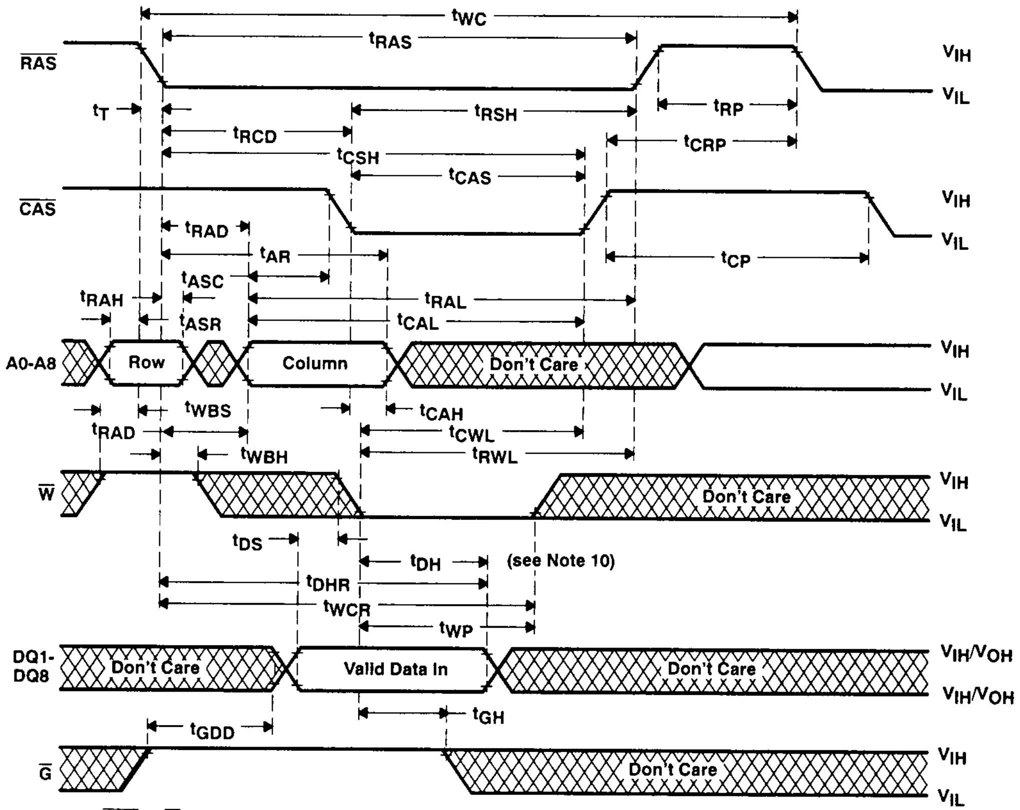
early write cycle (write-per-bit selected)

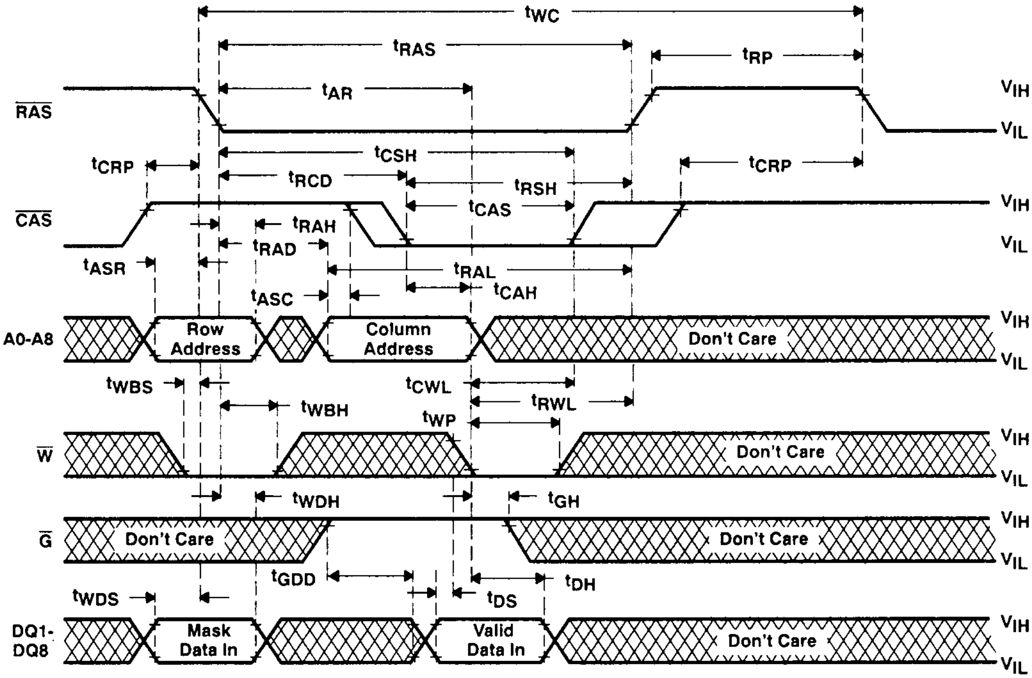


write cycle timing

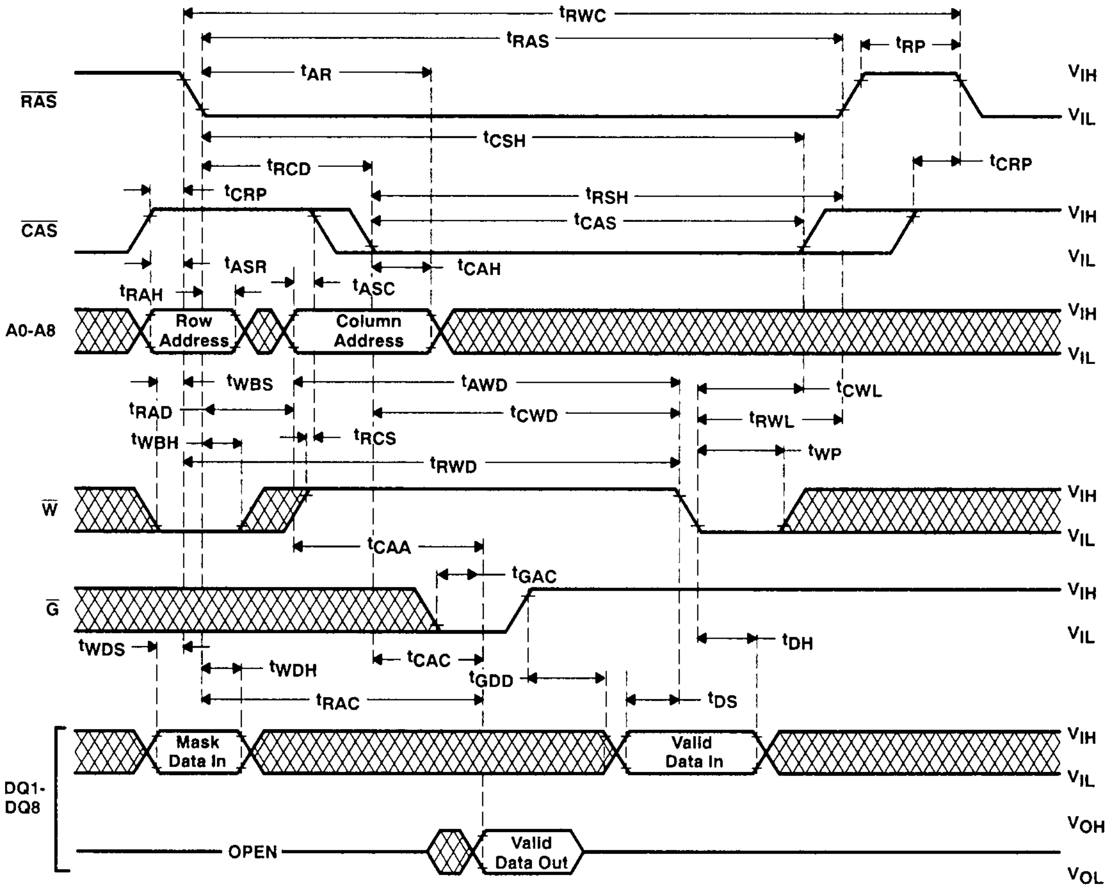


NOTE 10: Later of $\overline{CAS}$ or $\overline{W}$ in write operation.

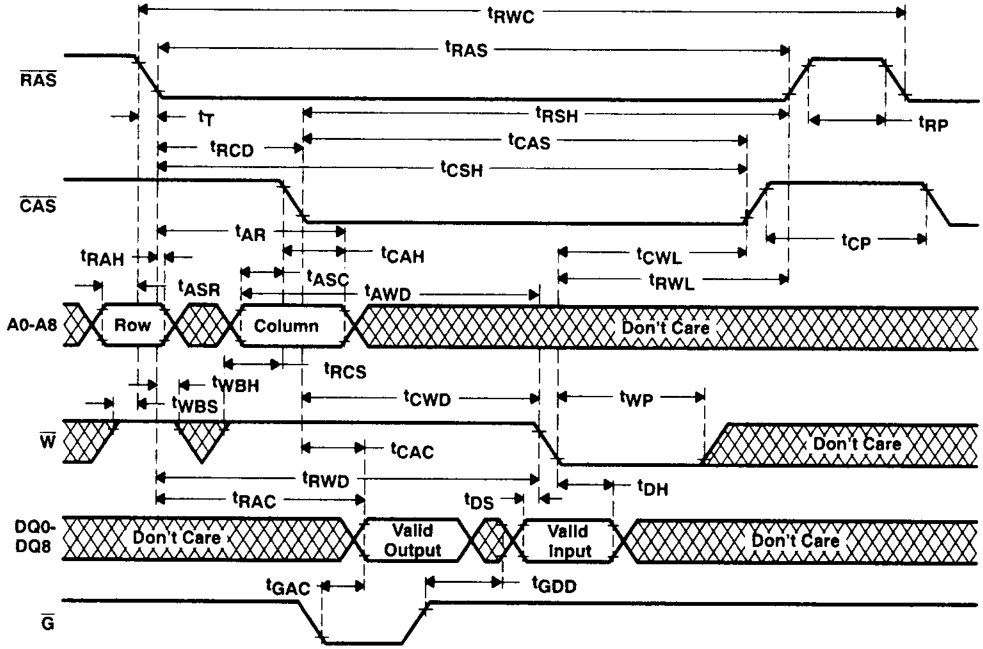
write cycle (write-per-bit selected)



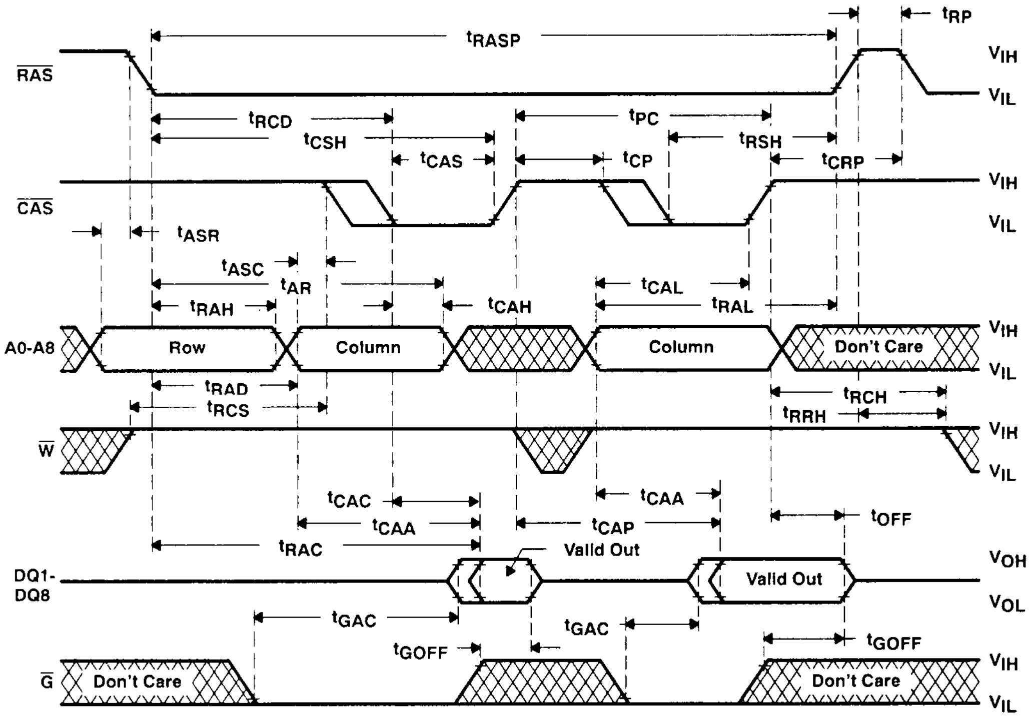
read-modify-write cycle (write-per-bit selected)



read-modify-write cycle timing

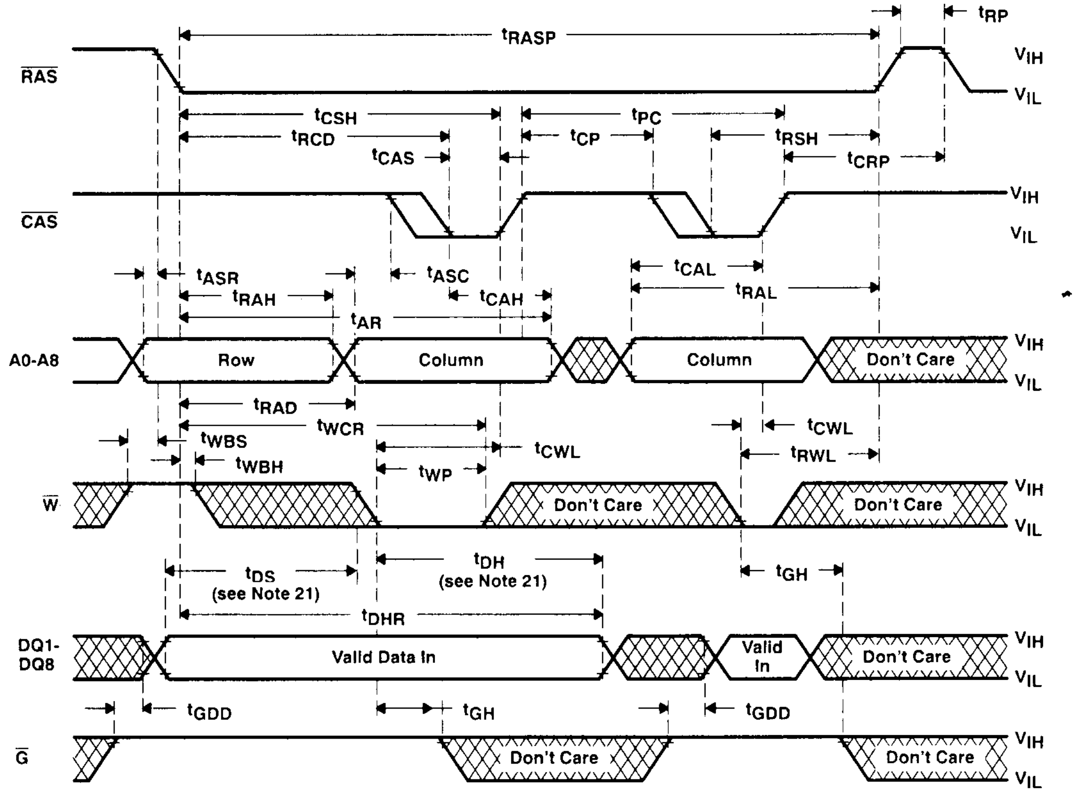


enhanced page-mode read cycle timing



NOTES: 17. Output may go from high impedance to an invalid data state prior to the specified access time.
18. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
19. Access time is t_{CAP} or t_{CAA} dependent.

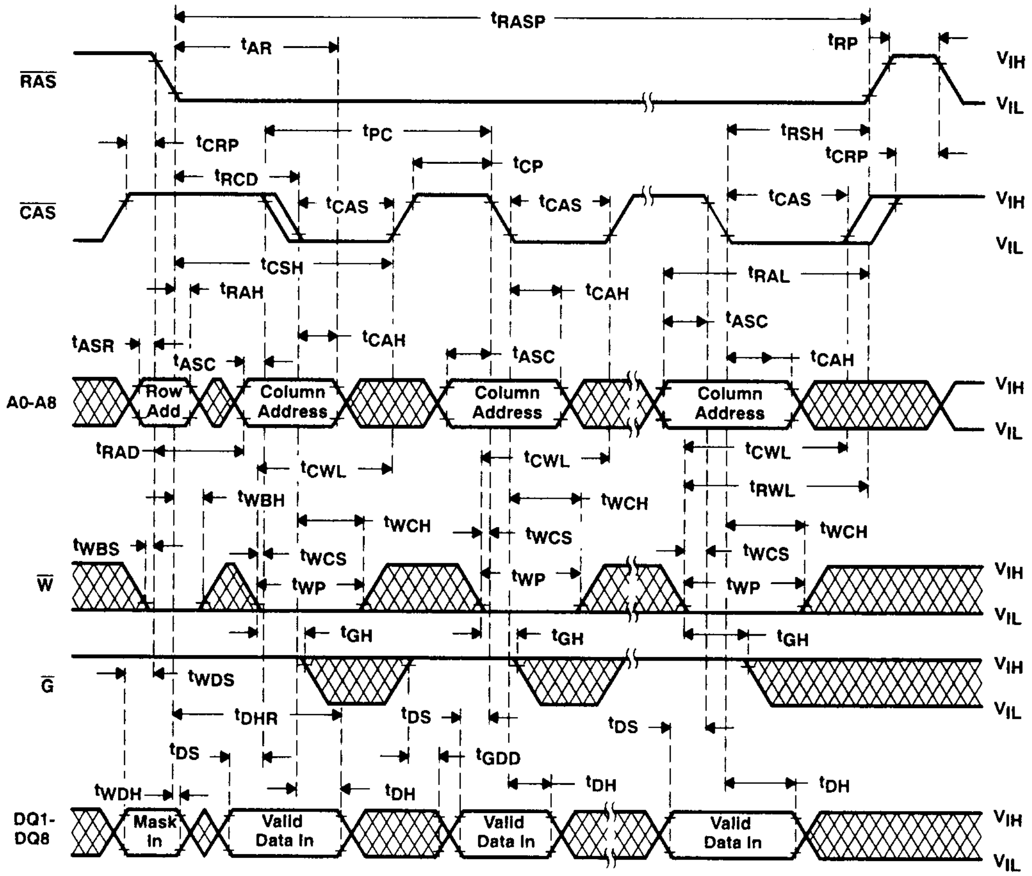
enhanced page-mode write cycle timing



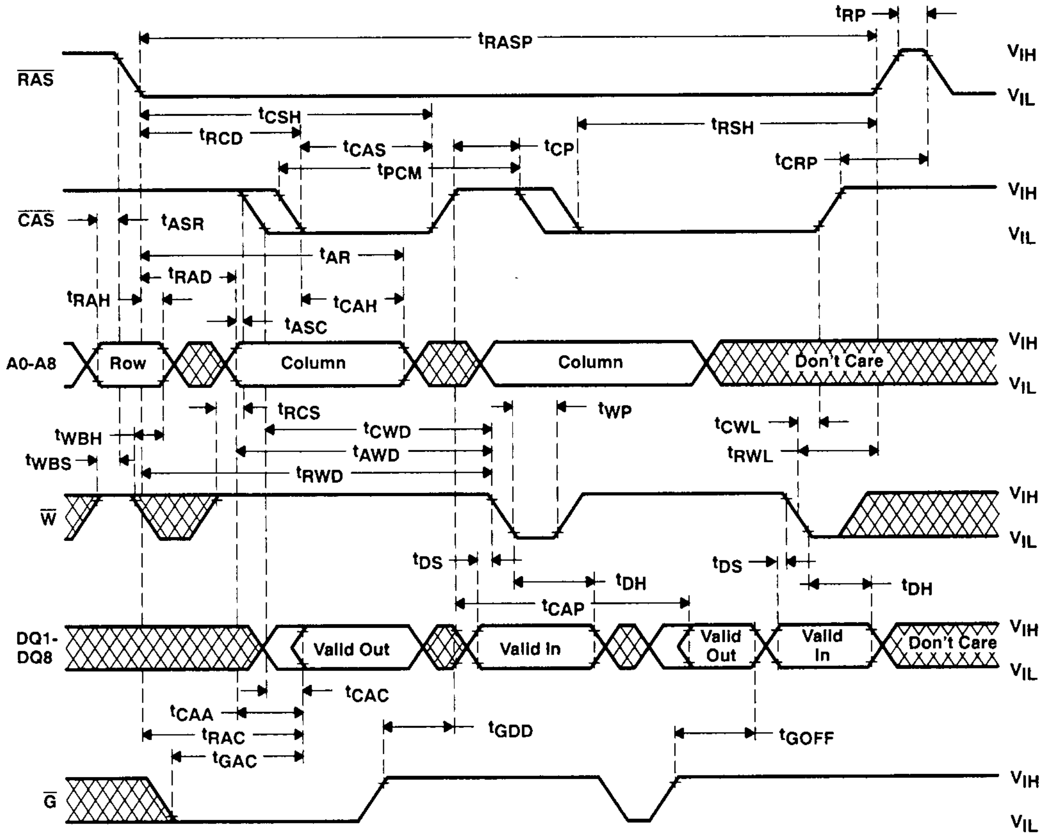
NOTES: 20. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

21. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode write cycle (write-per-bit selected)



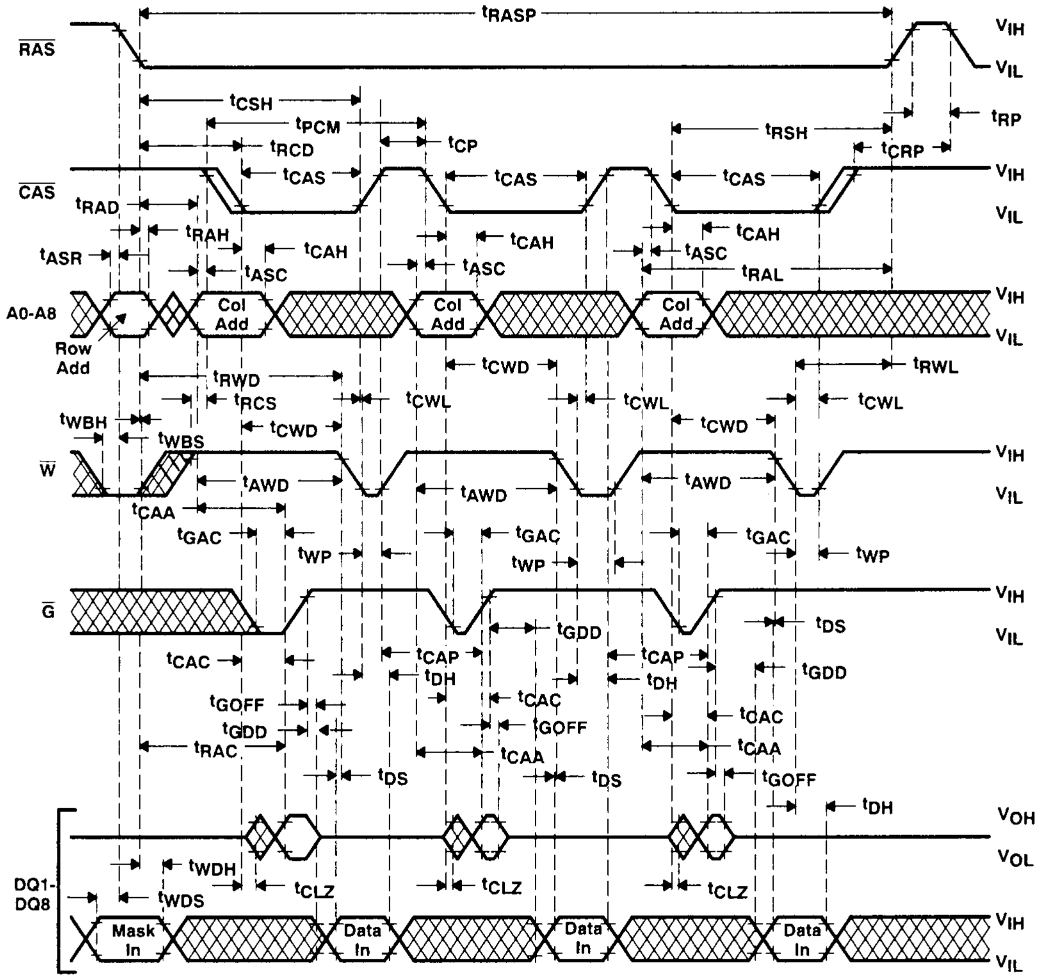
enhanced page-mode read-modify-write cycle timing



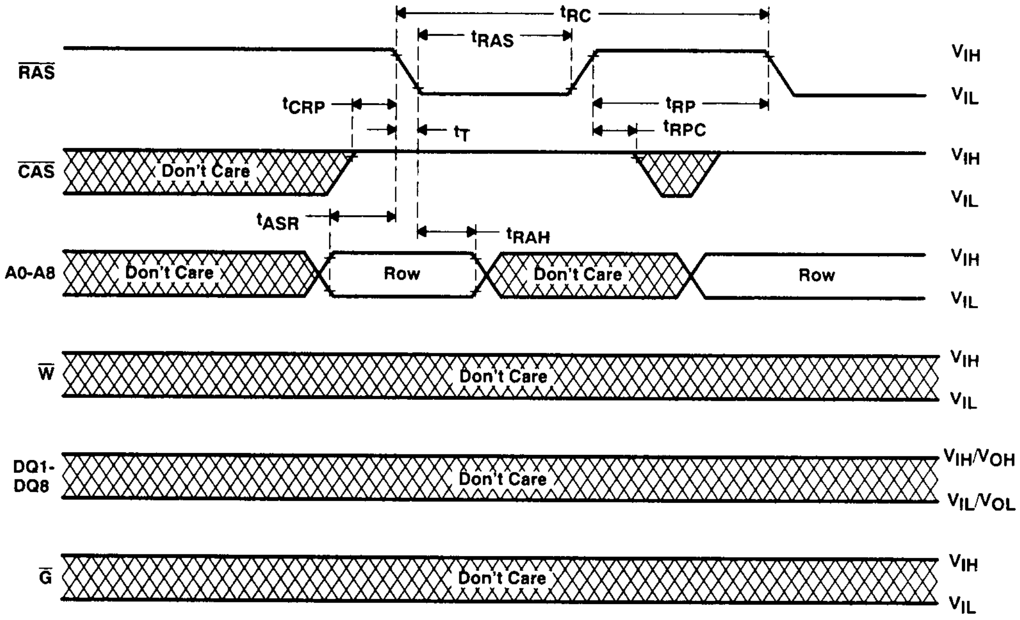
NOTES: 17. Output may go from high impedance to an invalid data state prior to the specified access time.

22. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

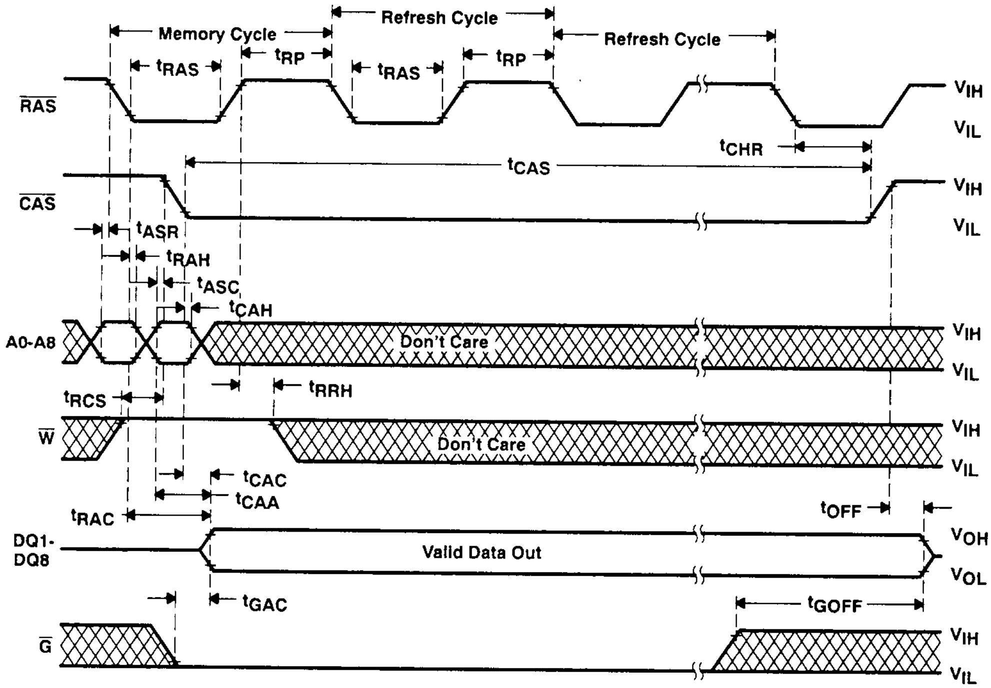
enhanced page-mode read-modify-write cycle (write-per-bit selected)



$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle



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automatic (CAS-before-RAS) refresh cycle timing