

CLC401

Fast Settling, Wideband High Gain Monolithic Op Amp

General Description

The CLC401 is a wideband, fast settling op amp designed for applications requiring gains greater than ± 7 . Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high speed monolithic op amps. For example, at a gain of +20, the -3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2° deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high frequency amplification-requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ± 7 to ± 50 gain range precludes the need for external compensation. And, unlike many other high speed-op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is based on **National's** proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in *Figure 1* and *Figure 2*). However, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-89973

Space level versions also available.

For more information, visit <http://www.national.com/mil>

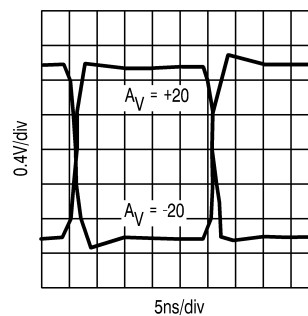
Features

- -3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- Low power, 150mW
- Overload and short circuit protected
- Stable without compensation
- Recommended gain range, ± 7 to ± 50

Applications

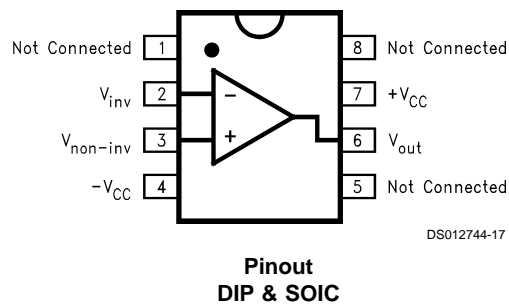
- Flash, precision A/D conversion
- Photodiode, CCD preamps
- IF processors
- High speed modems, radios
- Line drivers
- DC coupled log amplifiers
- High speed communications

Pulse Response



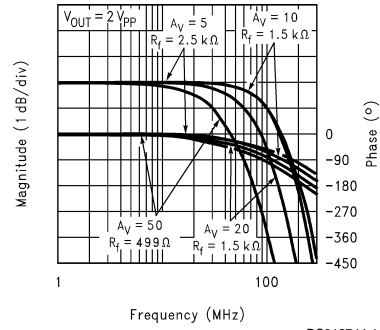
DS012744-18

Connection Diagram



DS012744-17

Connection Diagram (Continued)



Non-Inverting Frequency Response

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	-40°C to +85°C	CLC401AJP	CLC401AJP	N08E
8-pin plastic SOIC	-40°C to +85°C	CLC401AJE	CLC401AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $\pm 7V$

I_{OUT}
Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...

60mA

Common Mode Input Voltage $\pm V_{CC}$

Differential Input Voltage 5V

Junction Temperature Range +150°C

Operating Temperature Range -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Lead Solder Duration (+300°C) 10 sec

Operating Ratings

Thermal Resistance

Package (θ_{JC}) (θ_{JA})

MDIP 70°C/W 125°C/W

SOIC 65°C/W 145°C/W

Electrical Characteristics

($A_V = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 1.5k\Omega$; unless specified).

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature		CLC401AJ	+25°C	-40°C	+25°C	+85°C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	$V_{OUT} < 2V_{PP}$	150	>100	>100	>70	MHz
LSBW		$V_{OUTt} < 5V_{PP}$	100	>65	>65	>55	MHz
	Gain Flatness	$V_{OUT} < 2V_{PP}$					
GFPL	Peaking	<25MHz	0	<0.1	<0.1	<0.1	dB
GFPH	Peaking	>25MHz	0	<0.2	<0.2	<0.2	dB
GFR	Rolloff	<50MHz	0.2	<1.0	<1.0	<1.3	dB
LPD	Linear Phase Deviation	DC to 50MHz	0.2	<1.0	<1.0	<1.5	deg
Time Domain Response							
TRS	Rise and Fall Time	2V Step	2.5	<3.5	<3.5	<5.0	ns
TRL		5V Step	5	<7.0	<7.0	<8.0	ns
TS	Settling Time to $\pm 0.1\%$	2V Step	10	<15	<15	<15	ns
OS	Overshoot	2V Step	0	<10	<10	<10	%
SR	Slew Rate		1200	>800	>800	>700	V/ μ s
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz	-45	<-35	<-35	<-35	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz	-60	<-50	<-50	<-45	dBc
	Equivalent Input Noise						
SNF	Noise Floor	>1MHz	-158	<-155	<-155	<-154	dBm (1Hz)
INV	Integrated Noise	1MHz to 150MHz	35	<50	<50	<55	μ V
Static, DC Performance							
VIO	Input Offset Voltage (Note 3)		3	± 10.0	± 6.0	± 11.0	mV
DVIO	Average Temperature Coefficient		20	± 50	-	± 50	μ V/°C
IBN	Input Bias Current (Note 3)	Non-Inverting	10	± 36	± 20	± 20	μ A
DIBN	Average Temperature Coefficient		100	± 200	-	± 100	nA/°C
IBI	Input Bias Current (Note 3)	Inverting	10	46	30	40	μ A
DIBI	Average Temperature Coefficient		100	± 200	-	± 100	nA/°C
PSRR	Power Supply Rejection Ratio		55	50	50	50	dB
CMRR	Common Mode Rejection Ratio		55	50	50	50	dB
ICC	Supply Current (Note 3)	No Load	15	21	21	21	mA
Miscellaneous Performance							
RIN	Non-Inverting Input	Resistance	200	>50	>100	>100	k Ω
CIN		Capacitance	0.5	<2.5	<2.5	<2.5	pF
RO	Output Impedance	at DC	0.2	<0.3	<0.3	<0.3	Ω
VO	Output Voltage Range	No Load	3.5	>3.0	>3.2	>3.2	V

Electrical Characteristics (Continued)

($A_V = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 1.5k\Omega$; unless specified).

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Miscellaneous Performance							
CMIR	Common Mode Input Range	For Rated Performance	2.8	>2.0	>2.5	>2.5	V
IO	Output Current		60	>35	>50	>50	mA

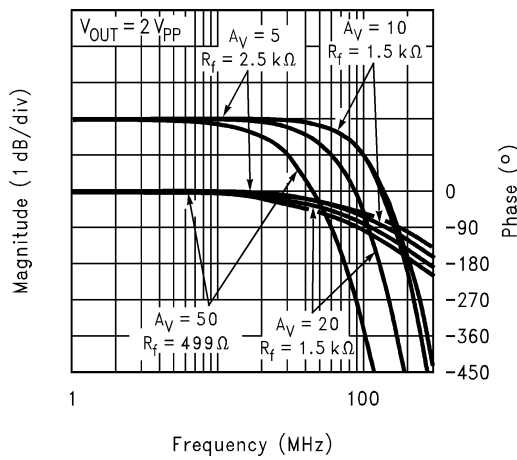
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25°C.

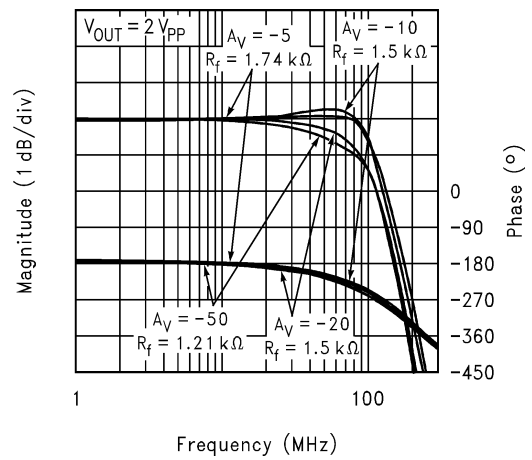
Typical Performance Characteristics ($T_A = 25^\circ$, $A_V = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$; Unless Specified).

Non-Inverting Frequency Response



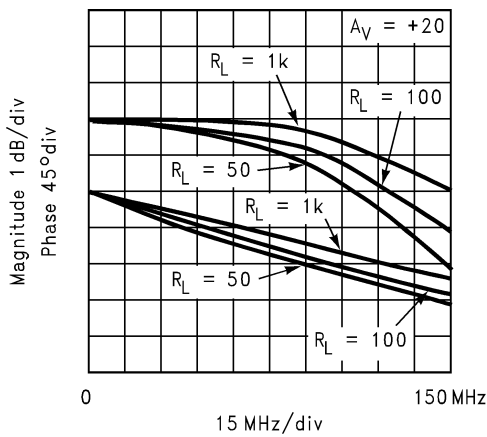
DS012744-1

Inverting Frequency Response



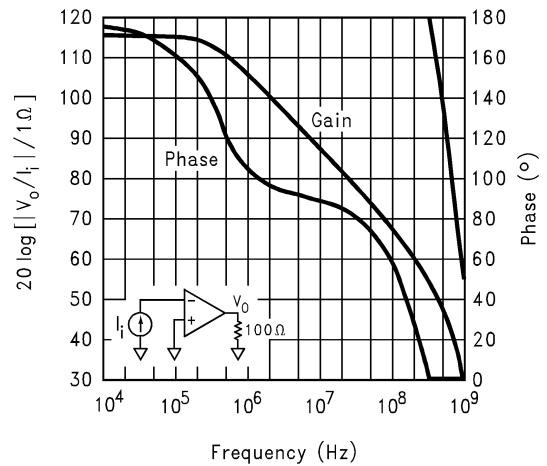
DS012744-2

Frequency Response for Various R_L s



DS012744-3

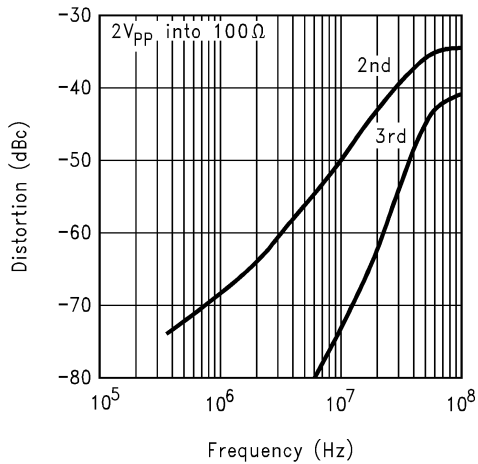
Open-Loop Transimpedance Gain, $Z(s)$



DS012744-4

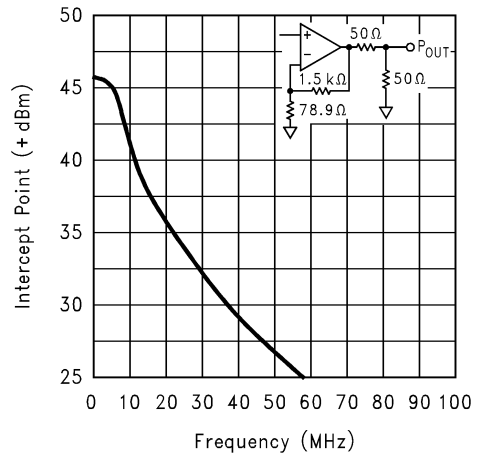
Typical Performance Characteristics ($T_A = 25^\circ$, $A_V = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$: Unless Specified).. (Continued)

2nd and 3rd Harmonic Distortion



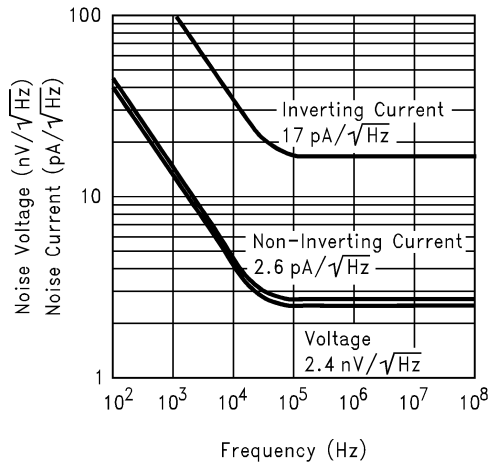
DS012744-5

2-Tone,3rd Order, Intermodulation Intercept



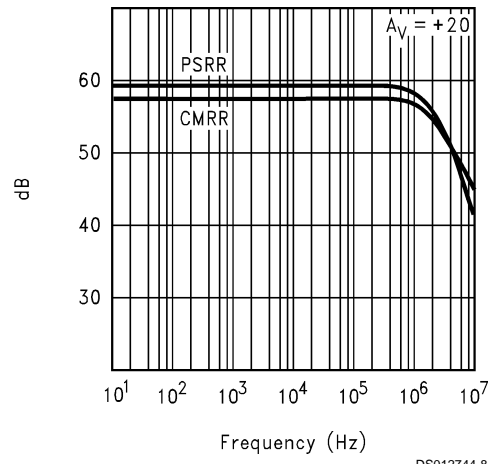
DS012744-6

Equivalent Input Noise



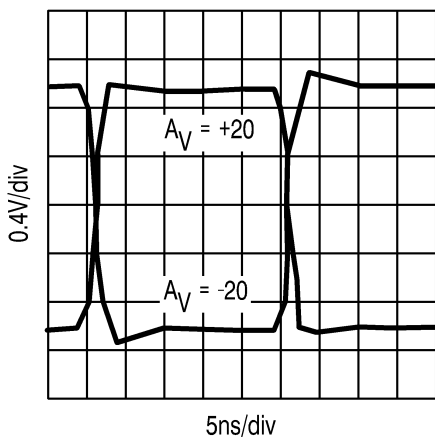
DS012744-7

CMRR and PSRR



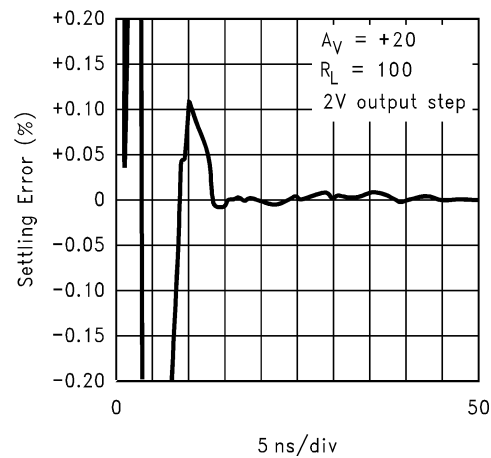
DS012744-8

Pulse Response



DS012744-18

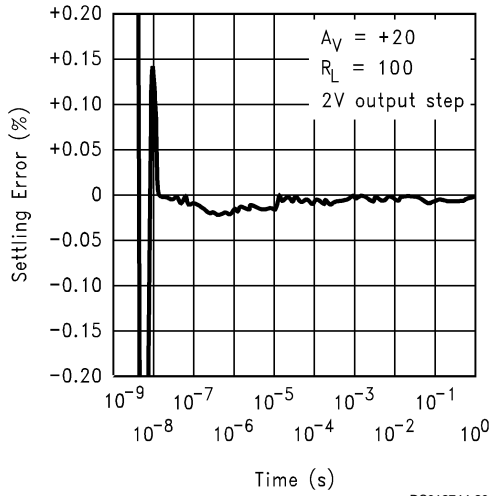
Setting Time



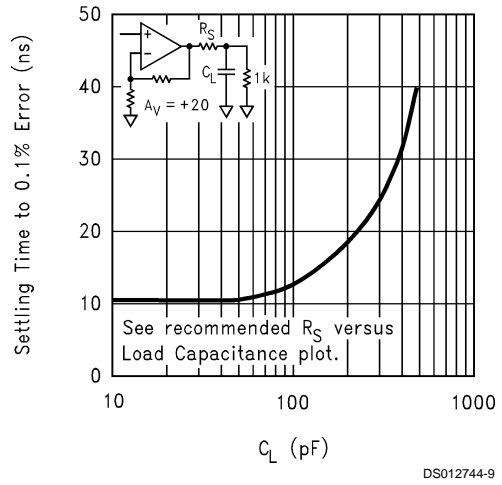
DS012744-19

Typical Performance Characteristics ($T_A = 25^\circ$, $A_V = +20$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$: Unless Specified).. (Continued)

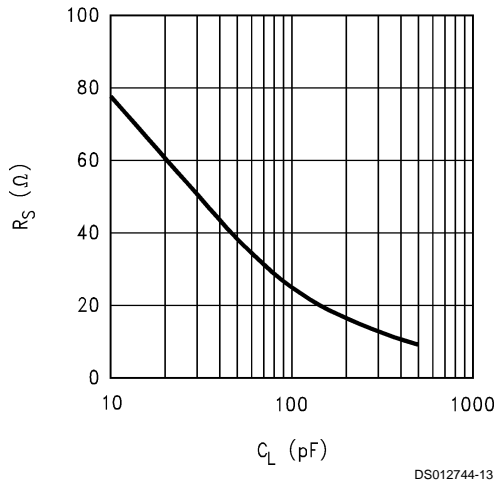
Long-Term Settling Time



Settling Time vs. Load Capacitance



Recommended R_S vs. Load Capacitance

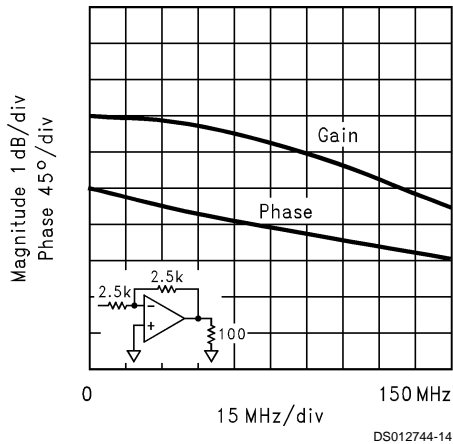


Low Gain & Transimpedance Applications

The CLC401 may be used at gains down to unity ($A_V = \pm 1$) by choosing R_f according to Equation (4) in this datasheet. The curves to the right show performance at inverting unity gain with $R_f = 2500\Omega$, a configuration appropriate for D/A converter buffering and other transimpedance applications.

DS012744-21

Frequency Response, $A_V = -1$, $R_f = 2.25k\Omega$



Application Division

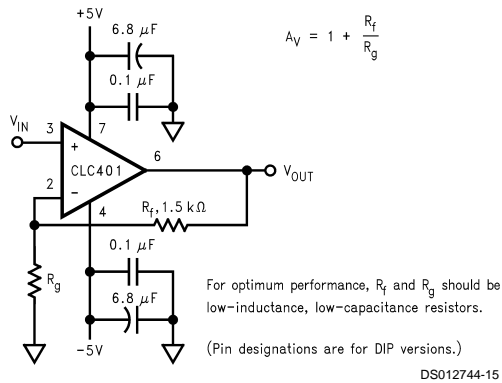


FIGURE 1. Recommended Non-Inverting Gain Circuit

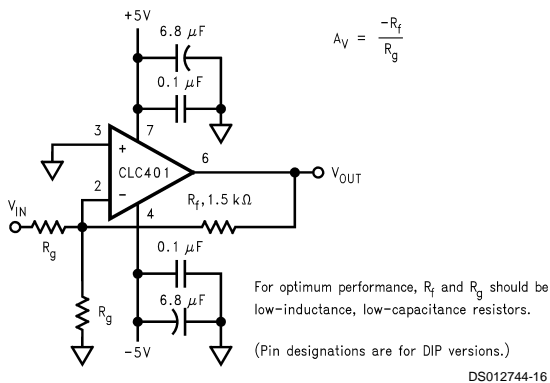


FIGURE 2. Recommended Inverting Gain Circuit

Understanding the Loop Gain

Referring to the equivalent circuit of *Figure 3*, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plots on page 3. This $Z(s)$ is analogous to the open-loop gain of a voltage feedback amplifier.

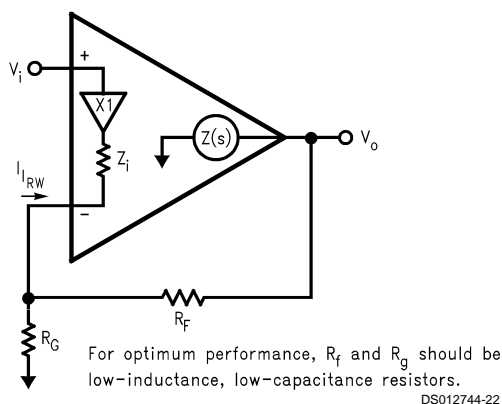


FIGURE 3. Current feedback topology

Developing the non-inverting frequency response for the topology of *Figure 3* yields:

Equation 1

$$\frac{V_O}{V_I} = \frac{1 + R_f / R_g}{1 - 1 / LG}$$

where LG is the loop gain defined by,

Equation 2

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f \parallel R_g)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression. For an idealized treatment, set $Z_i=0$ which results in a very simple $LG = Z(s)/R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1). Using the $Z(s)$ (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 1.5k\Omega$, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to $(1+R_f/R_g)$.

At higher frequencies, the roll-off of $Z(s)$ determines the closed-loop frequency response which, ideally, is dependent only on R_f . **The specifications reported on the previous pages are therefore valid only for the specified $R = 1.5k\Omega$.** Increasing R from $1.5k\Omega$ will decrease the loop gain and band width, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g .

The CLC401 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC401, $Z = 50\Omega$ leading to drop in loop gain and bandwidth at high gain settings, as given by Equation 2. The second term in Equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \parallel R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC401 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

Equation 3

$$\text{Output Offset } V_O = \pm IBN \times R_S (1 + R_f/R_g) \pm V_{IO} (1 + R_f/R_g) \pm IBI \times R_f$$

An important observation is that for fixed R_f , offsets as referred to the input improve as the gain is increased (divide all terms by $1+R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

Application Division (Continued)

The CLC400 is intended for gains of ± 1 to ± 8 while the CLC401 is designed for gains of ± 7 to ± 50 . Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5Ω with the CLC401- this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 1.5k\Omega$ and $R_g = 79\Omega$). For the CLC401 this gives,

Equation 4

$$R_f = 2500 - 50A_V \text{ and } R_g = \frac{2500 - 50A}{A_V - 1}$$

where A_V is the desired non-inverting gain. Note that with $A_V = +20$ we get the specified $R_f = 1.5k\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC401 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC401.

Printed Circuit Layout

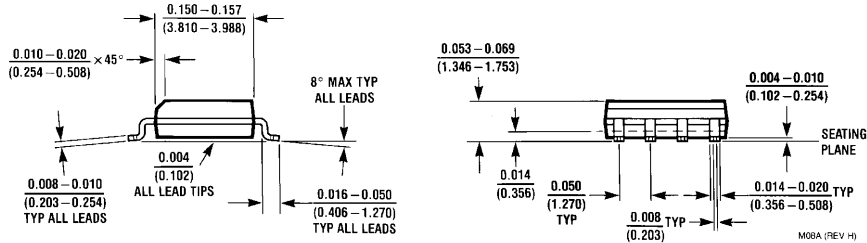
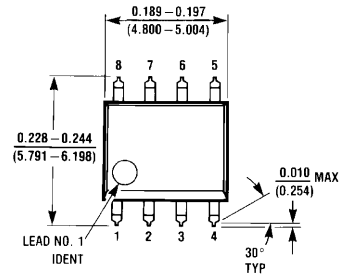
As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

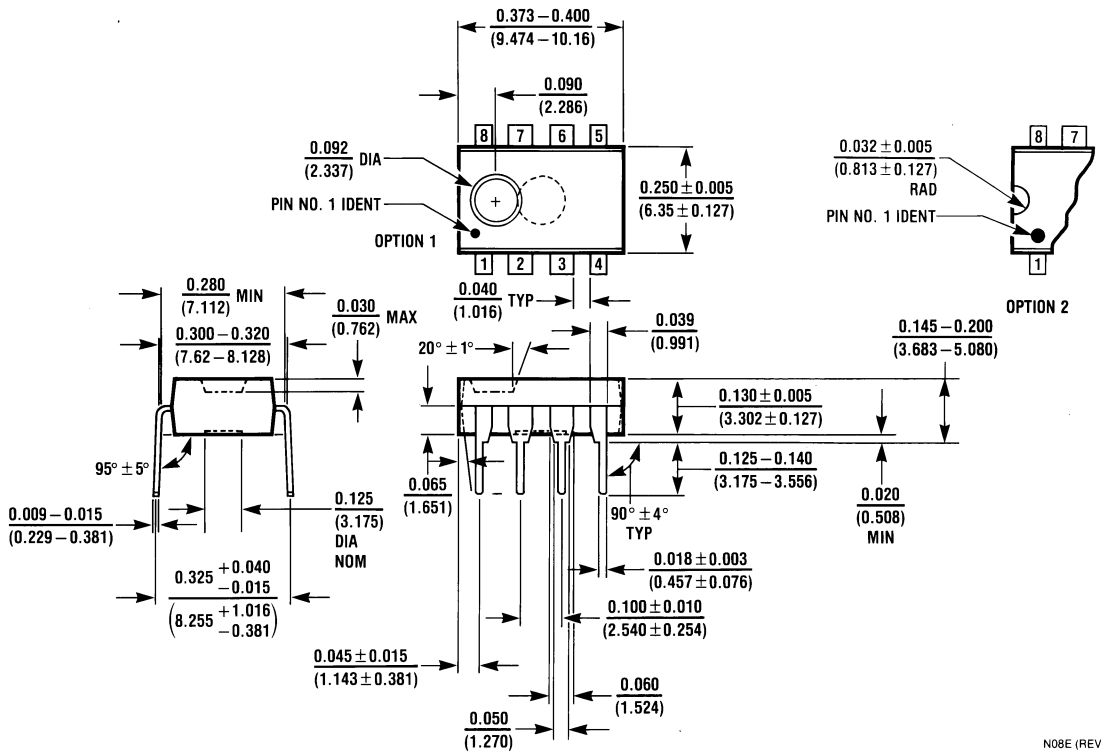
Precision buffered resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with the slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. CLC730013 for through-hole and CLC730027 for SOIC) for the CLC401 are available.

Physical Dimensions inches (millimeters) unless otherwise noted



NS Product Number M08A



NS Product Number N08E

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National Semiconductor Corporation
Home[Products](#) > [Analog - Amplifiers](#) > [Operational Amplifiers](#) > [High Speed > 50MHz](#) > CLC401

Product Folder

CLC401

 Fast Settling, Wideband High Gain Monolithic Op Amp

Contents

- [General Description](#)
- [Features](#)
- [Applications](#)
- [Datasheet](#)
- [Package Availability, Models, Samples & Pricing](#)
- [Design Tools](#)
- [Application Notes](#)

Parametric Table

Channels (Channels)	1
Input Output Type	Not Rail to Rail
Bandwidth, typ (MHz)	179
Slew Rate, typ (Volts/usec)	1200
Supply Current per Channel, typ (mA)	15
Minimum Supply Voltage (Volt)	10
Maximum Supply Voltage (Volt)	14
Offset Voltage, Max (mV)	6
Input Bias Current, Temp Max (nA)	36000
Output Current, typ (mA)	70
Voltage Noise, typ (nV/Hz)	2.40
Shut down	No
Feedback Type	Current
BW at Av+5 (MHz)	179
BW at Av+10 (MHz)	167
BW at Av+20 (MHz)	150
HD 2nd, typ (dB)	-45
HD 3rd, typ (dB)	-60
Settling Time	10nS to 0.1%
Special Features	AvCl>7

General Description

The CLC401 is a wideband, fast settling op amp designed for applications requiring gains greater than ± 7 . Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high speed monolithic op amps. For example, at a gain of +20, the -3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2° deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high frequency amplification-requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ± 7 to ± 50 gain range precludes the need for external compensation. And, unlike many other high speed-op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is based on **National's** proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in and). However, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-89973

Space level versions also available.

For more information, visit <http://www.national.com/mil>

Features

- -3dB bandwidth of 150MHz
 - 0.1% settling in 10ns
 - Low power, 150mW
 - Overload and short circuit protected
 - Stable without compensation
 - Recommended gain range, ± 7 to ± 50
-

Applications

- Flash, precision A/D conversion
 - Photodiode, CCD preamps
 - IF processors
 - High speed modems, radios
 - Line drivers
 - DC coupled log amplifiers
 - High speed communications
-

Datasheet

Title	Size (in Kbytes)	Date	<input type="checkbox"/> View Online	<input type="checkbox"/> Download	<input type="checkbox"/> Receive via Email
CLC401 Fast Settling, Wideband High Gain Monolithic Op Amp	279 Kbytes	14-Nov-00	View Online	Download	Receive via Email
CLC401 Fast Settling, Wideband High Gain Monolithic Op Amp (JAPANESE)	339 Kbytes		<input type="checkbox"/> View Online	<input type="checkbox"/> Download	<input type="checkbox"/> Receive via Email
CLC401 Mil-Aero Datasheet MNCLC401A-X	59 Kbytes		View Online	Download	Receive via Email

Please use [Adobe Acrobat](#) to view PDF file(s).

If you have trouble printing, see [Printing Problems](#).

Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	# pins		SPICE	IBIS		Quantity	\$US each		
CLC401AJE	SOIC NARROW	8	Full production	clc401.cir	N/A	<input type="checkbox"/> Samples <input type="checkbox"/> Buy Now	1K+	\$3.6500	tube of 95	[logo]ç2çT CLC40 1AJE
CLC401AJE-TR13	SOIC NARROW	8	Full production	clc401.cir	N/A	<input type="checkbox"/> Buy Now	1K+	\$3.6800	reel of 2500	[logo]ç2çT CLC40 1AJE
CLC401AJP	MDIP	8	Full production	clc401.cir	N/A	<input type="checkbox"/> Samples <input type="checkbox"/> Buy Now	1K+	\$3.6500	tube of 40	[logo]çUçZç2çT CLC401AJP
5962-8997301PA	Cerdip	8	Full production	clc401.cir	N/A	<input type="checkbox"/> Buy Now	25+	\$29.1000	tube of 40	[logo]çZçSç4çAçE CLC401AJ-QML 5962-8997301 PA
CLC401AJ	Cerdip	8	Full production	clc401.cir	N/A		500+	\$17.8000	tube of 40	[logo]çUçZç2çTçP CLC401AJ
CLC401AD-MLS	SB Cerdip	8	Full production	clc401.cir	N/A				tube of N/A	[logo]çZçSç4çA CLC401AD -MLS çE
CLC401AJ-MLS	Cerdip	8	Full production	clc401.cir	N/A		50+	\$220.0000	tube of 40	[logo]çZçSç4çAçE CLC401AJ-MLS

Design Tools

Title	Size (in Kbytes)	Date	<input type="checkbox"/> View Online	<input type="checkbox"/> Download	<input type="checkbox"/> Receive via Email
Amplifiers Selection Guide software for Windows	9 Kbytes	19-Mar-2001		View	
CLC730013EB 8-pin Op Amp Evaluation Board	130 Kbytes	2-Jan-2001	View Online	Download	Receive via Email
CLC730027EB 8-pin Op Amp Evaluation Board	130 Kbytes	2-Jan-2001	View Online	Download	Receive via Email

Please use [Adobe Acrobat](#) to view PDF file(s).

If you have trouble printing, see [Printing Problems](#).

Application Notes

Title	Size (in Kbytes)	Date	<input type="checkbox"/> View Online	<input type="checkbox"/> Download	<input type="checkbox"/> Receive via Email
OA-07: OA-07 Current- Feedback Op Amp Applications Circuit Guide	308 Kbytes	28-Oct-96	View Online	Download	Receive via Email
OA-11: OA-11 A Tutorial on Applying Op Amps to RF Applications	769 Kbytes	2-Apr-99	View Online	Download	Receive via Email
OA-12: OA-12 Noise Analysis for Comlinear's Op Amps	108 Kbytes	24-Feb-99	View Online	Download	Receive via Email
OA-13: OA-13 Current- Feedback Loop Gain Analysis	527 Kbytes	28-Oct-96	View Online	Download	Receive via Email
OA-14: OA-14 Improving Amplifier Noise Figure for High 3rd Intercept Amplifiers	92 Kbytes	15-Dec-00	View Online	Download	Receive via Email
OA-15: OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers	527 Kbytes	28-Jan-99	View Online	Download	Receive via Email
OA-18: OA-18 Simulation SPICE Models for Comlinear's Op Amps	337 Kbytes	23-May-00	View Online	Download	Receive via Email
OA-20: OA-20 Current Feedback Myths Debunked	139 Kbytes	10-Jul-97	View Online	Download	Receive via Email
OA-25: OA-25 Stability Analysis of Current Feedback Amplifier	262 Kbytes	10-Oct-96	View Online	Download	Receive via Email
OA-30: OA-30 Current vs. Voltage Feedback Amplifiers	56 Kbytes	5-Jun-98	View Online	Download	Receive via Email

Please use [Adobe Acrobat](#) to view PDF file(s).

If you have trouble printing, see [Printing Problems](#).

[Information as of 25-Apr-2001]

[Quick Search](#)

[Parametric
Search](#)

[System
Diagrams](#)

[Product
Tree](#)

[Home](#)

[About Languages](#) . [Website Guide](#) . [About "Cookies"](#) . National is [QS 9000 Certified](#)

[Site Terms & Conditions of Use](#) . Copyright 2001 © National Semiconductor Corporation

[Privacy/Security Statement](#) . [Preferences](#) . [Feedback](#)