

54LS253/DM54LS253/DM74LS253 TRI-STATE® Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

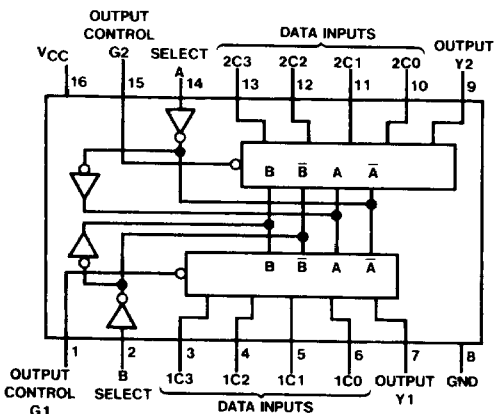
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
Data to output 12 ns
Select to output 21 ns
- Typical power dissipation 35 mW
- Alternate Military/Aerospace device (54LS253) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6416-1

Order Number 54LS253DMQB, 54LS253FMQB,
54LS253LMQB, DM54LS253J, DM54LS253W,
DM74LS253M or DM74LS253N
See NS Package Number E20A, J16A,
M16A, N16E or W16A

Function Table

| Select Inputs | | Data Inputs | | | | Output Control | Output |
|---------------|---|-------------|----|----|----|----------------|--------|
| B | A | C0 | C1 | C2 | C3 | G | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Address Inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (off).

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| DM54LS and 54LS | -55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | DM54LS253 | | | DM74LS253 | | | Units |
|-----------------|--------------------------------|-----------|-----|-----|-----------|-----|------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | -1 | | | -2.6 | mA |
| I _{OL} | Low Level Output Current | | | 12 | | | 24 | mA |
| T _A | Free Air Operating Temperature | -55 | | 125 | 0 | | 70 | °C |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
|------------------|---|--|--|--------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min | DM54 | 2.4 | 3.4 | V |
| | | | DM74 | 2.4 | 3.1 | |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min | DM54 | | 0.4 | V |
| | | | DM74 | | 0.5 | |
| | | | I _{OL} = 12 mA, V _{CC} = Min | DM74 | | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 7V | | | 0.1 | mA |
| I _{IH} | High Level Input Current | V _{CC} = Max, V _I = 2.7V | | | 20 | μA |
| I _{IL} | Low Level Input Current | V _{CC} = Max, V _I = 0.4V | | | -0.4 | mA |
| I _{OZH} | Off-State Output Current with High Level Output Voltage Applied | V _{CC} = Max, V _O = 2.7V V _{IH} = Min, V _{IL} = Max | | | 20 | μA |
| I _{OZL} | Off-State Output Current with Low Level Output Voltage Applied | V _{CC} = Max, V _O = 0.4V V _{IH} = Min, V _{IL} = Max | | | -20 | μA |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 2) | DM54 | -20 | -100 | mA |
| | | | DM74 | -20 | -100 | |
| I _{CC1} | Supply Current | V _{CC} = Max (Note 3) | | 7 | 12 | mA |
| I _{CC2} | Supply Current | V _{CC} = Max (Note 4) | | 8.5 | 14 | mA |

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, and all the inputs grounded.

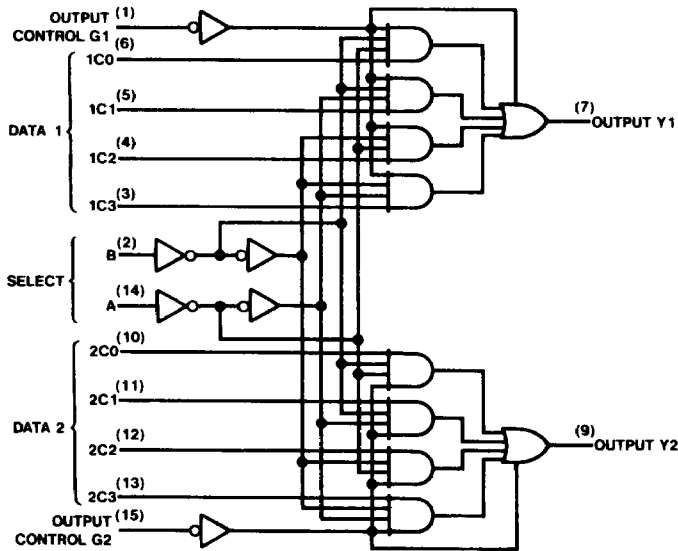
Note 4: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 687\Omega$ | | | | Units |
|-----------|--|-----------------------------|----------------------|-----|-----------------------|-----|-------|
| | | | $C_L = 45\text{ pF}$ | | $C_L = 150\text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Data to Y | | 25 | | 35 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Data to Y | | 20 | | 30 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Select to Y | | 45 | | 54 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Select to Y | | 32 | | 44 | ns |
| t_{PZH} | Output Enable Time to High Level Output | Output Control to Y | | 18 | | 32 | ns |
| t_{PZL} | Output Enable Time to Low Level Output | Output Control to Y | | 23 | | 35 | ns |
| t_{PHZ} | Output Disable Time from High Level Output (Note 1) | Output Control to Y | | 41 | | | ns |
| t_{PLZ} | Output Disable Time from Low Level Output (Note 1) | Output Control to Y | | 27 | | | ns |

Note 1: $C_L = 5\text{ pF}$.

Logic Diagram



TL/F/6416-2