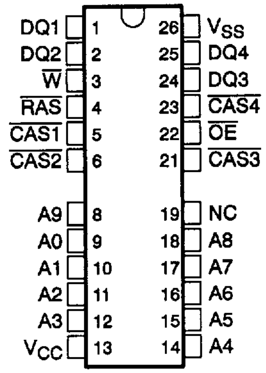
SMHS564A – MARCH 1995 – REVISED JUNE 1995

- **Organization . . . 1048576 × 4**
- **Single 5-V Power Supply for TMS44460/P (±10% Tolerance)**
- **Single 3.3-V Power Supply for TMS46460/P (±10% Tolerance)**
- **Low Power Dissipation (for TMS46460P)**
  - **200-μA CMOS Standby**
  - **200-μA Self Refresh**
  - **300-μA Extended-Refresh Battery Backup**
- **Performance Ranges:**

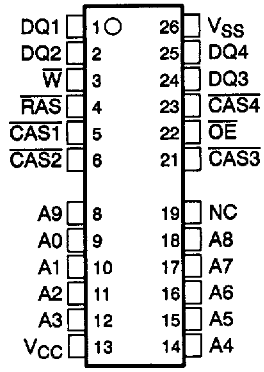
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4x460/P-60	60 ns	15 ns	30 ns	110 ns
'4x460/P-70	70 ns	18 ns	35 ns	130 ns
'4x460/P-80	80 ns	20 ns	40 ns	150 ns

- **Four Separate $\overline{CASx}$ Pins Provide for Separate I/O Operation**
- **Parity-Mode Operation**
- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  - **1024-Cycle Refresh in 16 ms**
  - **128 ms (Max) Low-Power, Self-Refresh Version (TMS4x460P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **Operating Free-Air Temperature Range 0°C to 70°C**

DJ PACKAGE
(TOP VIEW)



DGA PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS1}$–$\overline{CAS4}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

description

The TMS4x460 series are high-speed, 4194304-bit dynamic random-access memories, organized as 1048576 words of four bits each. The TMS4x400P series are high-speed, low-power, self-refresh with extended-refresh, 4194304-bit dynamic random-access memories, organized as 1048576 words of four bits each. Both series employ state-of-the-art enhanced performance implanted CMOS EPIC™ technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44460	5 V	—	1024 in 16 ms
TMS44460P	5 V	YES	1024 in 128 ms
TMS46460	3.3 V	—	1024 in 16 ms
TMS46460P	3.3 V	YES	1024 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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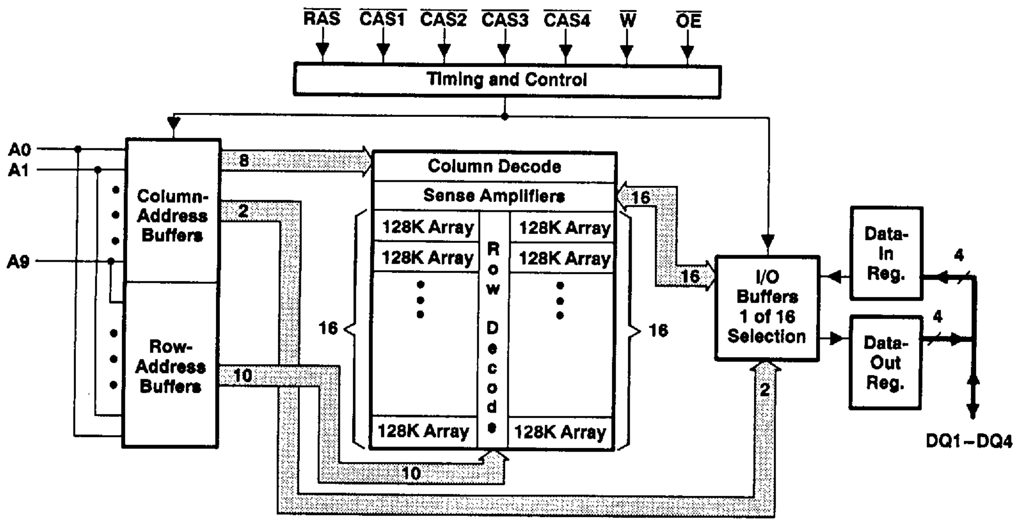
description (continued)

Four separate $\overline{\mathrm{CAS}}$ pins ($\overline{\mathrm{CAS1}}$–$\overline{\mathrm{CAS4}}$) provide for separate I/O operations, allowing this device to operate in parity mode. The TMS44460 also functions in enhanced page mode, similar to the TMS44400.

The TMS4x400 and TMS4x400P are offered in a 24/26-lead plastic small outline (TSOP) package (DGA suffix) and a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

functional block diagram



ADVANCE INFORMATION

operation

parity mode

Four $\overline{\mathrm{CASx}}$ pins ($\overline{\mathrm{CAS1}}$–$\overline{\mathrm{CAS4}}$) are provided to give independent control of the four data I/O pins (DQ1 – DQ4). For read or write cycles, the column addressed is latched on the first $\overline{\mathrm{CASx}}$ falling edge. Each $\overline{\mathrm{CASx}}$ pin going low enables its corresponding DQ pin with data coming from the column address latched on the first $\overline{\mathrm{CASx}}$ falling edge. All address setup and hold parameters are referenced to the first $\overline{\mathrm{CASx}}$ falling edge. The delay time from $\overline{\mathrm{CASx}}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{\mathrm{CASx}}$ to its corresponding DQx pin.

To latch in a new column address, all four $\overline{\mathrm{CASx}}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{\mathrm{CASx}}$ rising edge to the first $\overline{\mathrm{CASx}}$ falling edge of the new cycle. In order for a column address to remain valid while toggling $\overline{\mathrm{CASx}}$, there exists a minimum setup time (t_{CLCH}) where at least one $\overline{\mathrm{CASx}}$ must be brought low before all other $\overline{\mathrm{CASx}}$ pins are taken high.

For early-write cycles, the data is latched on the first $\overline{\mathrm{CASx}}$ falling edge. Only the DQs that have the corresponding $\overline{\mathrm{CASx}}$ low are written into. Each $\overline{\mathrm{CASx}}$ has to meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{\mathrm{CASx}}$ pins must come high and meet t_{CP}.

This DQ independence allows the TMS4x460/P to provide four parity bits in memory designs that normally require the use of four 1-megabit × 1 DRAMs.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CASx}$ page-cycle time used. With minimum $\overline{CASx}$ page-cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CASx}$ is high. The falling edge of $\overline{CASx}$ latches the column addresses. This feature allows the TMS4x400 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CASx}$ low) if t_{AA} max (access time from column address) has been satisfied. If column addresses for the next cycle are valid at the time $\overline{CASx}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CASx}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1048576 storage-cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CASx}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CASx}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CASx}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits (TMS44460/P) or low-voltage TTL circuits (TMS46460/P) without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CASx}$ (early write), data out remain in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CASx}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CASx}$ and $\overline{OE}$ are low. $\overline{CASx}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CASx}$ to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either $\overline{OE}$ or $\overline{CASx}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x400P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CASx}$ at the high (inactive) level,

refresh (continued)

conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding $\overline{CASx}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{CASx}$-before-$\overline{RAS}$ refresh (CBR)

CBR refresh is utilized by bringing $\overline{CASx}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CASx}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300-µA (TMS46460P) or 500-µA (TMS44460P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CASx}$ low prior to $\overline{RAS}$ going low. $\overline{CASx}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CASx}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS44460, TMS44460P .... – 1 V to 7 V
TMS46460, TMS46460P .... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS44460, TMS44460P .... – 1 V to 7 V
TMS46460, TMS46460P .... – 0.5 V to 4.6 V
Short-circuit output current .... 50 mA
Power dissipation .... 1 W
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{sttg} .... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		'44460/P			'46460/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.4		6.5	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS44460/P

PARAMETER		TEST CONDITIONS	'44460-60 '44460P-60 MIN	'44460-60 '44460P-60 MAX	'44460-70 '44460P-70 MIN	'44460-70 '44460P-70 MAX	'44460-80 '44460P-80 MIN	'44460-80 '44460P-80 MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	μA
I_O	Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC}, $\overline{CASx}$ high		± 10		± 10		± 10	μA
I_{CC1}	Read- or write-cycle current (see Note)	$V_{CC} = 5.5$ V, Minimum cycle		105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, $V_{IH} = 2.4$ V (TTL)		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, $V_{IH} = V_{CC} - 0.2$ V (CMOS) — '44460		1		1		1	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, $V_{IH} = V_{CC} - 0.2$ V (CMOS) — '44460P		500		500		500	μA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	$V_{CC} = 5.5$ V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CASx}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CASx}$ low (CBR)		105		90		80	mA
I_{CC4}	Average page current (see Notes 4 and 5)	$V_{CC} = 5.5$ V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CASx}$ cycling		90		80		70	mA
I_{CC6}†	Self-refresh current (see Note 4)	$\overline{CASx} < 0.2$ V, $\overline{RAS} < 0.2$ V, t_{RAS} and $t_{CAS} > 1000$ ms		500		500		500	μA
I_{CC7}	Standby current, outputs enabled (see Note 4)	$\overline{RAS} = V_{IH}$, $\overline{CASx} = V_{IL}$, Data out enabled		5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	$t_{RC} = 125$ μs, $t_{RAS} \le 1$ μs, $V_{CC} - 0.2\ V \le V_{IH} \le 6.5$ V, $0\ V \le V_{IL} \le 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable		500		500		500	μA

† For TMS44460P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
5. Measured with a maximum of one address change while $\overline{CASx} = V_{IH}$

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS46460/P

PARAMETER		TEST CONDITIONS		'46460-60 '46460P-60		'46460-70 '46460P-70		'46460-80 '46460P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA (LVTTL)		2.4		2.4		2.4		V
		I_{OH} = – 100 μA (LVCMOS)		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (LVTTL)			0.4		0.4		0.4	V
		I_{OL} = 100 μA (LVCMOS)			0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	μA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CASx}$ high			± 10		± 10		± 10	μA
I_{CC1}	Read- or write-cycle current (see Note)	V_{CC} = 3.6 V, Minimum cycle			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, V_{IH} = 2 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CASx}$ high, $V_{IH} = V_{CC} - 0.2$ V (LVCMOS)	'46460		300		300		300	μA
			'46460P		200		200		200	μA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CASx}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CASx}$ low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Notes 4 and 5)	V_{CC} = 3.6 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CASx}$ cycling			60		50		40	mA
I_{CC6}†	Self-refresh current (see Note 4)	$\overline{CASx}$< 0.2 V, $\overline{RAS}$< 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	μA
I_{CC7}	Standby current, outputs enabled (see Note 4)	$\overline{RAS} = V_{IH}$, $\overline{CASx} = V_{IL}$, Data out enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs, $V_{CC} - 0.2\ V \le V_{IH} \le 3.9$ V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			300		300		300	μA

† For TMS46460P only

NOTES: 4. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
5. Measured with a maximum of one address change while $\overline{CASx} = V_{IH}$

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A9		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CASx}$ and $\overline{RAS}$		7	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± .5 V for the TMS44460/P devices, V_{CC} = 3.3 V ± 0.3 V for the TMS46460/P devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CASx}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CASx}$ to output in low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CASx}$ high (see Note 7)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x400-60 '4x400P-60		'4x400-70 '4x400P-70		'4x400-80 '4x400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 8)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 8)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASS}	Pulse duration, $\overline{RAS}$ low, self refresh		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CASx}$ low (see Note 11)	10	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CASx}$ precharge time	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RPS}	Precharge time after self refresh using $\overline{RAS}$	110		130		150		ns
t_{WP}	Pulse duration, write	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CASx}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CASx}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CASx}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CASx}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CASx}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CASx}$ low to $\overline{CASx}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CASx}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CASx}$ low (early-write operation only)	10		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CHS}	Hold time, $\overline{CASx}$ low after $\overline{RAS}$ high (self refresh)	–50		–50		–50		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CASx}$ or $\overline{W}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

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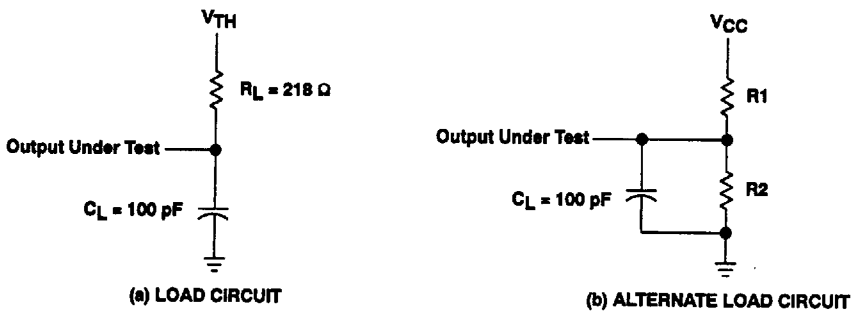
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4x460-60 '4x460P-60		'4x460-70 '4x460P-70		'4x460-80 '4x460P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{OED}	Hold time, $\overline{OE}$ to data delay		15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CASx}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CASx}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 15)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{REF}	Refresh time interval	'4x460		16		16		16	ms
		'4x460P		128		128		128	ms
t_T	Transition time		2	30	2	30	2	30	ns

NOTE 15: The maximum value is specified only to assure access time.

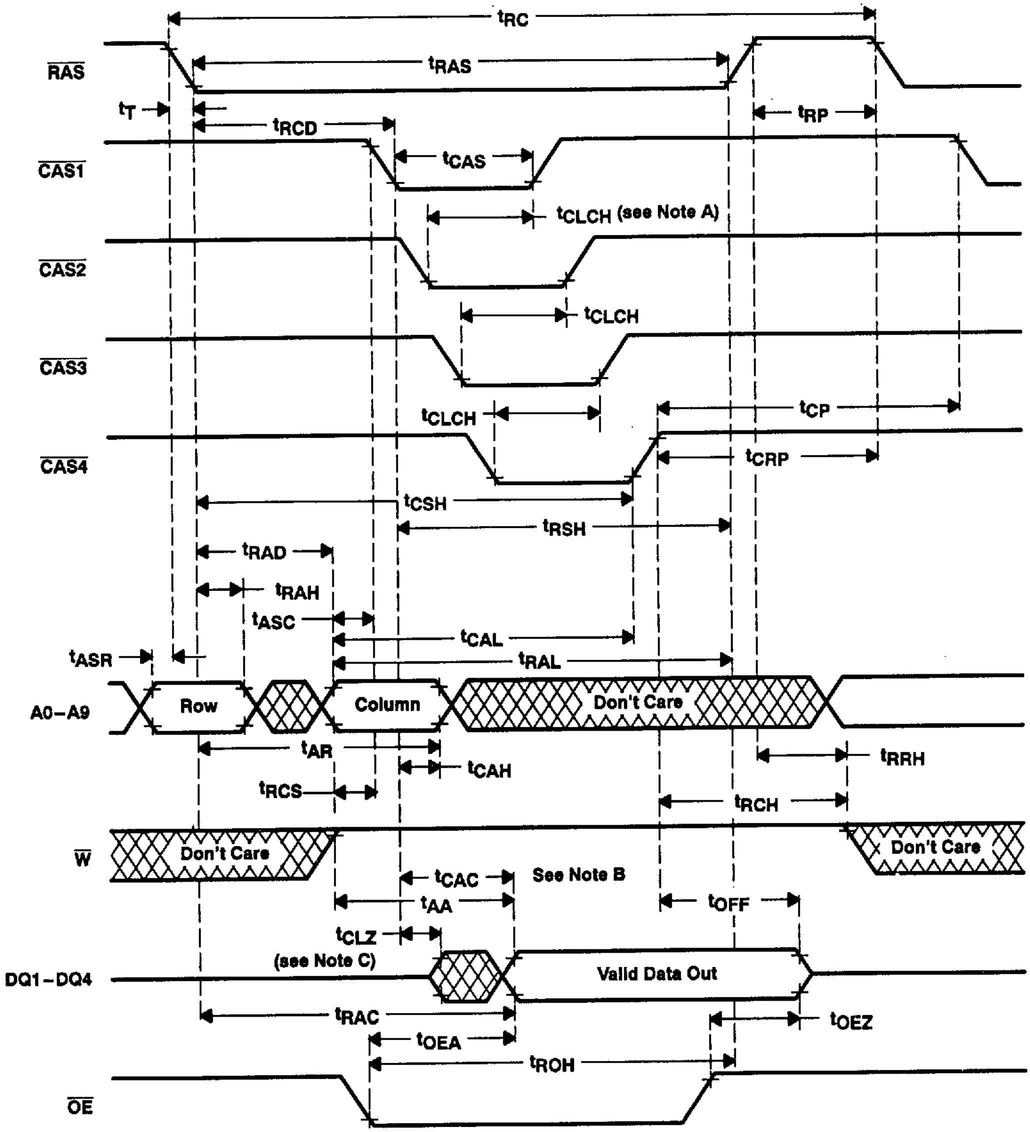
PARAMETER MEASUREMENT INFORMATION



DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
46460/P	3.3	1178	868	1.4	500
44460/P	5	828	295	1.31	218

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. Output can go from high-impedance to an invalid-data state prior to the specified access time.
D. $\overline{CASx}$ order is arbitrary.

Figure 2. Read-Cycle Timing (see Note D)

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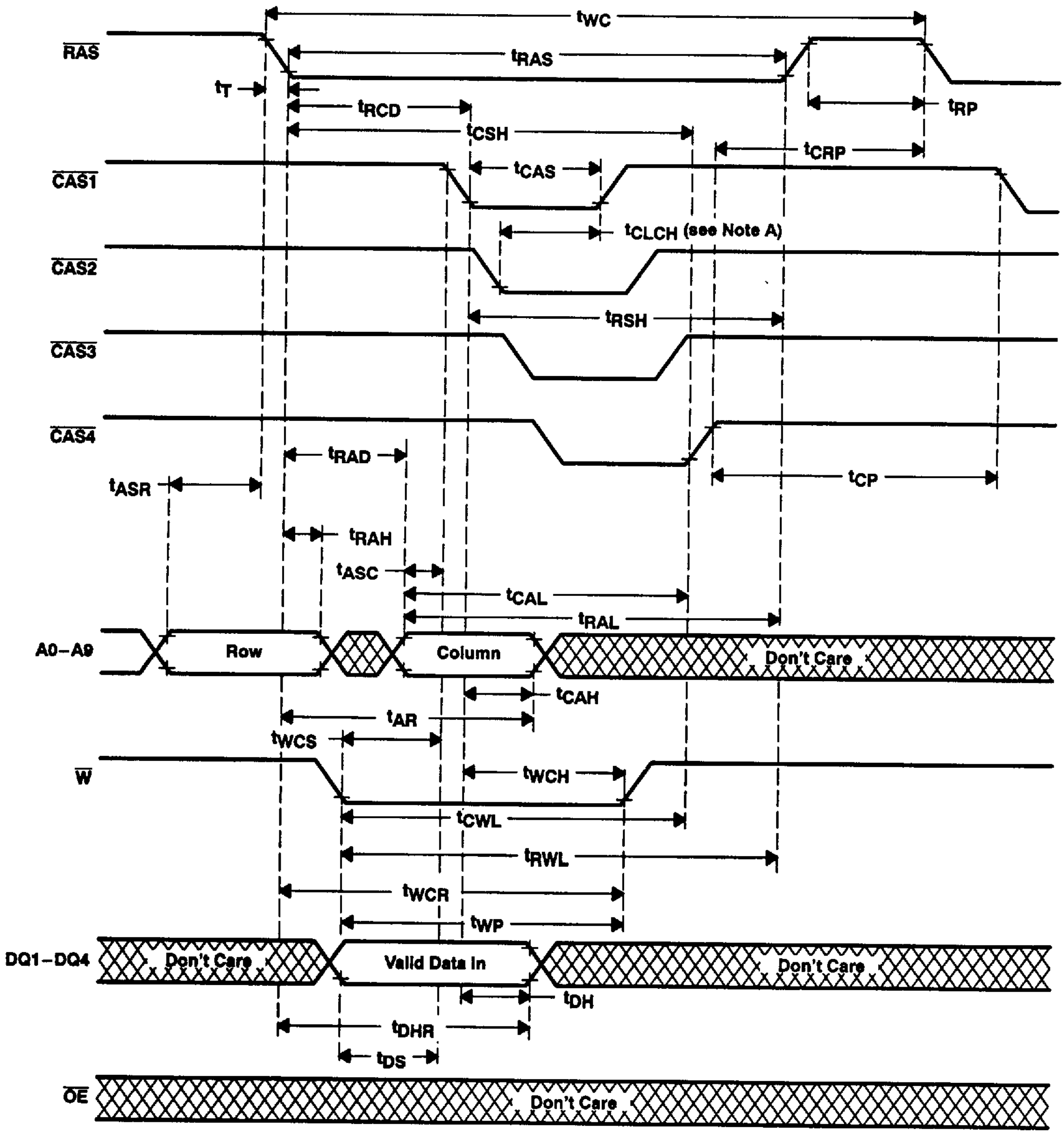
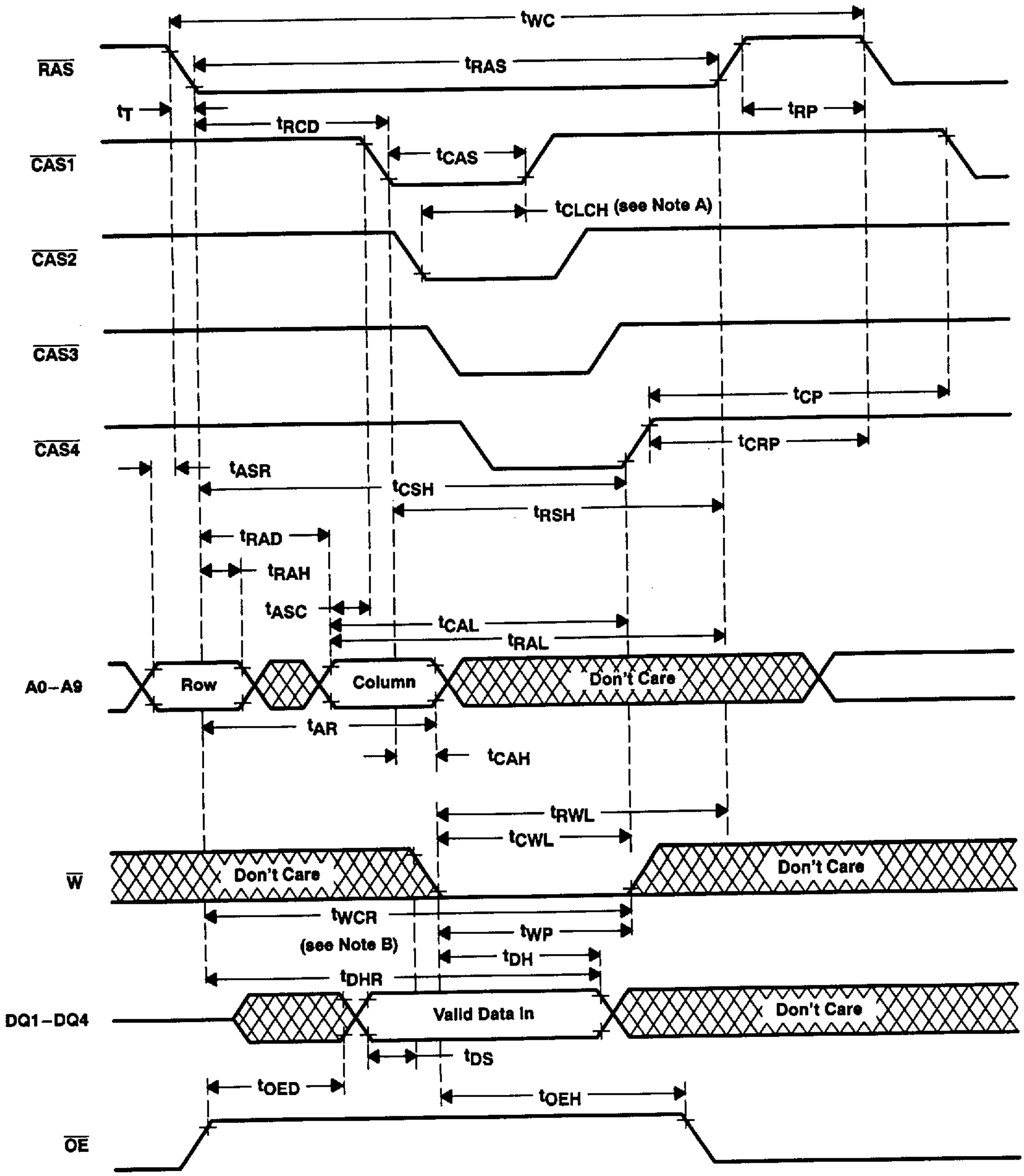


NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{CASx}$ order is arbitrary.

Figure 3. Early-Write-Cycle Timing (see Note B)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{CASx}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the later of either the first $\overline{\text{CASx}}$ or $\overline{\text{W}}$ in write operations.
C. $\overline{\text{CASx}}$ order is arbitrary.

Figure 4. Write-Cycle Timing (see Note C)

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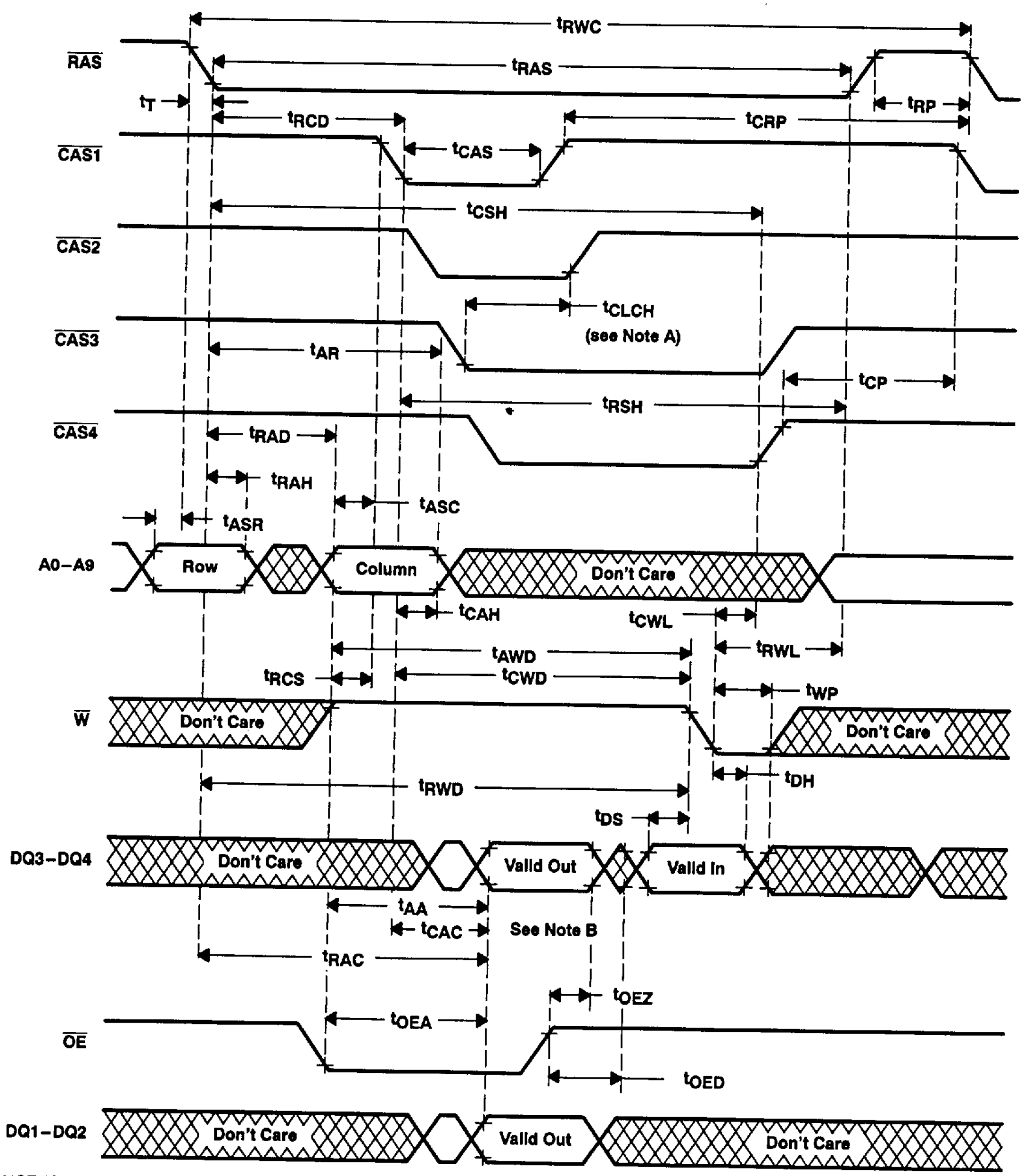
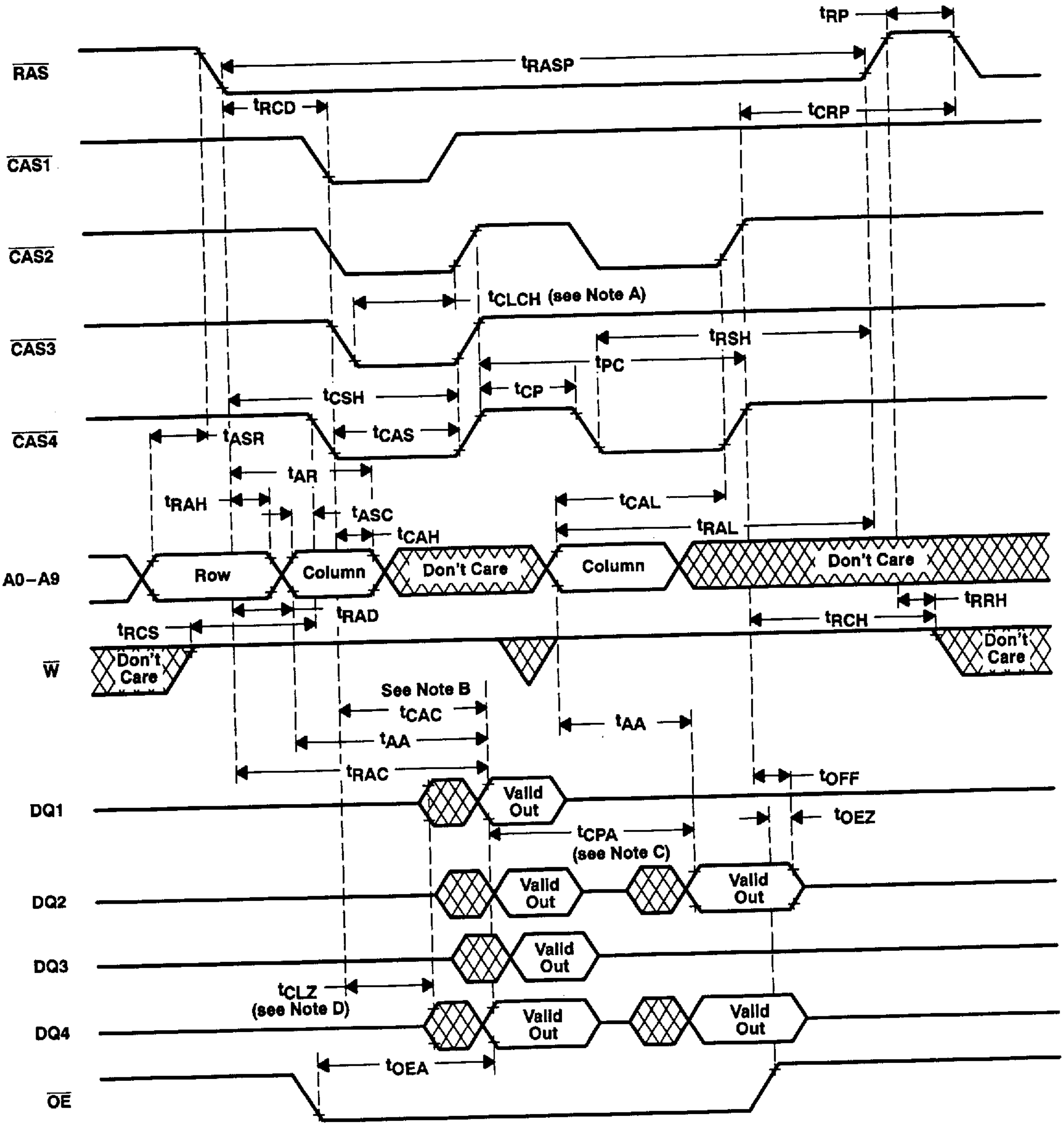


NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. $\overline{CASx}$ order is arbitrary.

Figure 5. Read-Write/Read-Modify-Write-Cycle Timing (see Note C)

PARAMETER MEASUREMENT INFORMATION



NOTES:
A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from high-impedance to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. $\overline{CASx}$ order is arbitrary.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing (see Notes E and F)

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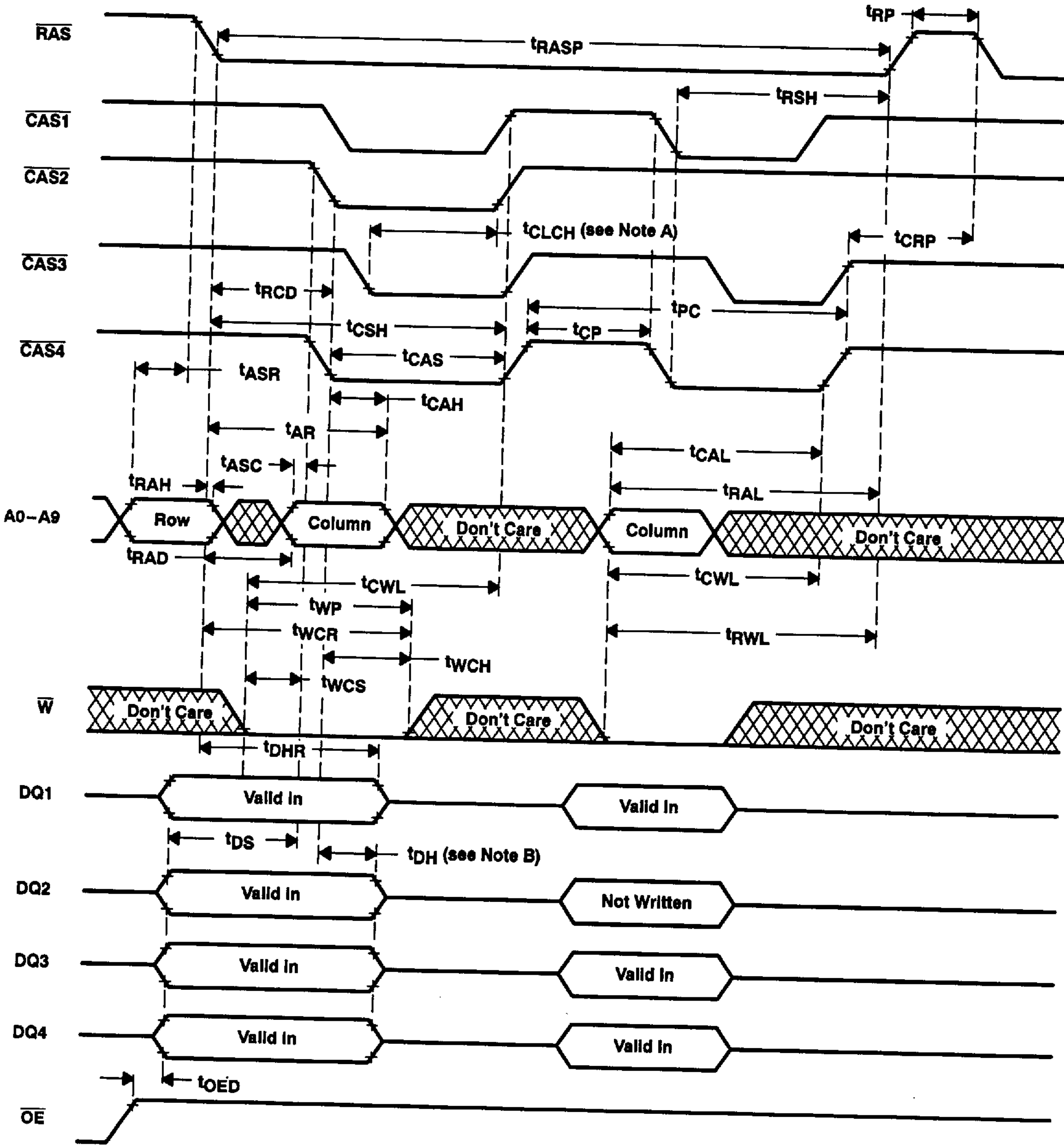

NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the later of either the first $\overline{CASx}$ or $\overline{W}$ in write operations.
C. $\overline{CASx}$ order is arbitrary.
D. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

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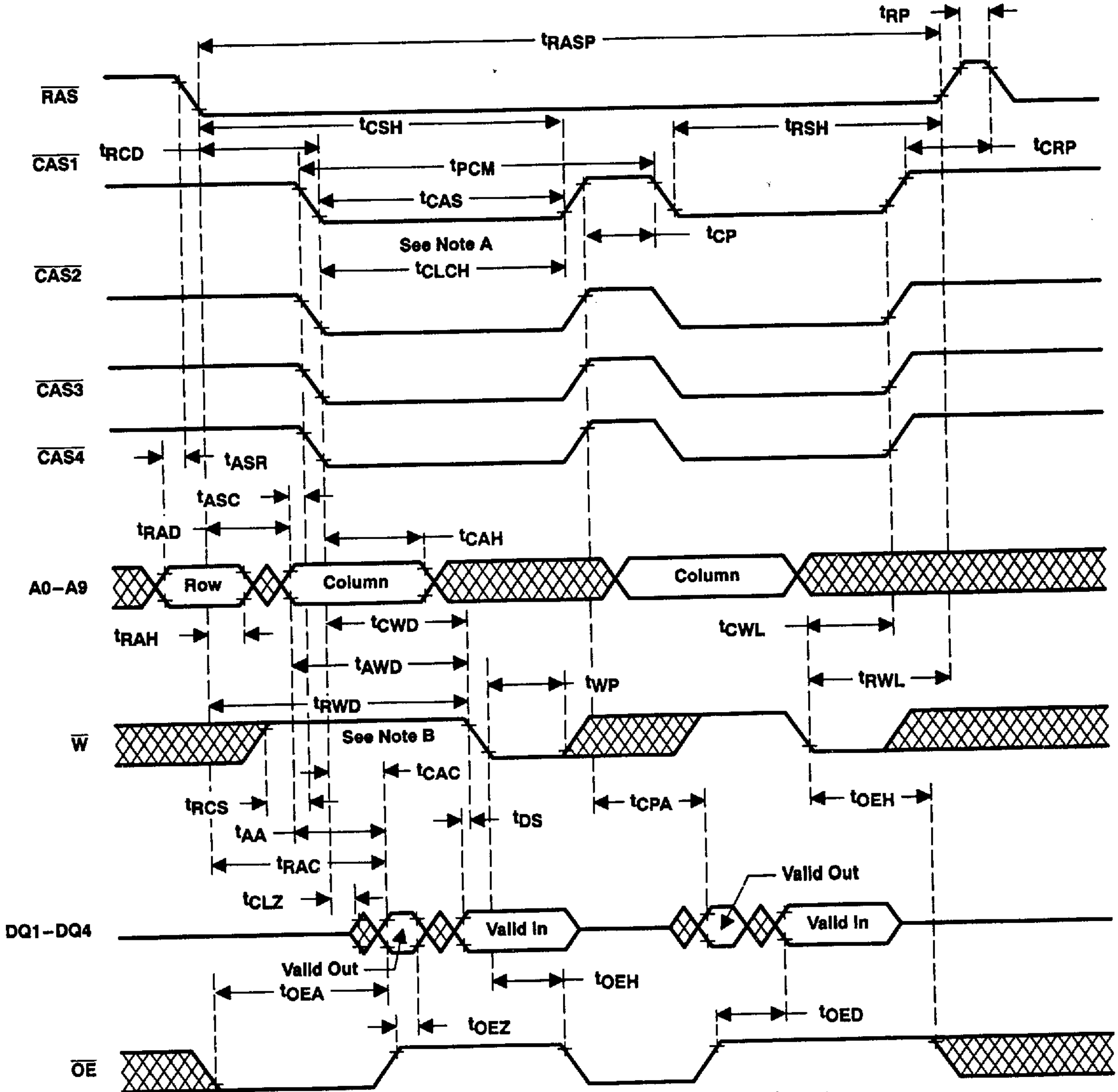

NOTES: A. To hold the address latched by the first $\overline{CASx}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{CASx}$ to its corresponding DQx.
C. $\overline{CASx}$ order is arbitrary.
D. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write Cycle Timing

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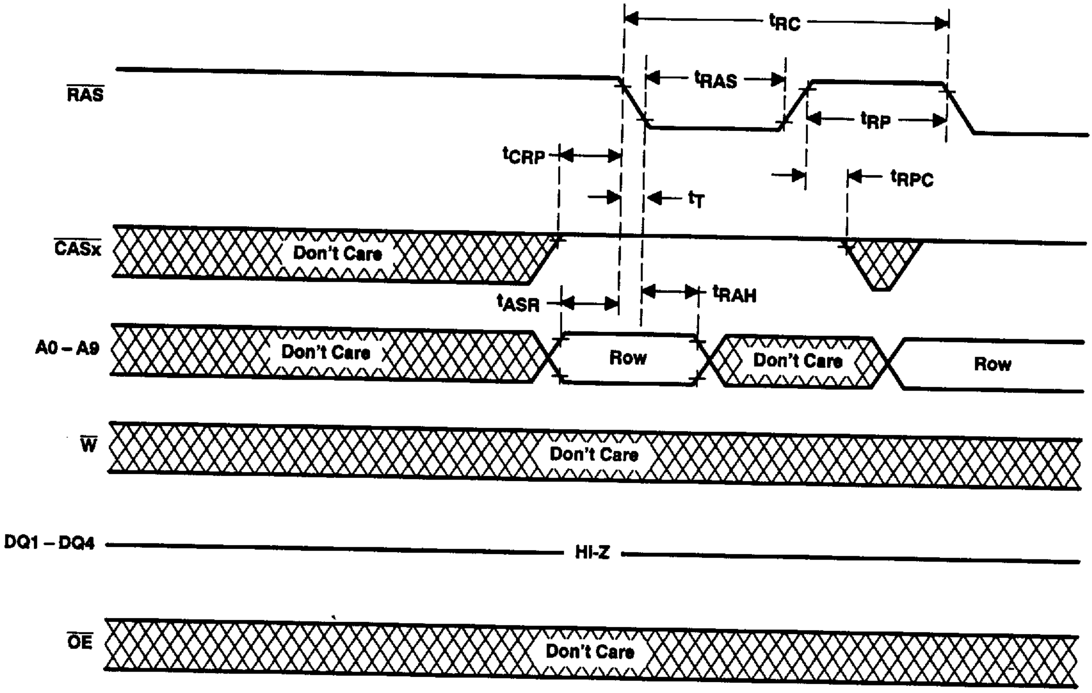
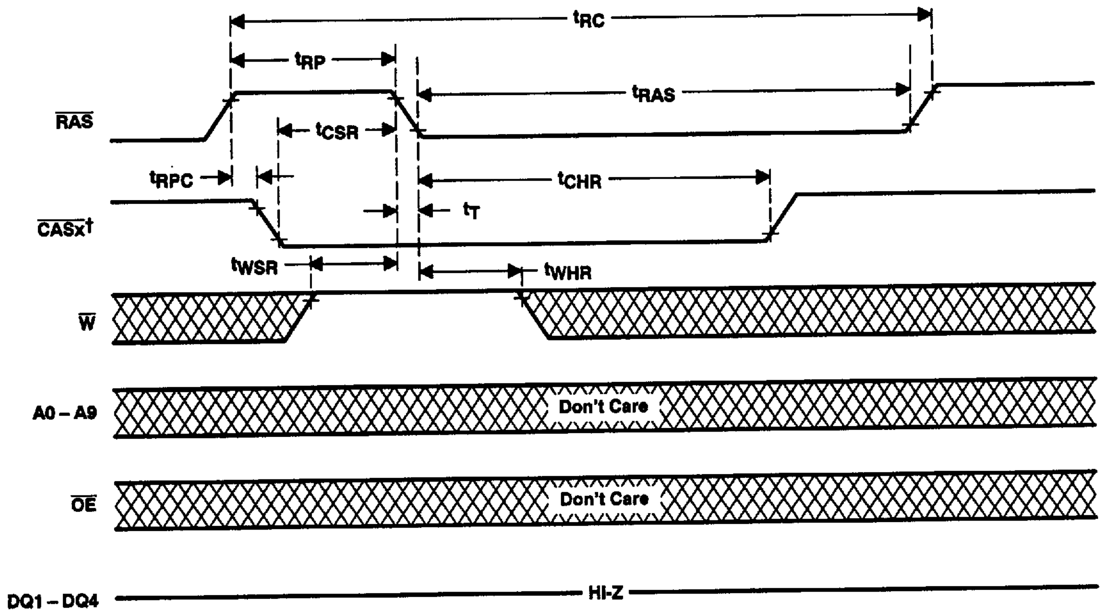


Figure 9. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Any CASx can be used.

Figure 10. Automatic CBR Refresh-Cycle Timing

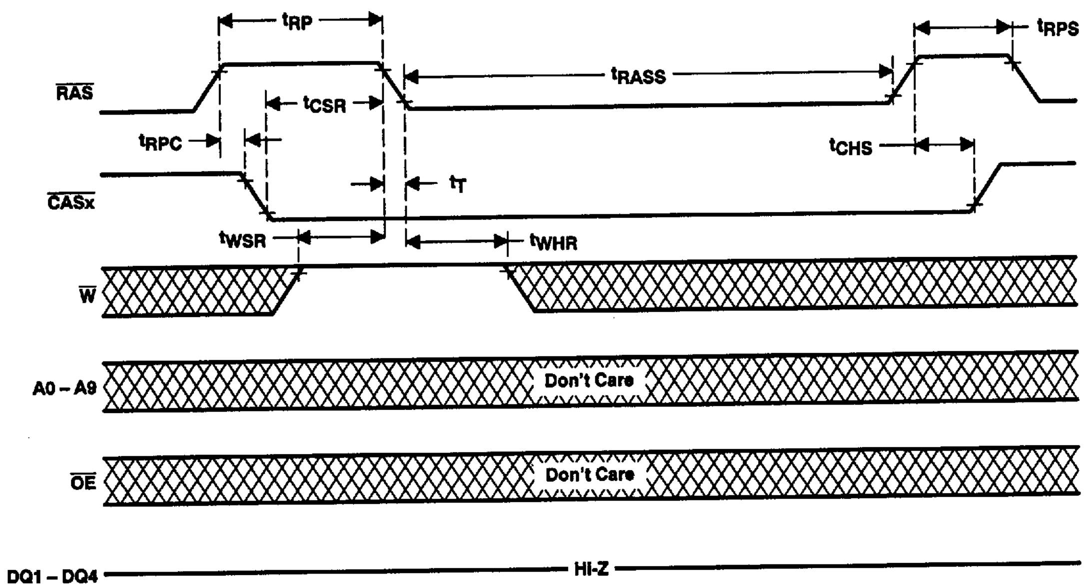


Figure 11. Self-Refresh-Cycle Timing

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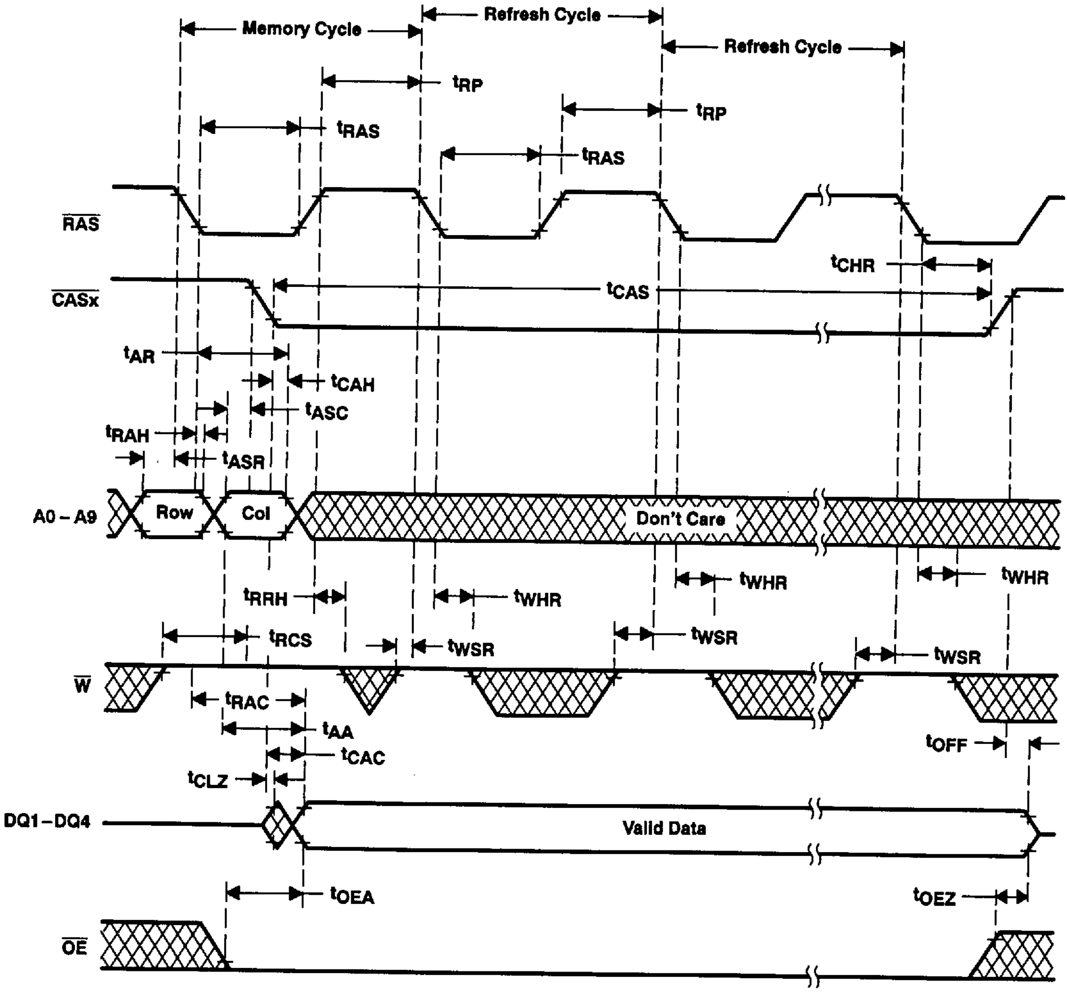

Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

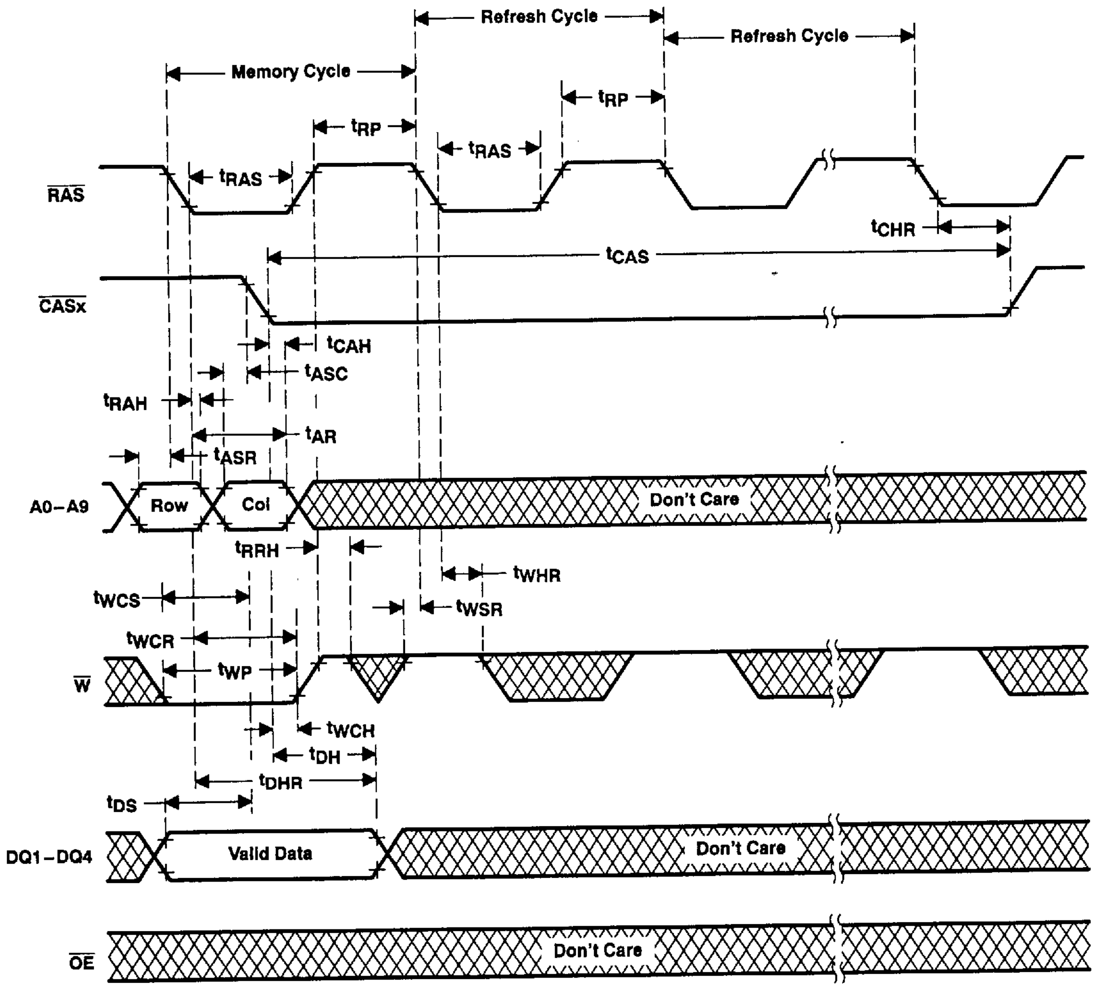

Figure 13. Hidden-Refresh-Cycle (Write) Timing

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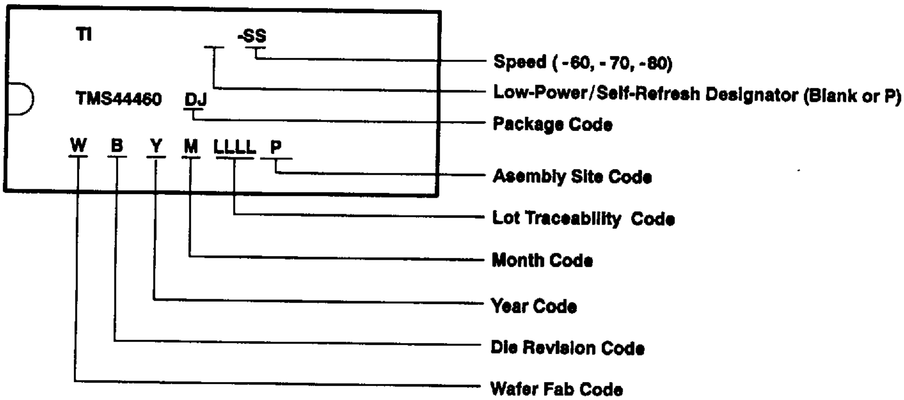
device symbolization (TMS44460 illustrated)



8961725 0084897 311