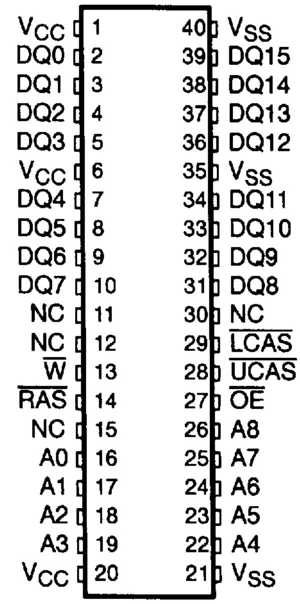
- **Organization . . . 262144 × 16**
- **5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

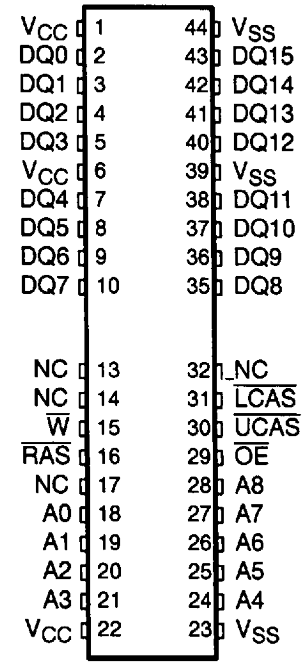
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45169/P-50	50 ns	13 ns	25 ns	84 ns
'45169/P-60	60 ns	15 ns	30 ns	110 ns
'45169/P-70	70 ns	20 ns	35 ns	130 ns

- **Extended Data Out (EDO) Operation CAS-Before-RAS (CBR) Refresh**
- **Long Refresh Period**
  - **512-Cycle Refresh in 8 ms (Max)**
  - **64 ms Max for Low-Power Version With Self Refresh (TMS45169P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **All Inputs, Outputs, and Clocks Are TTL Compatible**
- **High-Reliability, 40-Lead, 400-Mil-Wide Plastic Surface-Mount Small Outline J-Lead (SOJ) Package and 40/44-Lead Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low Power With Self-Refresh Version**
- **Upper- and Lower-Byte Control During Read and Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
DQ0–DQ15	Data In/Data Out
LCAS	Lower Column-Address Strobe
UCAS	Upper Column-Address Strobe
NC	No Internal Connection
OE	Output Enable
RAS	Row-Address Strobe
W	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS45169 series are high-speed, 4194304-bit dynamic random-access memories (DRAMs) organized as 262144 words of 16 bits each. The TMS45169P series are high-speed, low-power, self-refresh 4194304-bit DRAMs organized as 262144 words of 16 bits each. They employ state-of-the-art EPIC™ technology for high performance, reliability, and low power at low cost.

These devices feature maximum RAS access times of 50 ns, 60 ns, and 70 ns. Maximum power dissipation is as low as 880 mW operating and 11 mW standby on 80-ns devices. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

description (continued)

The TMS45169 and TMS45169P each are offered in a 40-lead plastic surface-mount SOJ package (DZ suffix) and a 40/44-lead plastic surface-mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{\text{CAS}}$

Two $\overline{\text{CAS}}$ pins ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$) are provided to give independent control of the 16 data I/O pins (DQ0–DQ15) with $\overline{\text{LCAS}}$ corresponding to DQ0–DQ7 and $\overline{\text{UCAS}}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{\text{xCAS}}$ falling edge. Each $\overline{\text{xCAS}}$ going low enables its corresponding DQx pins with data associated with the column address latched on the first falling $\overline{\text{xCAS}}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{\text{xCAS}}$ edge.The delay time from $\overline{\text{xCAS}}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{\text{xCAS}}$ to its corresponding DQx pins.

In order to latch in a new column address, both $\overline{\text{xCAS}}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{\text{xCAS}}$ rising edge to the first falling $\overline{\text{xCAS}}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{\text{xCAS}}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{\text{xCAS}}$ must be brought low before the other $\overline{\text{xCAS}}$ is taken high.

For early-write cycles, the data is latched on the first falling edge of $\overline{\text{xCAS}}$. Only the DQs that have the corresponding $\overline{\text{xCAS}}$ low are written into. Each $\overline{\text{xCAS}}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, both $\overline{\text{xCAS}}$ pins must go high and meet t_{CP}.

extended data out

Extended data out allows for data output rates of up to 40 MHz for 60-ns devices. By keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{\text{RAS}}$ low time.

Extended data out does not place the DQs into the high-impedance state with the rising edge of $\overline{\text{xCAS}}$. The output remains valid for the system to latch the data. After $\overline{\text{xCAS}}$ goes high, the DRAM decodes the next address. $\overline{\text{OE}}$ and $\overline{\text{W}}$ can be used to control the output impedance. Descriptions of $\overline{\text{OE}}$ and $\overline{\text{W}}$ further explain EDO operation benefit.

address (A0–A8)

Eighteen address bits are required to decode each of the 262144 storage-cell locations. Nine row-address bits are set up on A0 through A8 and latched onto the chip by $\overline{\text{RAS}}$. Then, nine column-address bits are set up on A0 through A8 and latched onto the chip by the first $\overline{\text{xCAS}}$. All addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{xCAS}}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through $\overline{\text{W}}$. A logic high on $\overline{\text{W}}$ selects the read mode and a logic low selects the write mode. $\overline{\text{W}}$ can be driven from the standard TTL circuits without a pullup resistor. The data input lines are disabled when the read mode is selected. When $\overline{\text{W}}$ goes low prior to $\overline{\text{xCAS}}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{\text{OE}}$ grounded. If $\overline{\text{W}}$ goes low in an extended-data-out read cycle, the DQs are disabled so long as $\overline{\text{xCAS}}$ is high (see Figure 9).

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{xCAS}}$ and the data is strobed in by the first occurring $\overline{\text{xCAS}}$ with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, $\overline{\text{xCAS}}$ is already low and the data is strobed in by $\overline{\text{W}}$ with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, $\overline{\text{OE}}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines. The DQs drive valid data after all access times are met and remain valid except in the case described in the $\overline{\text{W}}$ and $\overline{\text{OE}}$ sections.

data out (DQ0–DQ15)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{xCAS}}$ and $\overline{\text{OE}}$ are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC} (which begins with the negative transition of $\overline{\text{xCAS}}$) as long as t_{RAC} and t_{AA} are satisfied. The DQs drive valid data after all access times are met and remain valid except in the case described in the $\overline{\text{W}}$ and $\overline{\text{OE}}$ sections.

output enable ($\overline{\text{OE}}$)

$\overline{\text{OE}}$ controls the impedance of the output buffers. While $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are low and $\overline{\text{W}}$ is high, $\overline{\text{OE}}$ can be brought low or high and the DQs transition between valid data and high impedance (see Figure 8). There are two methods for placing the DQs into the high-impedance state and keeping them that way during $\overline{\text{xCAS}}$ high time. The first method is to transition $\overline{\text{OE}}$ high before $\overline{\text{xCAS}}$ transitions high and keep $\overline{\text{OE}}$ high for t_{CHO} past the $\overline{\text{xCAS}}$ transition. This disables the DQs and they remain disabled, regardless of $\overline{\text{OE}}$, until $\overline{\text{xCAS}}$ falls again. The second method is to have $\overline{\text{OE}}$ low as $\overline{\text{xCAS}}$ transitions high. Then $\overline{\text{OE}}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{\text{xCAS}}$ high time; therefore, disabling the DQs regardless of further transitions on $\overline{\text{OE}}$ until $\overline{\text{xCAS}}$ falls again.

$\overline{\text{RAS}}$-only refresh

A refresh operation must be performed at least once every 8 ms (64 ms for TMS45169P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding all $\overline{\text{xCAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{xCAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ refresh

$\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing at least one $\overline{\text{xCAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive $\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{xCAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500-µA refresh current is available on the TMS45169P. Data integrity is maintained using $\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$ refresh with a period of 125 µs holding $\overline{\text{RAS}}$ low for less than 1 µs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

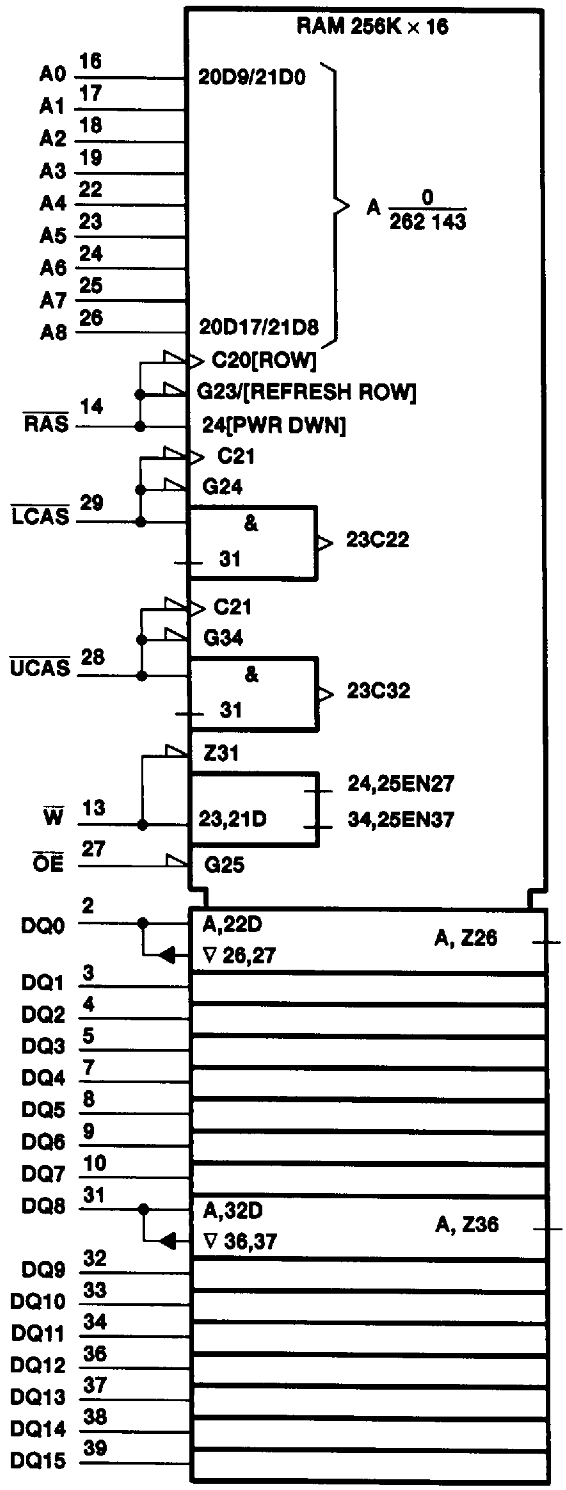
self refresh (TMS45169P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 µs. The chip is refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures that the DRAM is refreshed fully.

power up

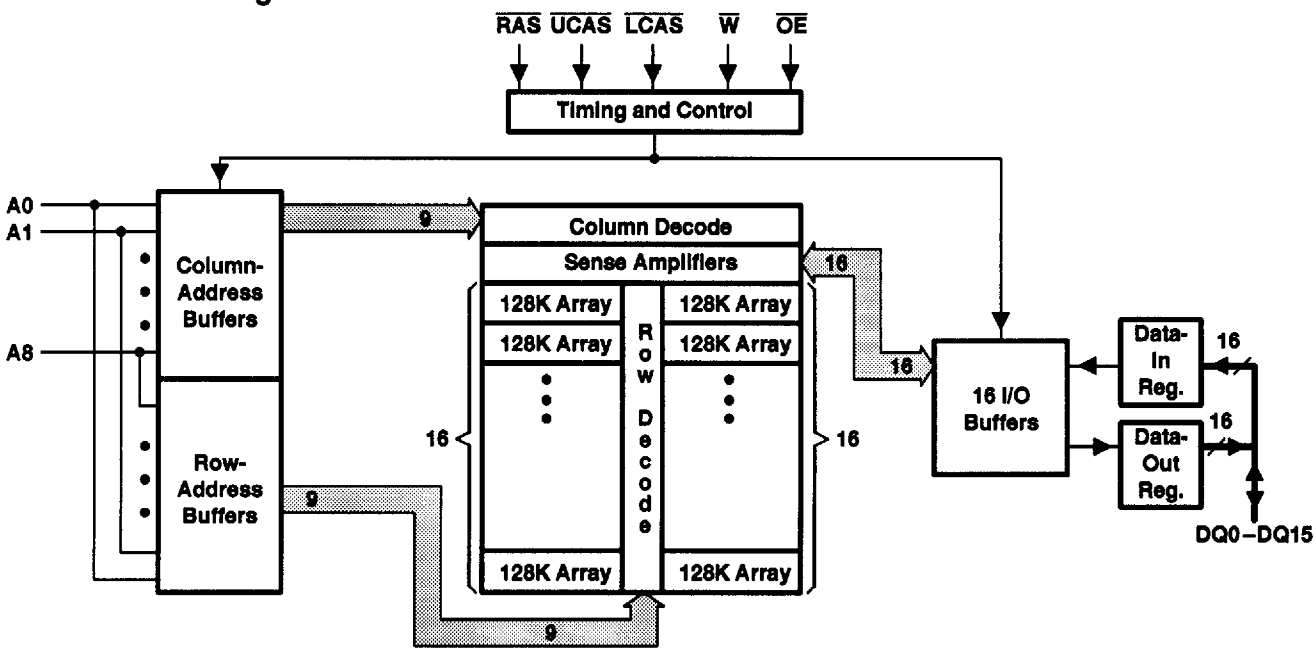
To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power up to the full V_{CC} level.These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or $\overline{\text{xCAS}}$-before-$\overline{\text{RAS}}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45169-50 '45169P-50		'45169-60 '45169P-60		'45169-70 '45169P-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA		2.0		2.4		2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA			0.8		0.4		0.4	V
I_I	Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	μA
I_O	Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	μA
I_{CC1}†‡	Read- or write-cycle current	$V_{CC} = 5.5$ V, Minimum cycle			190		180		160	mA
I_{CC2}	Standby current	$V_{IH} = 2.4$ V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		$V_{IH} = V_{CC} - 0.2$ V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'45169		1		1		1	mA
			'45169P		350		350		350	μA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$V_{CC} = 5.5$ V, Minimum cycle, ($\overline{RAS}$-only), $\overline{RAS}$ cycling, $\overline{xCAS}$ high (CBR only), $\overline{RAS}$ low after $\overline{xCAS}$ low			190		180		160	mA
I_{CC4}†‡	Average EDO page current	$V_{CC} = 5.5$ V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			160		160		140	mA
I_{CC5}¶	Battery-backup operating current (equivalent refresh time is 64 ms); CBR only	$t_{RC} = 125$ μs, $t_{RAS} \le 1$ μs, $V_{CC} - 0.2 V \le V_{IH} \le 6.5$ V, $0 V \le V_{IL} \le 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and data stable			500		500		500	μA
I_{CC6}†¶	Self-refresh current	$\overline{xCAS} < 0.2$ V, $\overline{RAS} < 0.2$ V, t_{RAS} and $t_{CAS} > 1000$ ms			400		400		400	μA

† Measured with outputs open
‡ Measured with a maximum of one address change while $\overline{xCAS} = V_{IH}$
§ Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$
¶ For TMS45169P only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz# (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

Capacitance measurements are made on a sample basis only.
NOTE 3: $V_{CC} = 5$ V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'45169-50 '45169P-50		'45169-60 '45169P-60		'45169-70 '45169P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		13		15		20	ns
t_{AA}	Access time from column address		25		30		35	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 5)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$ low		13		15		20	ns
t_{CPA}	Access time from column precharge		28		35		40	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low impedance	0		0		0		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	3	13	3	15	3	20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	3	13	3	15	3	20	ns
t_{CEZ}	Output disable time after $\overline{xCAS}$ high	3	13	3	15	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ low	3	13	3	15	3	20	ns

NOTES: 4. Maximum t_{REZ}, t_{CEZ}, t_{WEZ}, and t_{OEZ} are specified when the outputs are no longer driven.
5. 50 ns specifications are measured with C_L = 50 pF, V_{OL} = 0.8 V, and V_{OH} = 2.0 V

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'45169-50 '45169P-50		'45169-60 '45169P-60		'45169-70 '45169P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	20		25		30		ns
t_{CSH}	Hold time, $\overline{xCAS}$ from $\overline{RAS}$	40		50		55		ns
t_{CHO}	Hold time, $\overline{OE}$ after $\overline{xCAS}$	8		10		10		ns
t_{DOH}	Hold time, output from $\overline{xCAS}$	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{xCAS}$	8	10000	10	10000	12	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{xCAS}$	8		10		10		ns
t_{CP}	Precharge time, $\overline{xCAS}$	8		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 6)

		'45169-50 '45169P-50		'45169-60 '45169P-60		'45169-70 '45169P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	84		110		130		ns
t_{WC}	Cycle time, write	84		110		130		ns
t_{RWC}	Cycle time, read-write/read-modify-write	111		150		180		ns
t_{PRWC}	Cycle time, EDO page-mode read-write	57		80		85		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	8	10 000	10	10 000	15	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	30		40		50		ns
t_{WP}	Pulse duration, write	8		10		10		ns
t_{ASC}	Setup time, column address before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ high	8		10		15		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	8		10		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{xCAS}$ low (see Note 11)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns

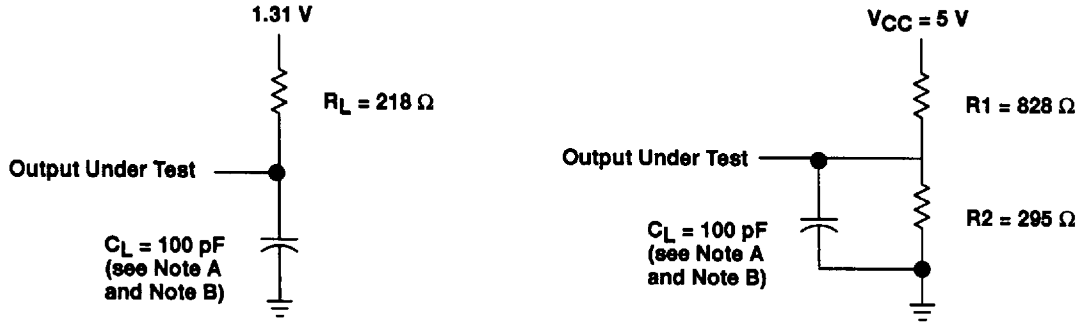
NOTES: 6. Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.
7. 50 ns specifications assume t_T = 2 ns; 60 and 70 ns assume t_T = 5 ns
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
11. Early-write operation only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 6)

			'45169-50 '45169P-50		'45169-60 '45169P-60		'45169-70 '45169P-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{xCAS}$ low (see Note 10)		8		10		15		ns
t_{DH}	Hold time, data after $\overline{xCAS}$ low (see Note 10)		8		10		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low		8		10		10		ns
t_{RCH}	Hold time, read after $\overline{xCAS}$ high (see Note 13)		0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 13)		0		0		0		ns
t_{WCH}	Hold time, write after $\overline{xCAS}$ low (see Note 13)		8		10		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high		5		5		5		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$		8		10		10		ns
t_{CHS}	Hold time, $\overline{xCAS}$ low after $\overline{RAS}$ high (for self refresh)		– 50		– 50		– 50		ns
t_{OEH}	Hold time, $\overline{OE}$ command		10		15		20		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)		45		55		65		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (see Note 12)		8		15		15		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (see Note 12)		5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (see Note 14)		30		40		50		ns
t_{OED}	Delay time, valid data in after $\overline{OE}$ high		13		15		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high		25		20		25		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 15)		18	35	20	45	20	50	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high		8		10		15		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)		67		85		100		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{xCAS}$ precharge (read-write only)		45		54		64		min
t_{CPR}	Pulse duration, $\overline{xCAS}$ precharge before self refresh		0		0		0		ns
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		84		110		130		ns
t_{RASS}	Pulse duration, self refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{REF}	Refresh time interval	'45169		8		8		8	ms
		'45169P		64		64		64	
t_T	Transition time		2	50	2	50	2	50	ns

NOTES:
6. Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.
10. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
12. CBR refresh only
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only
15. Maximum value specified only to assure access time

PARAMETER MEASUREMENT INFORMATION



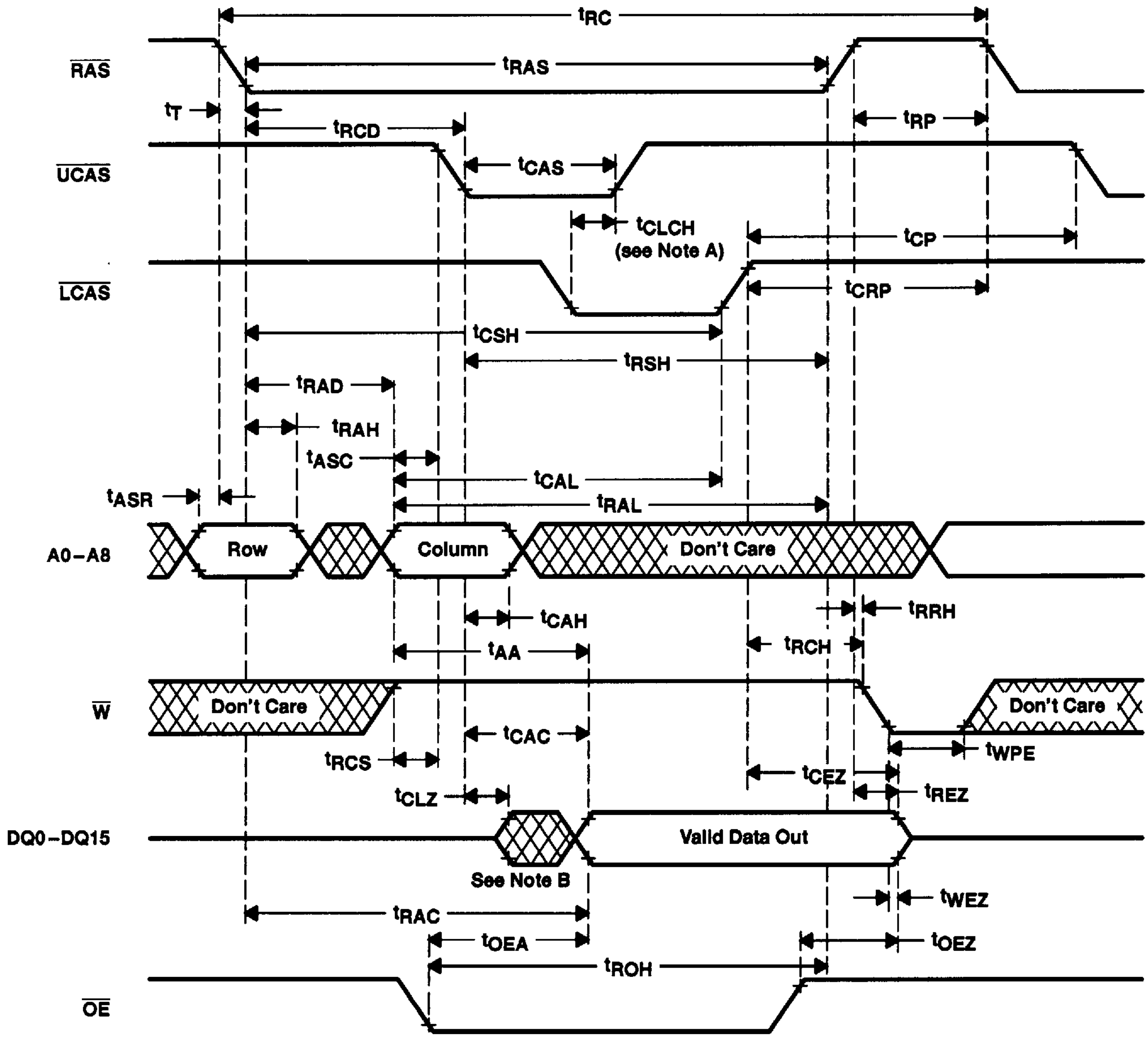
(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTES: A. C_L includes probe and fixture capacitance.
B. 50 ns specifications are measured with C_L = 50 pF

Figure 1. Load Circuits for Timing Parameters

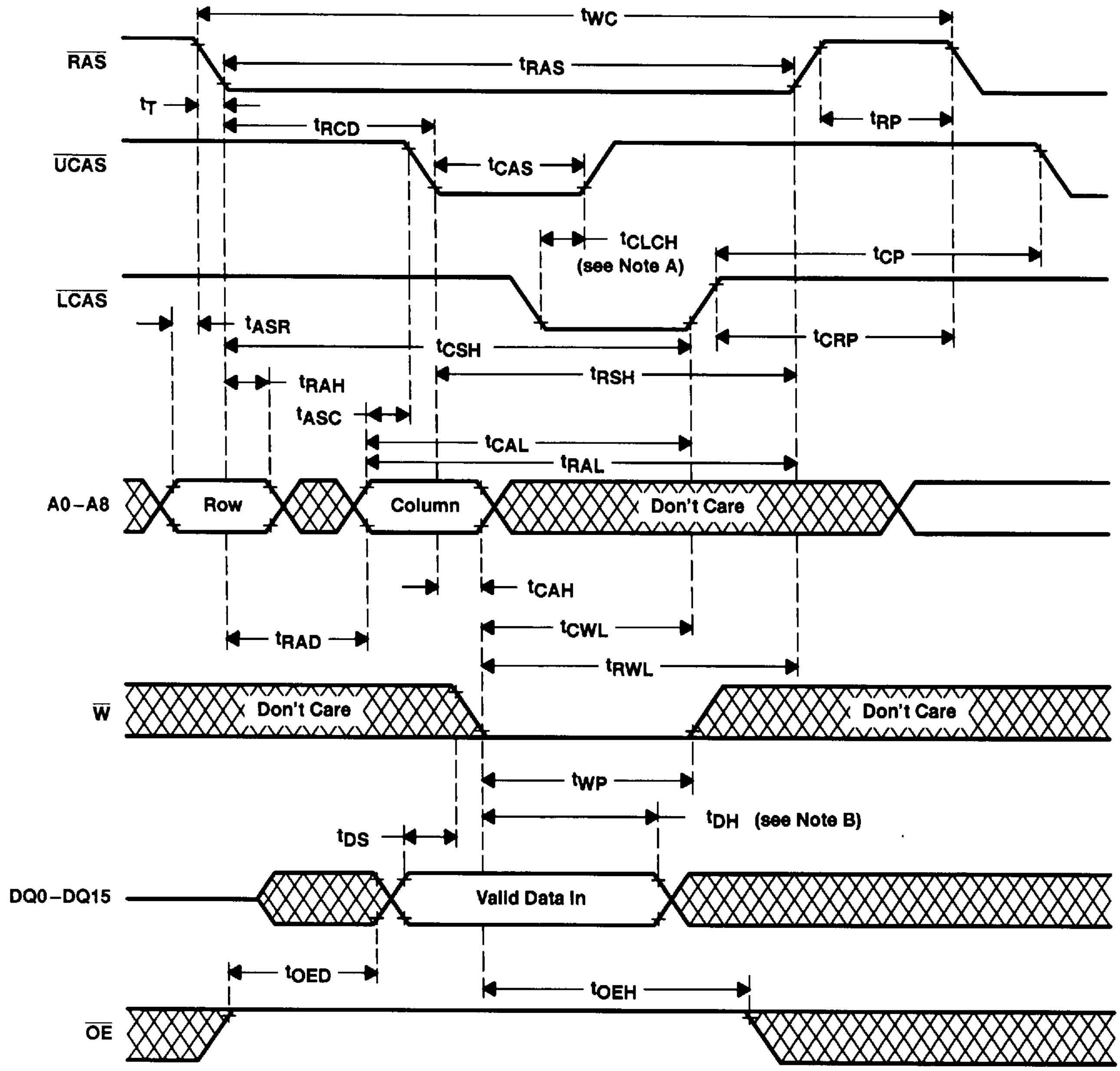
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
D. $\overline{xCAS}$ order is arbitrary.

Figure 2. Read-Cycle Timing

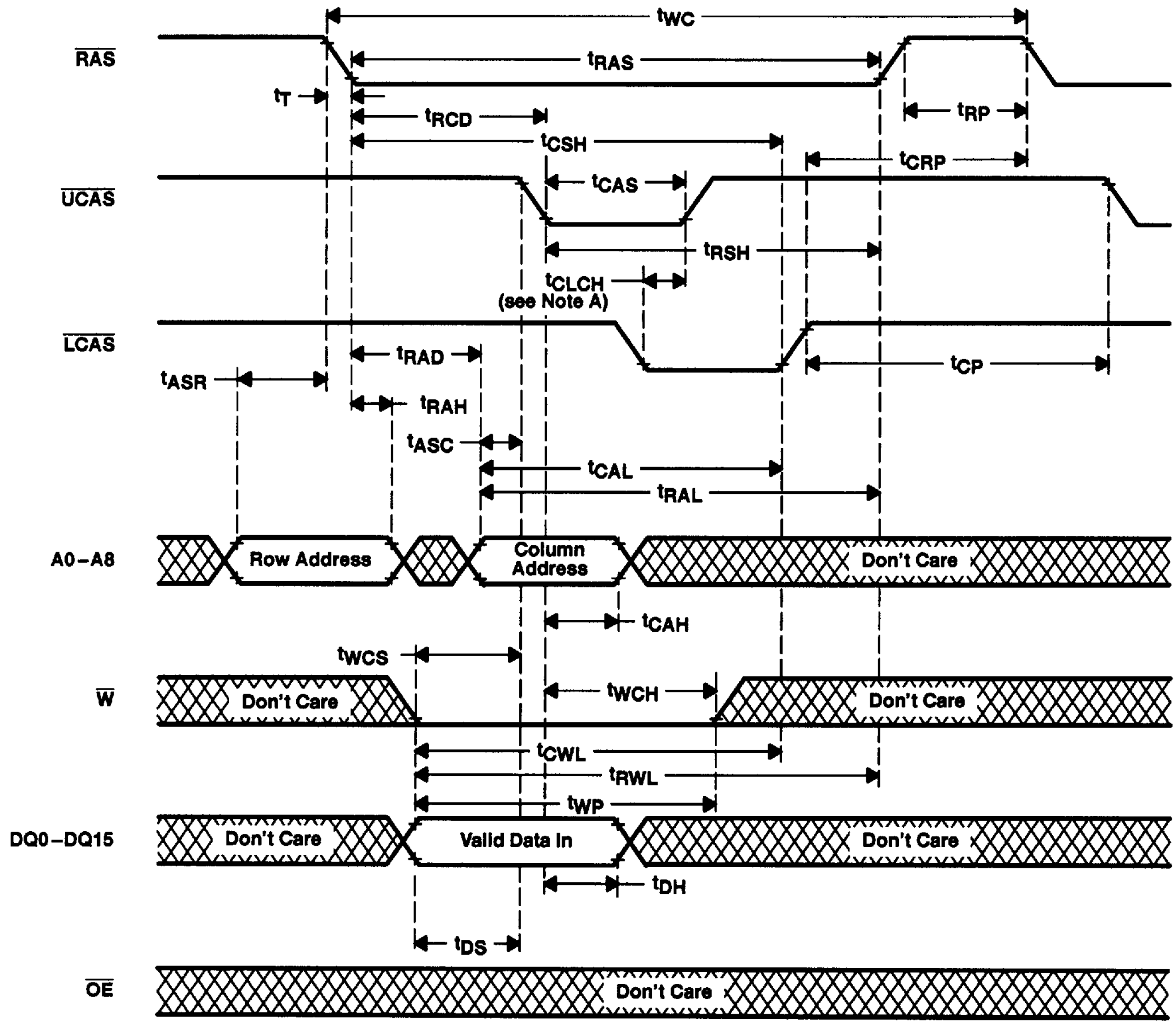
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Later of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ in write operations
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

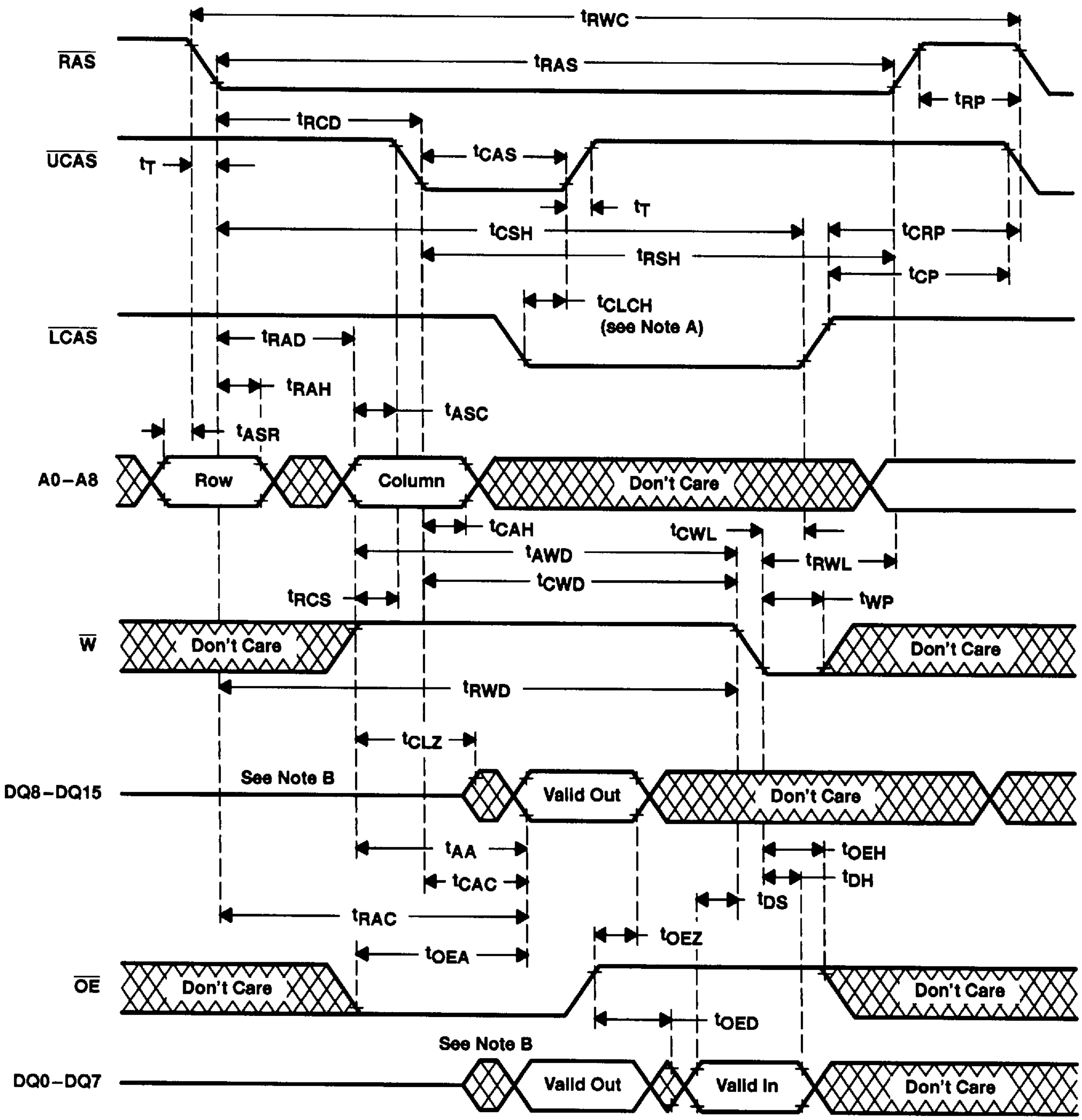


NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

8961725 0086746 853

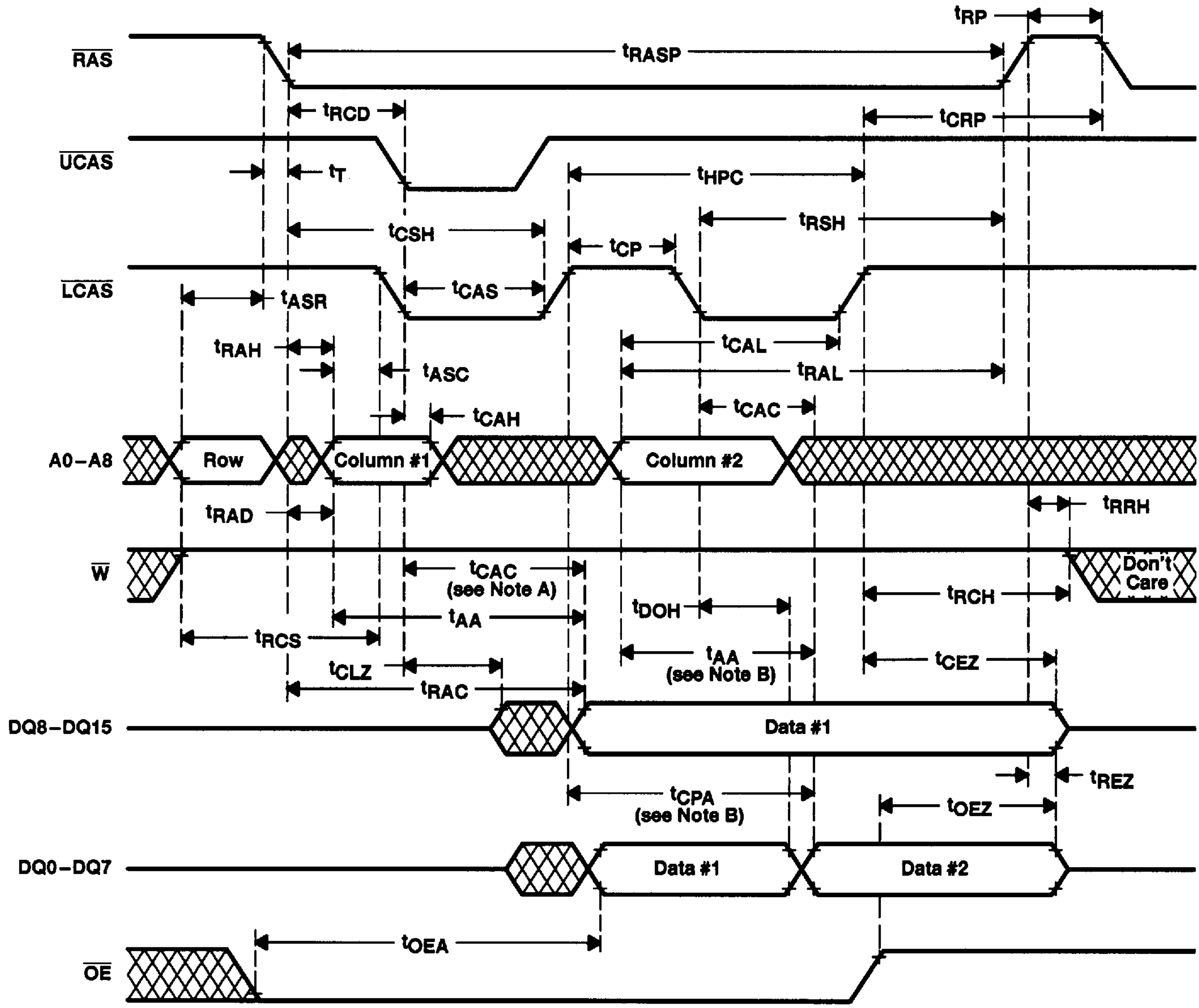
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. $\overline{xCAS}$ order is arbitrary.
D. Later of $\overline{xCAS}$ or $\overline{W}$ in write operations

Figure 5. Read-Modify-Write-Cycle Timing

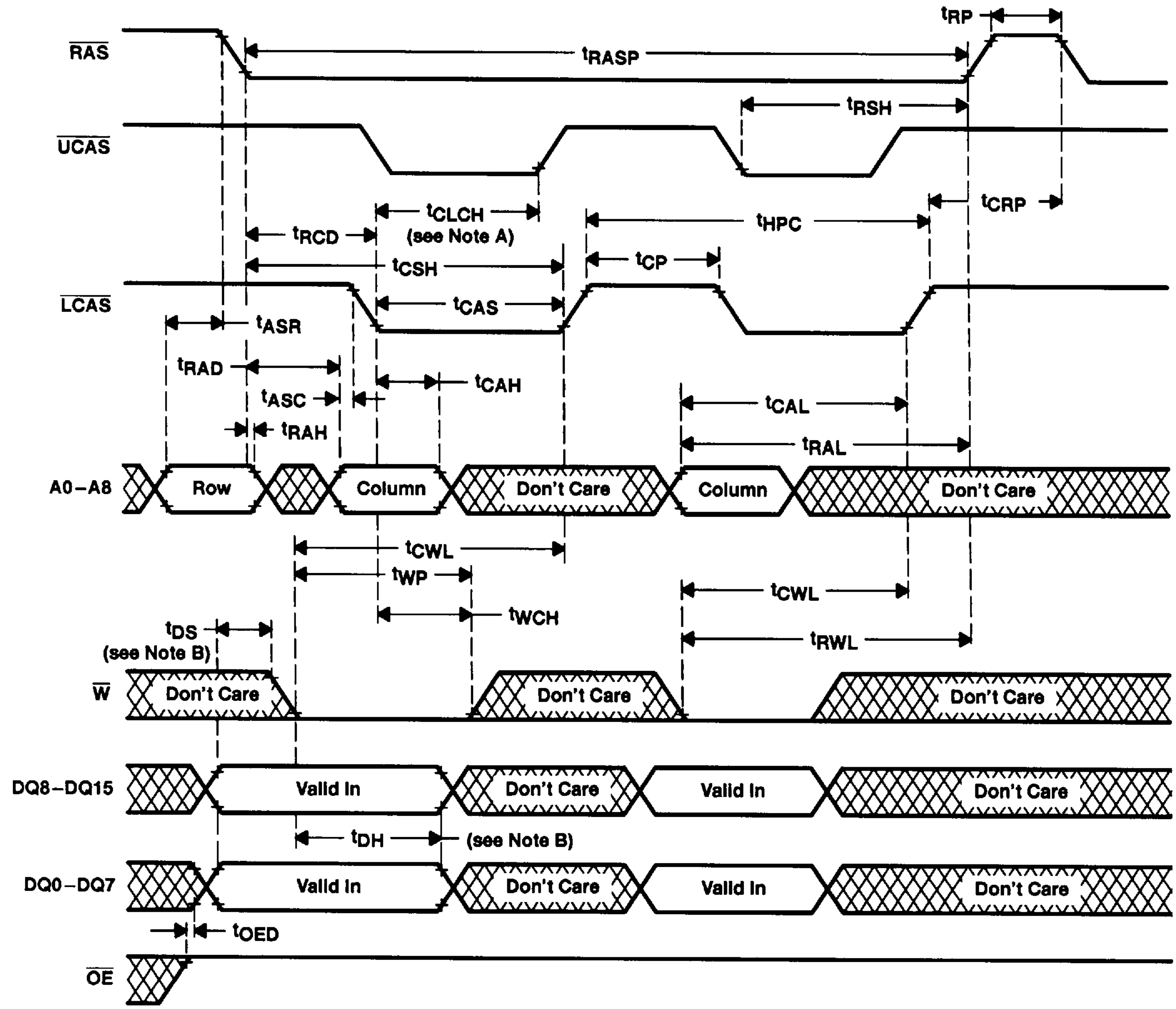
PARAMETER MEASUREMENT INFORMATION



NOTES: A. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.
E. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. EDO Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. EDO Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

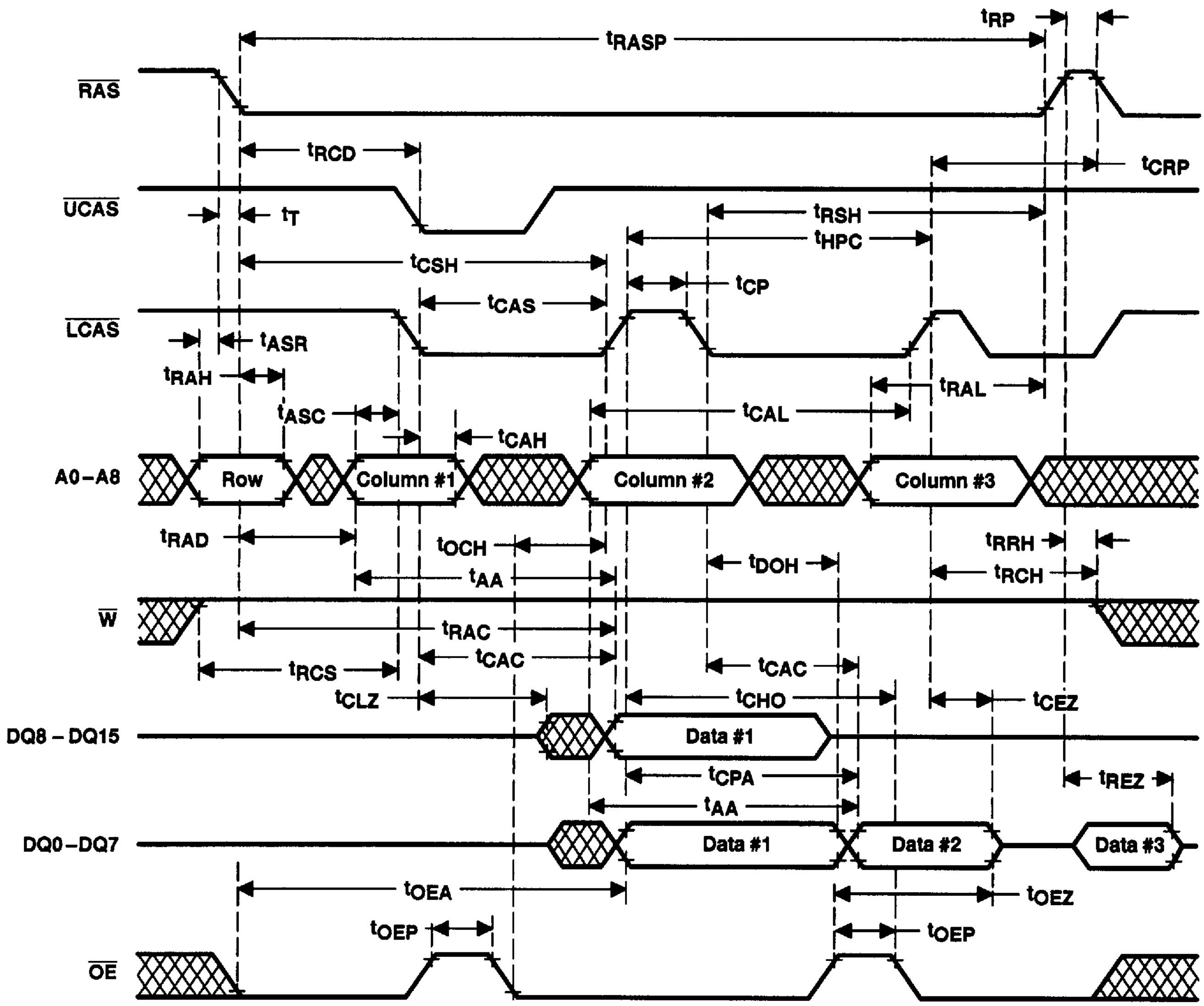


Figure 8. EDO Read-Cycle With $\overline{OE}$ Control

PARAMETER MEASUREMENT INFORMATION

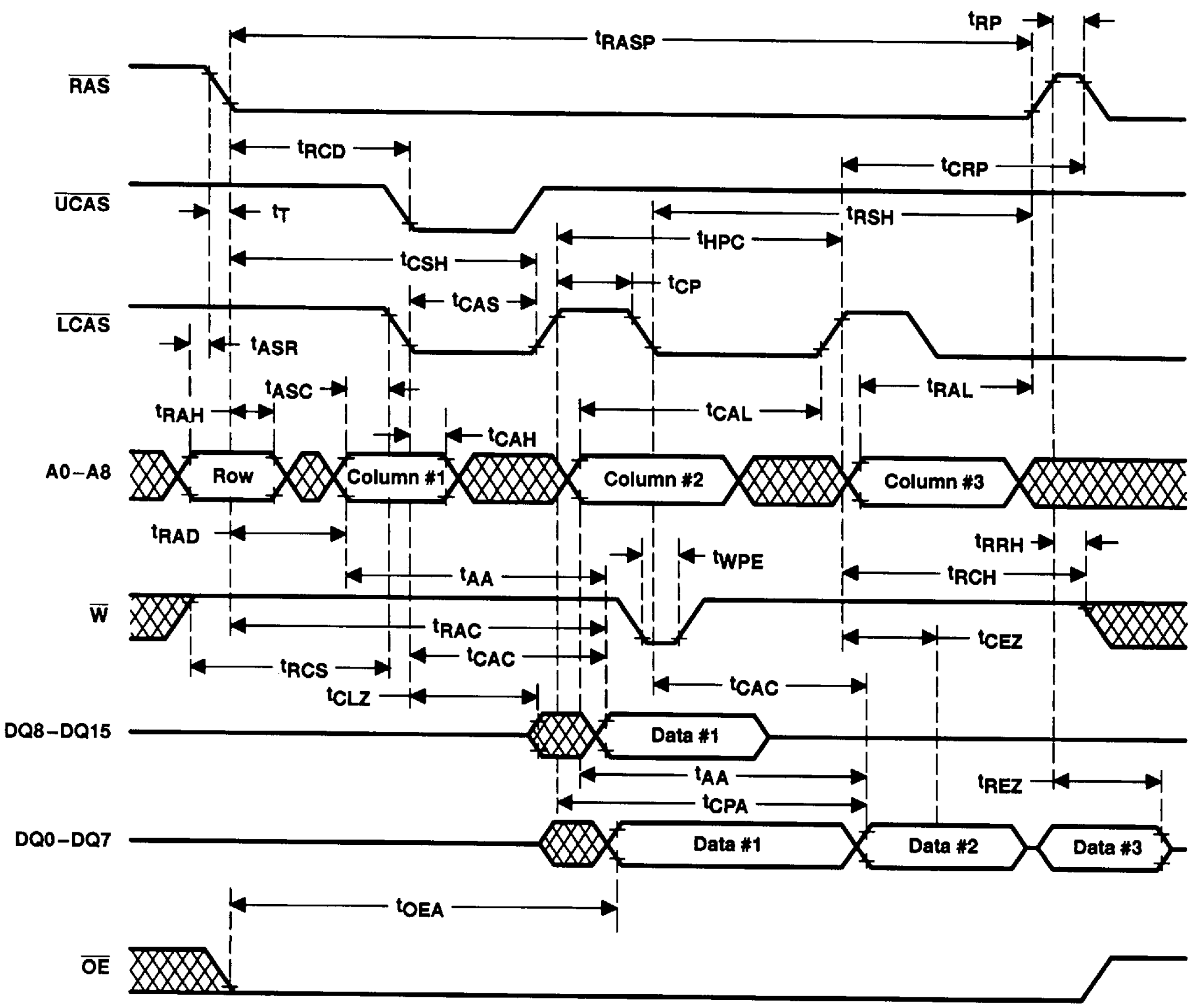
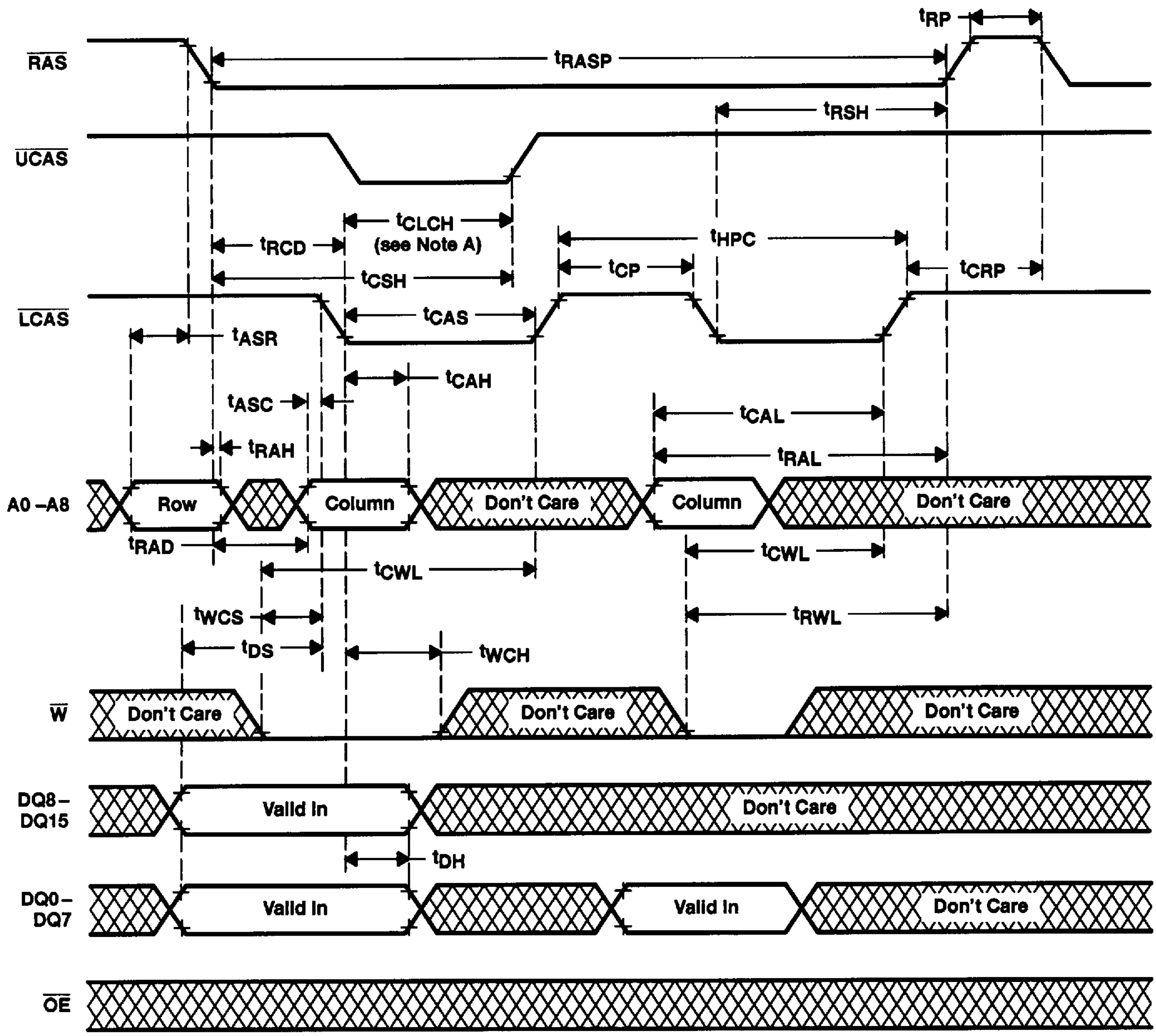


Figure 9. EDO Read-Cycle With $\overline{W}$ Control

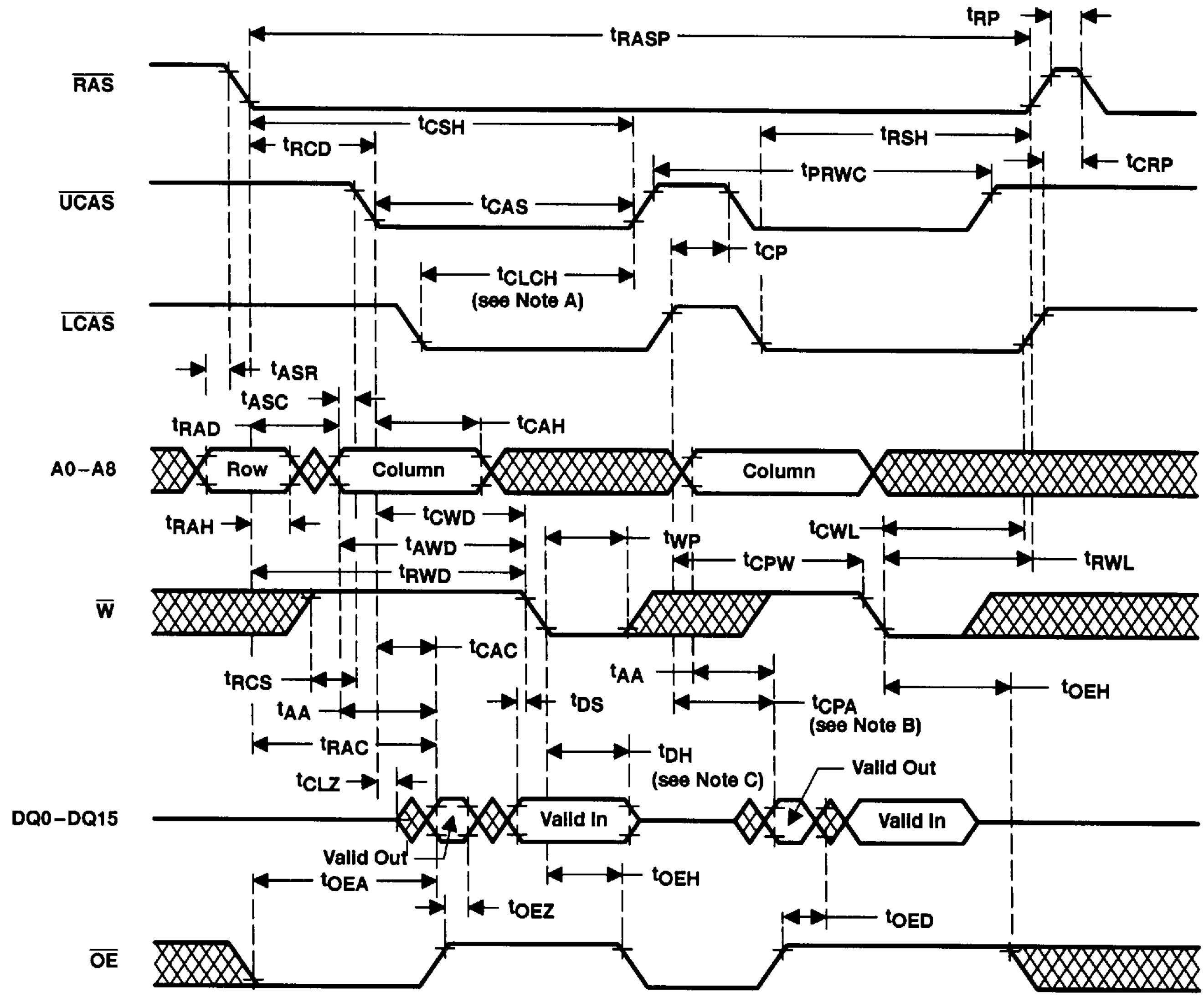
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 10. EDO Early Write-Cycle Timing

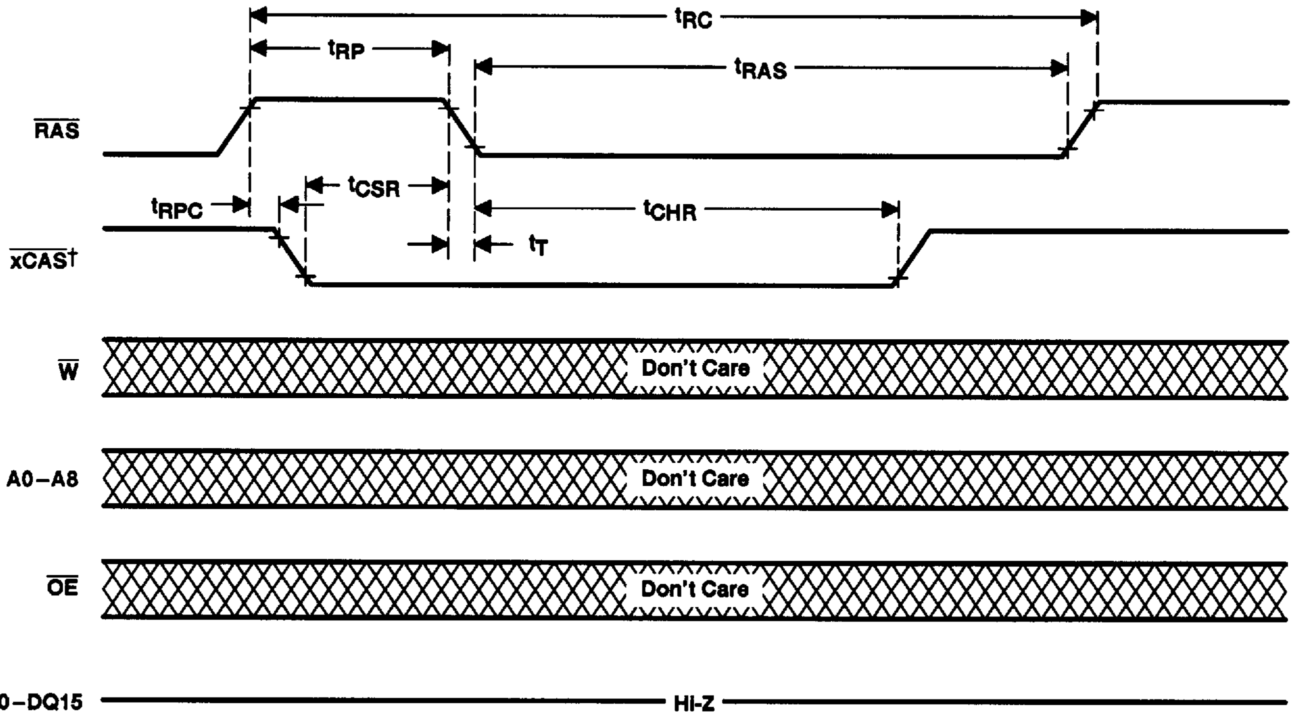
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{xCAS}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.

Figure 11. EDO Read-Modify-Write-Cycle Timing

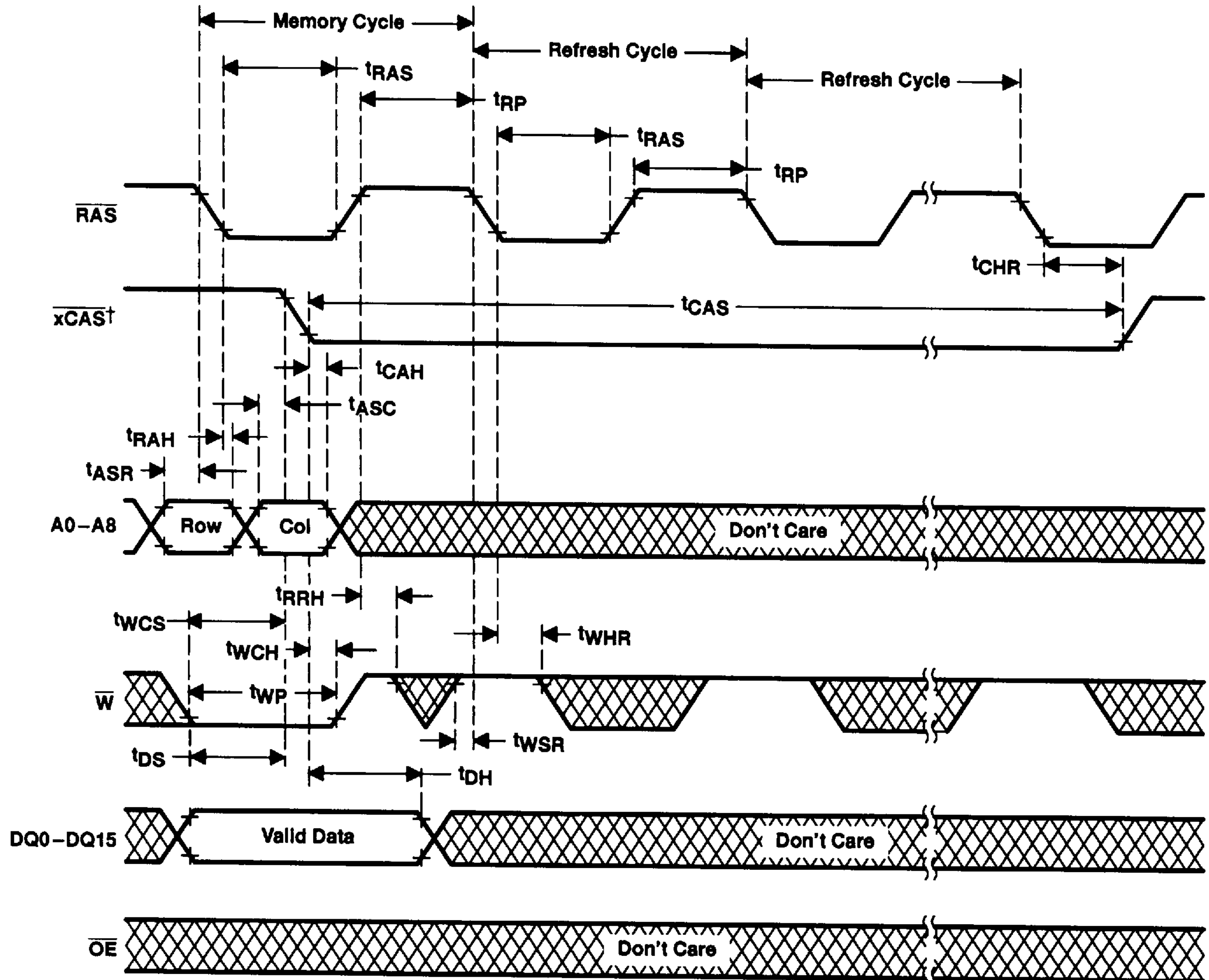
PARAMETER MEASUREMENT INFORMATION



† xCAS includes UCAS and LCAS.

Figure 12. Automatic CBR-Refresh-Cycle Timing

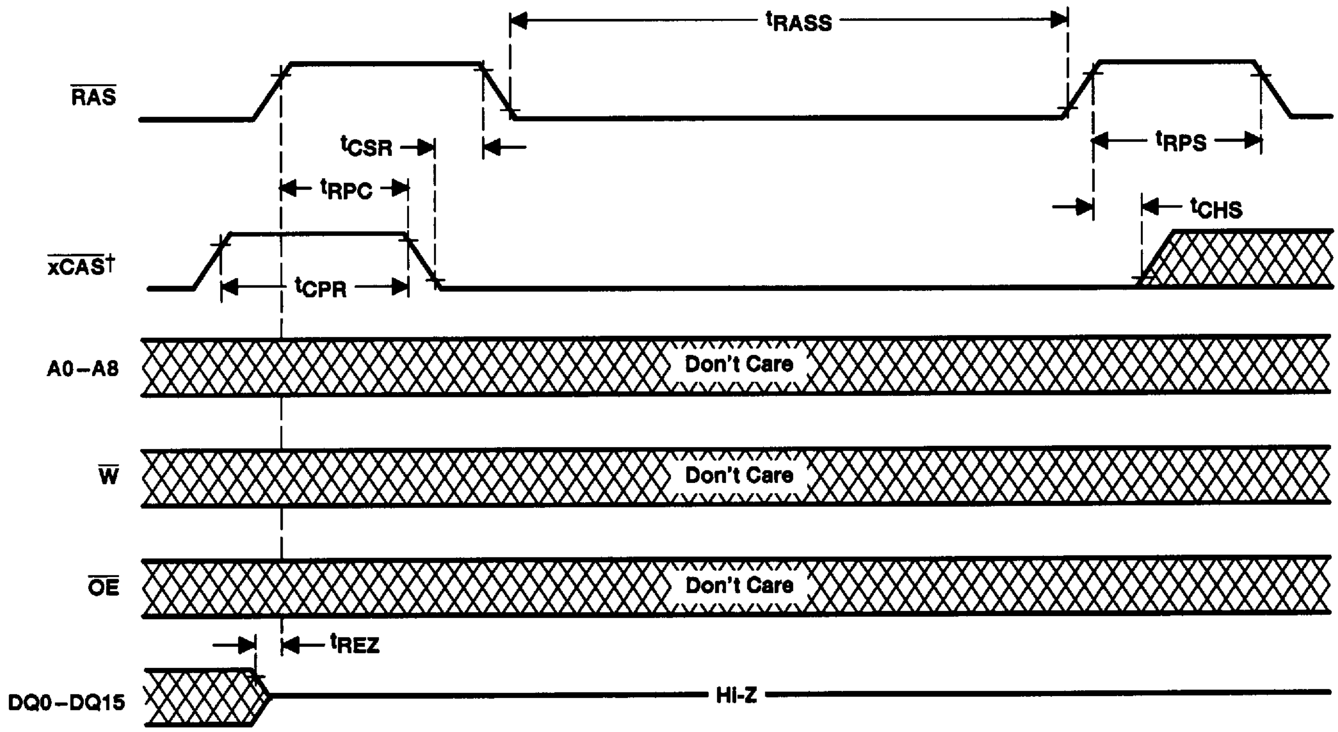
PARAMETER MEASUREMENT INFORMATION



† xCAS includes UCAS and LCAS.

Figure 13. Hidden-Refresh Cycle (Write)

PARAMETER MEASUREMENT INFORMATION

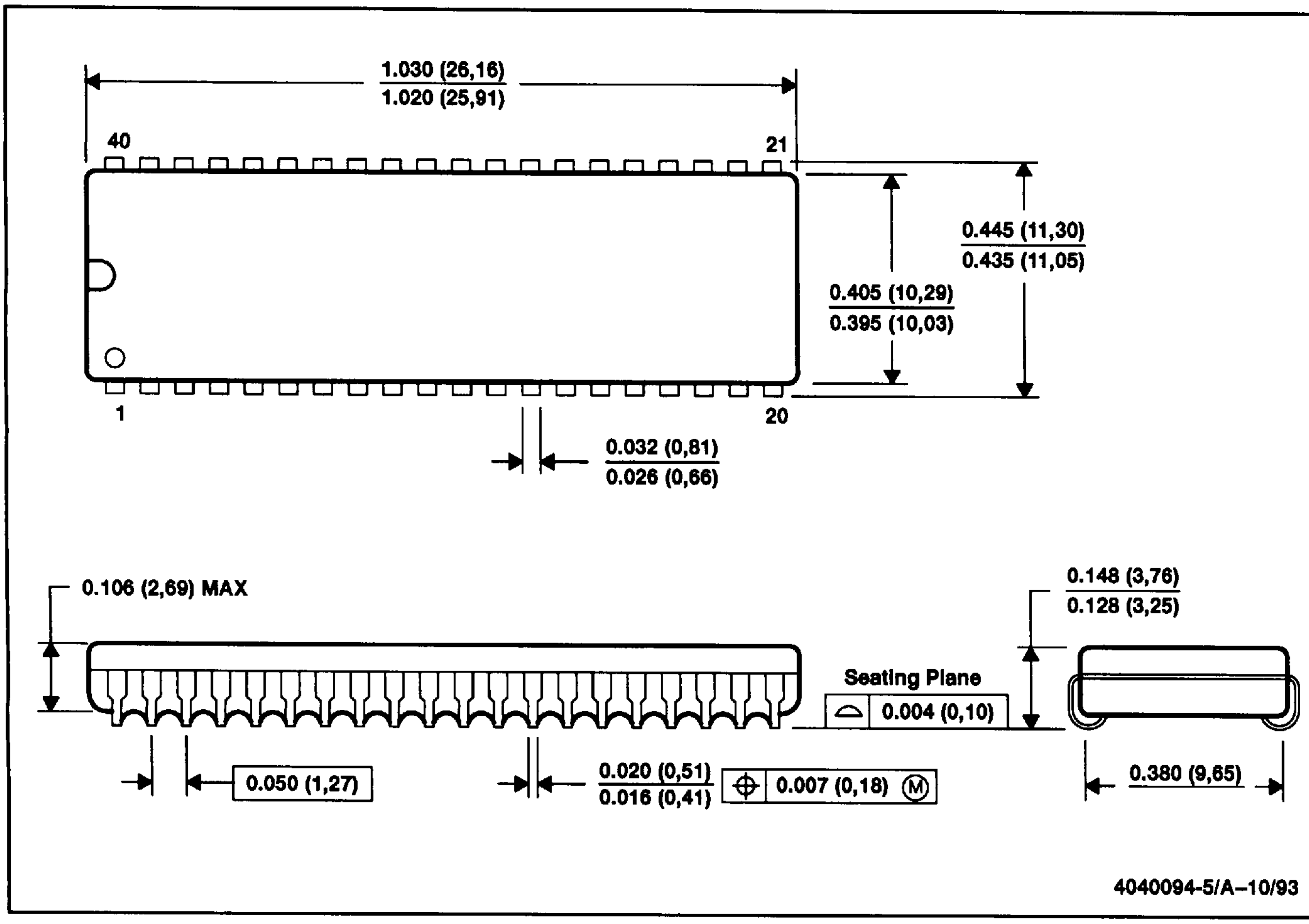


† xCAS includes UCAS and LCAS.

Figure 14. Self-Refresh Timing

MECHANICAL DATA

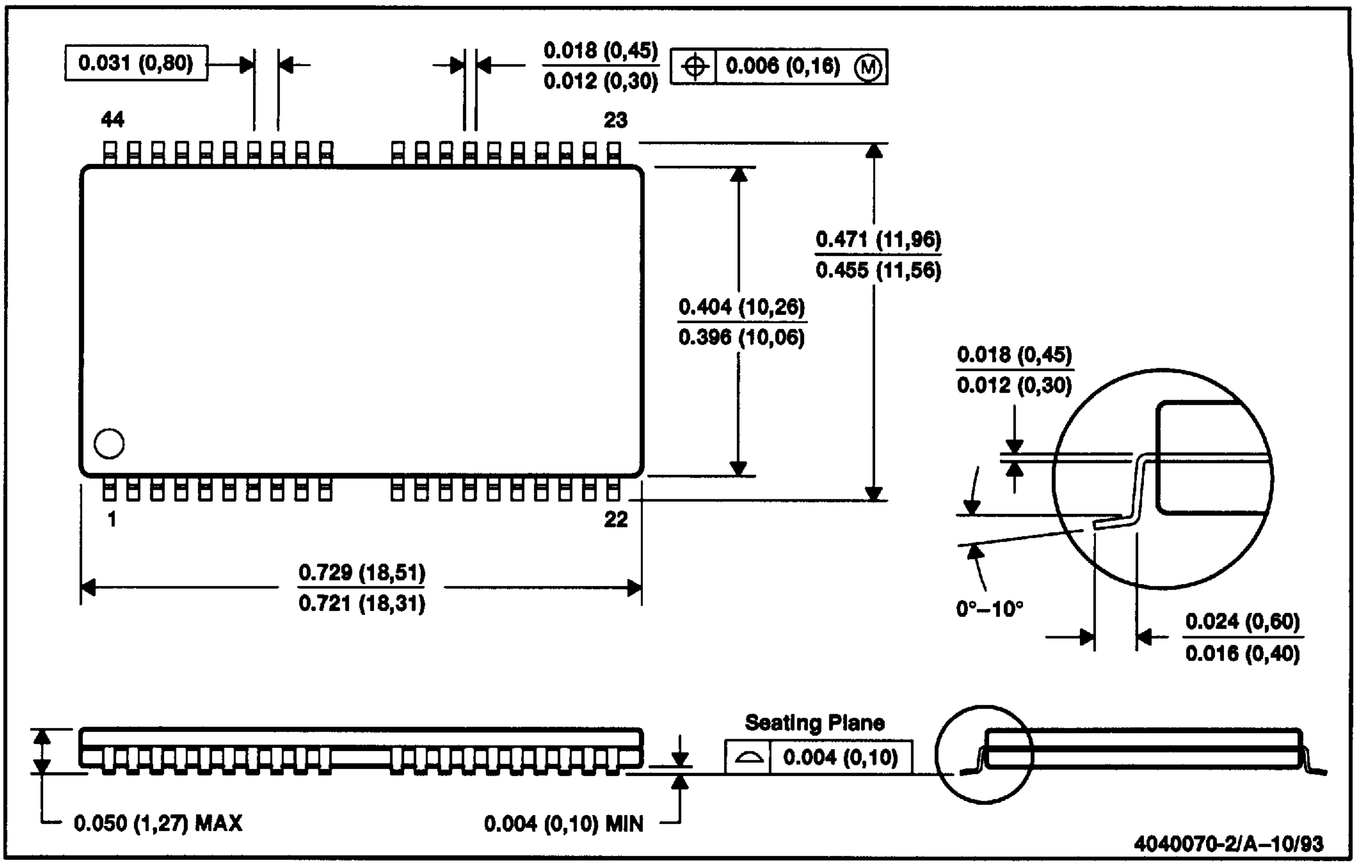
DZ/R-PDSO-J40 **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

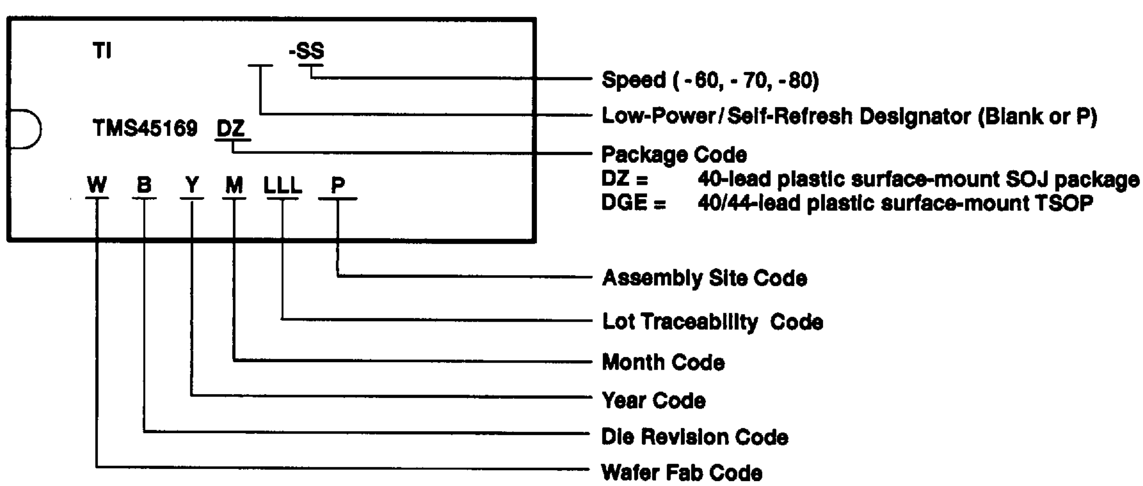
MECHANICAL DATA

DGE/ R-PDSO-G40/44 **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

device symbolization (TMS45169 illustrated)



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