bq28300 INTEGRATED GAS GAUGE and BATTERY PROTECTION MANAGEMENT with SBS

Check for Samples: bq28300

FEATURES

- **Fully Integrated Gas Gauge and Analog Monitoring with Protection in Single Package**
- **Supports 2 or 3 Series Li-Ion or Li-Polymer Cells**
- **Pre-Programmed with Easy User Setup**
- **Integrated Pre-Charge Mode**
- **Complete Set of Protection:**
  - **OV (Overvoltage)**
  - **UV (Undervoltage)**
  - **SC (Short Circuit)**
  - **OT (Overtemperature)**
  - **CIM (Cell Imbalance)**
- **Accurate CEDV Gauging Algorithm with Self Discharge Compensation**
- **High Accuracy Analog Interface with Two Independent ADCs:**
  - **High Resolution 16 bit Integrator for Coulomb Counting**
  - **15 bit Delta-Sigma ADC with 16 Channel Multiplexer for Voltage, Current, and Temperature**
- **P-Channel High Side Protection FET Drive**
- **Fully Integrated Internal Clock Synthesizer with no External Components Required**
- **Integrated Single Write Memory for User Settings**
- **Two-Wire SMBus v1.1 Communications**
- **Reduced Power Modes (Typical Battery Pack Operating Range Conditions)**
  - **Low Power: < 180 µA**
  - **Sleep: < 80 µA**
- **20-Pin TSSOP Package (RoHS Compliant)**

APPLICATIONS

- **Notebook and Netbook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The Texas Instruments bq28300 is a fully integrated gas gauge and analog monitoring management solution that provides protection and control for 2 or 3 series cell Li-Ion battery packs in a small single TSSOP package.

Implementing the optimum balance of quick response analog hardware based monitoring and control along with an integrated fast pre-programmed intelligent CPU, provides the ideal pack-based or in-system Li-Ion battery solution. The bq28300 also provides flexible user programmable settings stored in a non-volatile single write memory for control of critical system parameters such as over current, short circuit, under/overvoltage, and over/undertemperature conditions.

The bq28300 communicates with the system host via a 2 wire SMBus 1.1 compatible interface providing high accuracy reporting and control of battery pack operation.

The P-channel FET drive and small TSSOP package, allows a lower cost and small footprint solution along with simple layout and routing on narrow pack PCBs.

PRODUCT PREVIEW

AVAILABLE OPTIONS

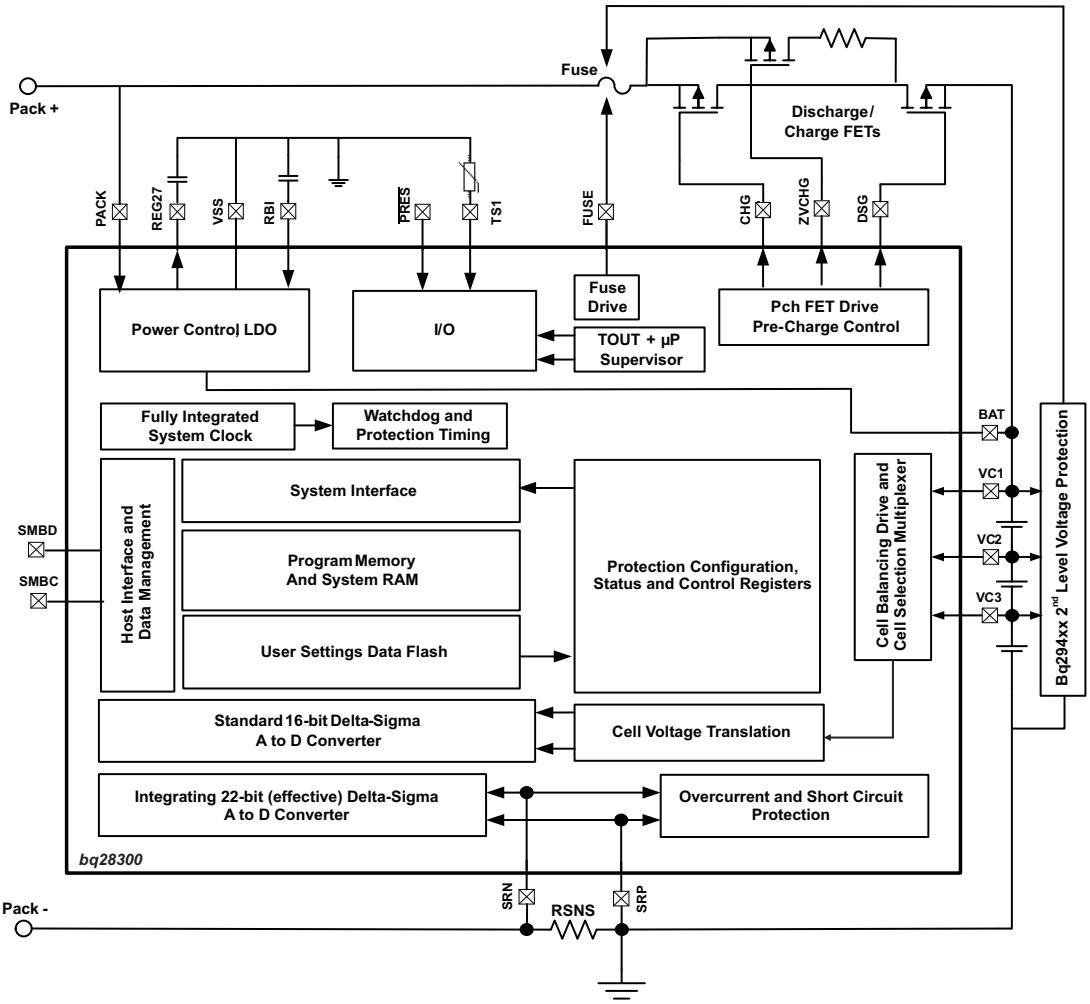
T_A	PACKAGE(1)	
	20-PIN TSSOP (PW) Tube	20-PIN TSSOP (PW) Tape and Reel
–40°C to 85°C	bq28300PW(2)	bq28300PWR(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) A single tube quantity is 50 units.
(3) A single reel quantity is 2000 units

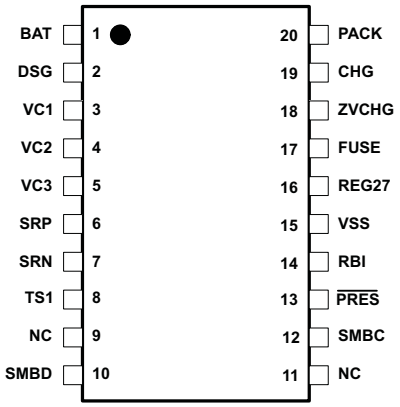
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM and TYPICAL IMPLEMENTATION



bq28300
PW PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

PIN FUNCTIONS

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
BAT	1	P	Alternate supply input
DSG	2	O	P-channel discharge FET gate drive
VC1	3	AI	Sense voltage input terminal for most positive cell and external cell balancing drive output for most positive cell
VC2	4	AI	Sense voltage input terminal for second most positive cell and external cell balancing drive output for second most positive cell.
VC3	5	AI	Sense voltage input terminal for least positive cell and external cell balancing drive output for least positive cell
SRP	6	AI	Differential Coulomb counter input or SRP oversampled ADC input
SRN	7	AI	Differential Coulomb counter input or SRN oversampled ADC input
TS1	8	I	Thermistor 1 input
NC	9	-	No Connection – leave floating
SMBD	10	I/OD	SBS data
NC	11	-	No Connection
SMBC	12	I/OD	SBS clock
$\overline{PRES}$	13	I	System Present
RBI	14	P	RAM backup pin to provide backup potential to the internal DATA RAM if power is momentarily lost, by using a capacitor attached between RBI and VSS.
VSS	15	P	Device ground
REG27	16	P	2.7V regulator. Connect a capacitor between REG27 and VSS
FUSE	17	O	Push-pull fuse circuit drive
ZVCHG	18	O	P-channel precharge FET gate drive
CHG	19	O	P-channel charge FET gate drive
PACK	20	P	Alternate supply input

THERMAL INFORMATION

THERMAL METRIC(1)		bq28300 PW 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	91.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	20.4	
θ_{JB}	Junction-to-board thermal resistance (4)	45.6	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter (6)	43.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

		Value/Unit
Supply voltage range, V_{MAX}	PACK w.r.t. V_{SS}	-0.3 to 34V
Input voltage range, V_{IN}	VC1, BAT	V_{VC2} -0.3 to V_{VC2} +8.5 or 34V which ever is lower
	VC2	V_{VC3} -0.3 to V_{VC3} +8.5V
	VC3	V_{SRP} -0.3 to V_{SRP} +8.5V
	SRP, SRN	–0.3 to V_{REG27}
	General Purpose open-drain I/O pins: SMBD, SMBC	V_{SS} –0.3 V to 6 V
	General Purpose push-pull I/O pins: TS1, $\overline{PRES}$	–0.3 V to V_{REG27} + 0.3 V
	Input voltage range to all other pins, V_{IN} relative to V_{SS}, $\overline{XRST}$	–0.3 V to V_{REG27} + 0.3 V
	DSG, CHG, ZVCHG	-0.3 to BAT
	FUSE	–0.3 to [BAT or PACK] (whichever is lower)
	RBI, REG27	-0.3 to 2.75V
Maximum VSS current, I_{SS}		50mA
Ambient Temperature, T_A		–20 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
	Supply voltage	PACK			V_{BAT} + 5	V
		BAT	3.8		V_{VC2} + 5	
$V_{(STARTUP)}$	Minimum startup voltage	Start up voltage at PACK		5.2	5.5	V
V_{IN}	Input Voltage Range	VC!, BAT	V_{VC2}		V_{VC2} + 5	V
		VC2	V_{VC3}		V_{VC3} + 5	V
		VC3	V_{SRP}		V_{SRP} + 5	V
		VCn – VC(n + 1), (n = 1, 2, 3)	0		5	V
		PACK			18.75	V
		SRP to SRN	-0.3		1	V
$C_{(REG27)}$	External 2.7V REG capacitor		1			µF
T_{OPR}	Operating temperature		-20		85	°C

ESD CHARACTERISTICS

T_A = 25°C, V_{BAT} = V_{PACK} = 3.8V to 18.75V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESD	Electrostatic discharge, SMBD, SMBC, $\overline{PRES}$	Contact discharge (1)			12	KV
		Air discharge			15	

(1) This value is based on Texas Instruments evaluation module design and is application circuit dependent. Results may vary based on the end application design.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Typical values stated where T_A = 25ºC and V_{BAT} = V_{PACK} = 10.8V, Min/Max values stated where T_A = -20ºC to 85ºC and V_{BAT} = V_{PACK} = 3.8V to 18.75V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION(1)	MIN	TYP	MAX	UNIT
General Purpose I/O						
V_{IH}	High-level input voltage	SMBD, SMBC, $\overline{PRES}$, TS1	2			V
V_{IL}	Low-level input voltage	SMBD, SMBC, $\overline{PRES}$, TS1			0.8	V
V_{OH}	Output voltage high	SMBD, SMBC, $\overline{PRES}$, TS1, I_L = –0.5 mA	V_{REG27}– 0.5			V
$V_{OH(FUSE)}$	High level Fuse output	V_{BAT} = 3.8V to 9V, C_L = 1nF	3	V_{BAT}- 0.3	8.6	V
		V_{BAT} = 9V to 18.75V, C_L = 1nF	7.5	8	9	
$t_{R(FUSE)}$	FUSE output rise time	C_L = 1nF, $V_{OH(FUSE)}$ = 0V to 5V			10	µs
$I_{O(FUSE)}$	FUSE output current	FUSE active	–3			mA
$Z_{O(FUSE)}$	FUSE output impedance			2	6	KΩ
V_{FUSE_DET}	FUSE Detect Input Voltage		0.8	2	3.2	V
V_{OL}	Low-level output voltage	SMBD, SMBC, $\overline{PRES}$, TS1, I_L = 7mA			0.4	V
C_{IN}	Input capacitance			5		pF
$I_{(VOUT)}$	VOUT source currents	V_O active, V_O = V_{REG27} – 0.6V	–3			mA
$I_{LKG(VOUT)}$	VOUT leakage current	V_O inactive	–0.2		0.2	µA
I_{LKG}	Input leakage current	SMBD, SMBC, $\overline{PRES}$, TS1			1	µA
$R_{PD(SMBx)}$	SMBD and SMBC, Pull-Down resistor	T_A = -20°C to 100°C	600	950	1300	KΩ
R_{PAD}	Pad resistance	TS1		87	110	Ω
Supply Current						
I_{CC}	Normal Mode	No memory write, No I/O activity		1		mA
I_{SLEEP}	Sleep Mode	CPU=HALT CHG=DSG=PCHG=OFF LDO ON but no load, No communication		69		µA
$I_{SHUTDOWN}$	Shutdown Mode	T_A = -20°C to 110°C		0.5	1	µA
REG27 Power On Reset						
$V_{REG27IT-}$	Negative-going voltage input, At REG27		2.22	2.35	2.34	V
$V_{REG27IT+}$	Positive-going voltage input, At REG27		2.25	2.5	2.6	V
RAM Backup						
$I_{(RBI)}$	RBI data-retention input current	V_{RBI} > $V_{(RBI)MIN}$, V_{REG27} < $V_{REG27IT-}$, T_A = 70°C to 110°C		20	1500	nA
		V_{RBI} > $V_{(RBI)MIN}$, V_{REG27} < $V_{REG27IT-}$, T_A = -20°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage (2)		1			V
Internal LDO						
V_{REG}	Regulator output voltage	I_{REG27} = 10mA, T_A = –20°C to 85°C	2.5	2.7	2.75	V
I_{REG}	Regulator Output Current	PACK and BAT ≤ 4.5 V, T_A = –20°C to 110°C	3			mA
		4.5 V < PACK and BAT ≤ 6.8 V	10			
		6.8 V < PACK and BAT ≤ 18.75V, T_A = –20°C to 70°C	16			
$\Delta V_{(REGTEMP)}$	Regulator output change with temperature	I_{REG} = 10mA, T_A = –20°C to 85°C		±0. 5%		
$\Delta V_{(REGLINE)}$	Line regulation	I_{REG} = 10mA		±2	±4	mV
$\Delta V_{(REGLOAD)}$	Load regulation	I_{REG} = 0.2 to 10mA		±20	±40	mV
$I_{(REGMAX)}$	Current limit		25		50	mA

(1) By default SMBus has internal pull-down.
(2) Specified by design. Not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

Typical values stated where T_A = 25ºC and V_{BAT} = V_{PACK} = 10.8V, Min/Max values stated where T_A = -20ºC to 85ºC and V_{BAT} = V_{PACK} = 3.8V to 18.75V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION(1)	MIN	TYP	MAX	UNIT
SRx Wake from Sleep						
V_{WAKE_ACR}	Accuracy of V_{WAKE}	V_{WAKE} = 1.2mV	0.2	1.2	2	mV
		V_{WAKE} = 2.4mV	0.4	2.4	3.6	
		V_{WAKE} = 5mV	2	5	6.8	
		V_{WAKE} = 10mV	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of V_{WAKE} accuracy			0.5		%/°C
t_{WAKE}	Time from application of current and wake of bq28300			0.2	1	ms
Coulomb Counter						
	Input voltage range		-0.20		0.25	V
	Conversion time	Single conversion		250		ms
	Effective resolution	Single conversion	15			Bits
	Integral nonlinearity	T_A = -20 to 85°C		±0.007	±0.034	%FSR
	Offset error (3)	T_A = -20 to 85°C		10		µV
	Offset error drift			0.3	0.5	µV/°C
	Full-scale error (4)		-0.8%	0.2%	0.8%	
	Full-scale error drift				150	PPM/°C
	Effective input resistance		2.5			MΩ
ADC						
	Input voltage range		–0.2		0.8 x V_{REG27}	V
	Conversion time			31.5		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution			15		Bits
	Integral nonlinearity	–0.1 V to 0.8 x V_{ref}			±0.020	%FSR
	Offset error (5)			70	160	µV
	Offset error drift			25		µV/°C
	Full-scale error	V_{IN} = 1V	-0.8%	±0.2%	0.4%	
	Full –scale error drift				150	PPM/°C
	Effective input resistance		8			MΩ
External Cell Balance Drive						
R_{BAL_drive}	Internal pull-down resistance for external cell balance	Cell balance ON for VC1, VCi - VCi + 4V, where I = 1 to 3		3.7		kΩ
		Cell balance ON for VC2, VCi - VCi + 4V, where I = 1 to 3		1.75		
		Cell balance ON for VC3, VCi - VCi + 4V, where I = 1 to 3		0.85		
Cell Voltage Monitor						
	CELL Voltage Measurement Accuracy	T_A = -10ºC to 60ºC		±10	±20	mV
		T_A = -20ºC to 85ºC		±10	±35	

(3) Post Calibration Performance
(4) Uncalibrated performance. This gain error can be eliminated with external calibration.
(5) Chanel to Chanel Offset

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

Typical values stated where T_A = 25ºC and V_{BAT} = V_{PACK} = 10.8V, Min/Max values stated where T_A = -20ºC to 85ºC and V_{BAT} = V_{PACK} = 3.8V to 18.75V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION(1)		MIN	TYP	MAX	UNIT
Internal Temperature Sensor							
T_{INT}	Temperature sensor accuracy				±3%		°C
Thermistor Measurement Support							
R_{ERR}	Internal resistor drift				±230		PPM/°C
R	Internal resistor				18	20	KΩ
Internal Thermal Shutdown							
T_{MAX}	Maximum REG27 temperature (6)			125		175	°C
$T_{RECOVER}$	Recovery hysteresis temperature (6)				10		°C
Current Protection Thresholds							
$V_{(OCD)}$	OCD detection threshold voltage range, typical			50		200	mV
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step				10		mV
$V_{(SCCT)}$	SCC detection threshold voltage range, typical			-100		-300	mV
$\Delta V_{(SCCT)}$	SCC detection threshold voltage program step				-50		mV
$V_{(SCDT)}$	SCD detection threshold voltage range, typical			100		450	mV
$\Delta V_{(SCDT)}$	SCD detection threshold voltage program step				50		mV
$V_{(OFFSET)}$	SCD, SCC, and OCD offset			-10		10	mV
$V_{(Scale\_Err)}$	SCD, SCC, and OCD scale error			-10%		10%	
Current Protection Timing							
$t_{(OCDD)}$	Overcurrent in discharge delay			1		31	ms
$t_{(OCDD\_STEP)}$	OCDD Step options				2		ms
$t_{(SCDD)}$	Short circuit in discharge delay			0		1830	µs
$t_{(SCDD\_STEP)}$	SCDD Step options				122		µs
$t_{(SCCD)}$	Short circuit in charge delay			0		915	µs
$t_{(SCCD\_STEP)}$	SCCD Step options				61		µs
$t_{(DETECT)}$	Current fault detect time	$V_{SRP-SRN}$ = V_{THRESH} + 12.5mV, T_A = -20˚C to 85˚C			35	160	µs
t_{ACC}	Overcurrent and short circuit delay time accuracy	Accuracy of typical delay time with no WDI input		-50%		50%	
P-Ch FET Drive							
$V_{O(FETON)}$	Output voltage, charge and discharge FETs on	$V_{O(FETONDSG)}$ = $V_{(BAT)}$ - $V_{(DSG)}$, R_{GS} = 1MΩ, T_A = –20 to 110°C, BAT = 15V (7)		9	11.25	13.5	V
		$V_{O(FETONCHG)}$ = $V_{(PACK)}$ - $V_{(CHG)}$, R_{GS} = 1MΩ, T_A = –20 to 110°C, PACK = 15V(7)		9	11.25	13.5	V
$V_{O(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{O(FETOFFDSG)}$ = $V_{(BAT)}$ - $V_{(DSG)}$, T_A = –20°C to 110°C, BAT = 12V				0.2	V
		$V_{O(FETOFFCHG)}$ = $V_{(PACK)}$ - $V_{(CHG)}$, T_A = –20°C to 110°C, PACK = 12V				0.2	V
t_r	Rise time	C_L = 4700 pF	VDSG: 10% to 90%		40	200	µs
			VCHG: 10% to 90%		40	200	
t_f	Fall time	C_L = 4700 pF	VDSG : 90% to 10%		40	200	
			VCHG: 90% to 10%		40	200	

(6) Specified by Design. Not production tested.
(7) For a V_{BAT} or V_{PACK} input range of 3.8V to 18.75V, MIN $V_{O(FETON)}$ voltage is 9V or V(BAT) - 1V, whichever is less.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

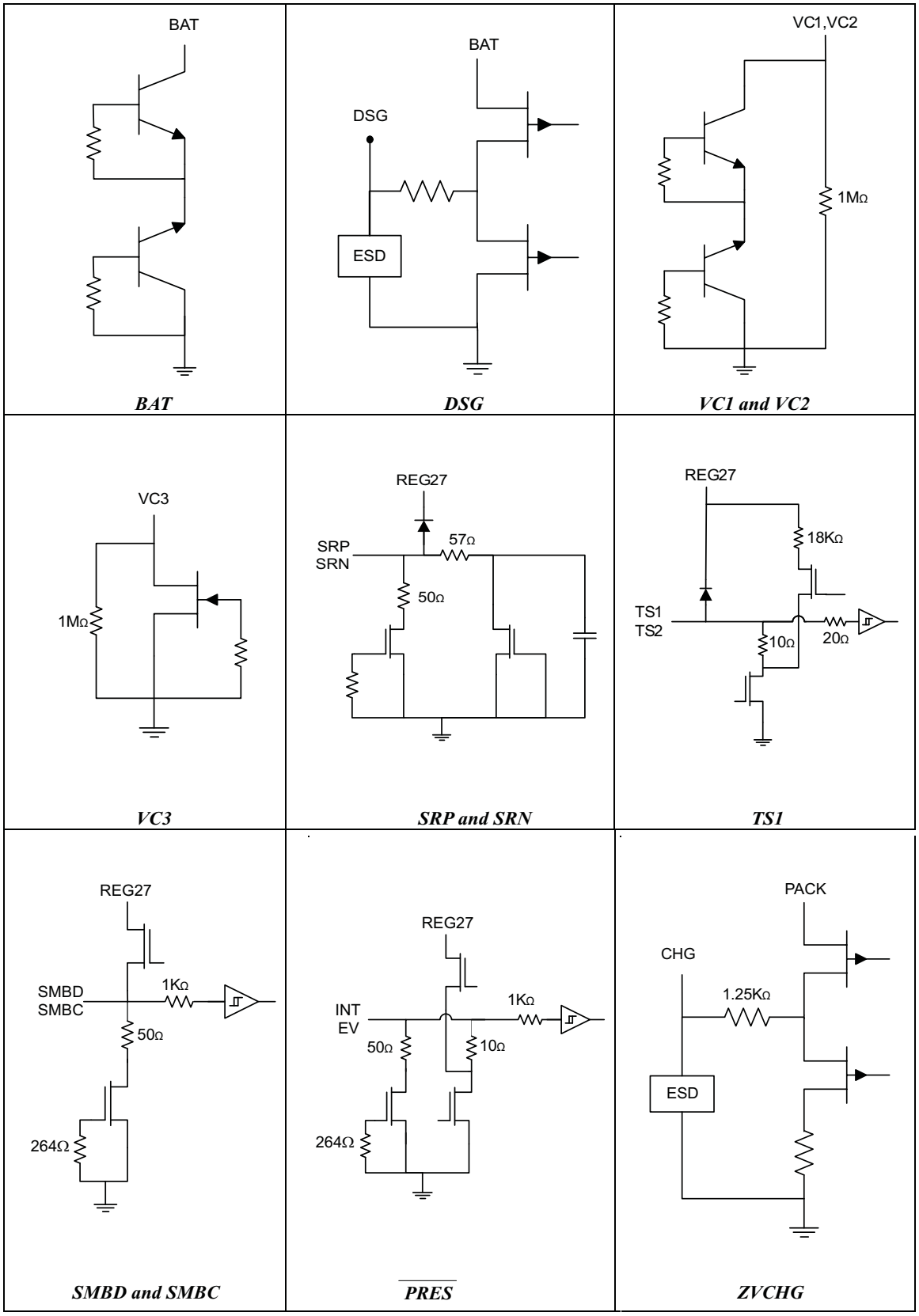
Typical values stated where T_A = 25ºC and V_{BAT} = V_{PACK} = 10.8V, Min/Max values stated where T_A = -20ºC to 85ºC and V_{BAT} = V_{PACK} = 3.8V to 18.75V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION(1)		MIN	TYP	MAX	UNIT
Pre-Charge/ZVCHG FET Drive							
$V_{(PreCHGON)}$	$V_{O(PreCHGON)}$ = $V_{(PACK)}$ - $V_{(ZVCHG)}$, pre-charge FET on (8)	R_{GS} = 1MΩ, T_A = –20 to 110°C		9	11.25	13.5	V
$V_{(PreCHGOFF)}$	Output voltage, pre-charge FET off (8)	R_{GS} = 1MΩ, T_A = –20°C to 110°C				V_{BAT} - 0.5	V
t_r	Rise time	C_L = 4700 pF, R_G = 5.1KΩ	V_{ZVCHG}: 10% to 90%		80	200	µs
t_f	Fall time	C_L = 4700 pF, R_G = 5.1KΩ	V_{ZVCHG} : 90% to 10%		1.7		ms
SMBµs							
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle		10		100	KHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend			51.2		KHz
t_{BUF}	Bus free time between start and stop			4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start			4			µs
$t_{SU:STA}$	Repeated start setup time			4.7			µs
$t_{SU:STO}$	Stop setup time			4			µs
$t_{HD:DAT}$	Data hold time	Receive mode		0			ns
		Transmit mode		300			
$t_{SU:DAT}$	Data setup time			250			ns
$t_{TIMEOUT}$	Error signal/detect	See (9)		25		35	ms
t_{LOW}	Clock low period			4.7			µs
t_{HIGH}	Clock high period	See (10)		4		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (11)				25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (12)				10	ms
t_f	Clock/data fall time	See (13)				300	ns
t_r	Clock/data rise time	See (14)				1000	ns

(8) For a V_{BAT} or V_{PACK} input range of 3.8V to 18.75V, MIN $V_{O(FETON)}$ voltage is 9V or V(BAT) - 1V, whichever is less.
(9) The bq28300 times out when any clock low exceeds $t_{TIMEOUT}$
(10) $t_{HIGH:MAX}$, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 µs, causes reset of any transaction involving bq28300 that is in progress.
(11) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(12) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(13) Rise time t_r = V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15).
(14) Fall time t_f = 0.9V_{DD} to (V_{ILMAX} – 0.15).

PRODUCT PREVIEW

PIN EQUIVALENT CIRCUITS

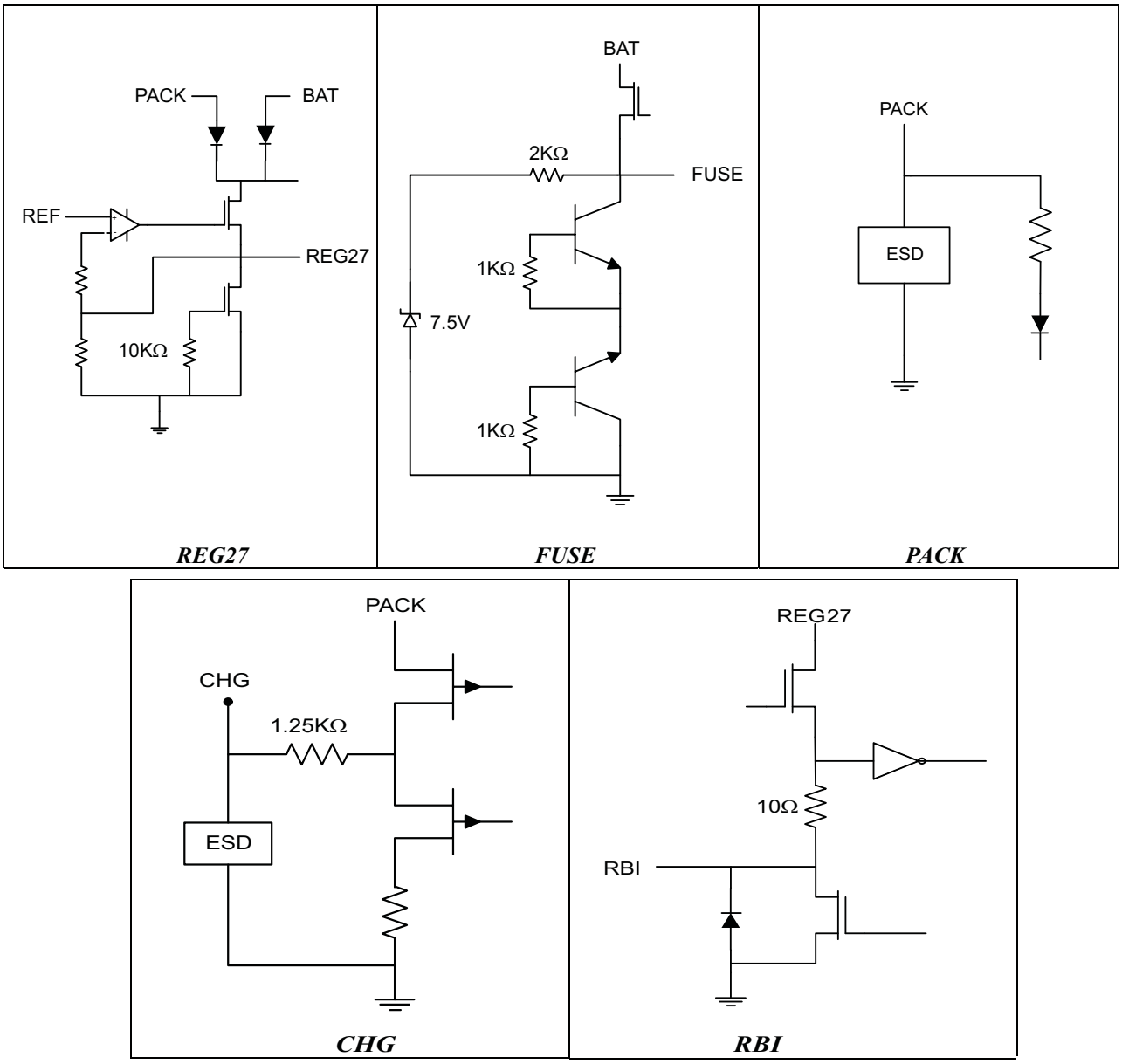


BAT | *DSG* | *VC1 and VC2*

VC3 | *SRP and SRN* | *TS1*

SMBD and SMBC | *$\overline{PRES}$* | *ZVCHG*

PRODUCT PREVIEW



TIMING CIRCUITS

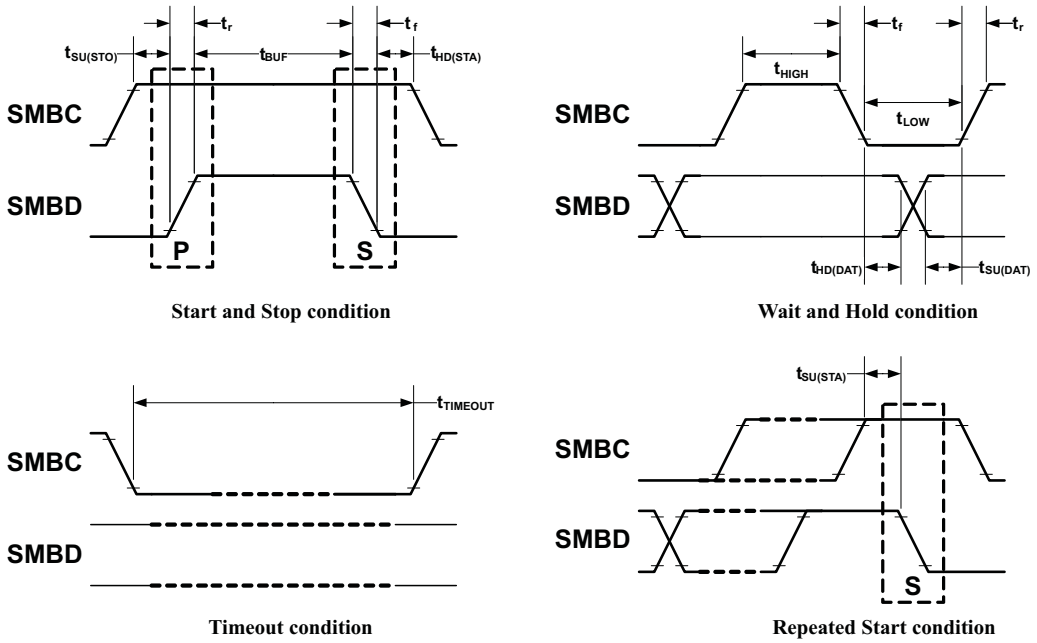


Figure 1. Timing Conditions

GENERAL OVERVIEW

The bq28300 has a flexible architecture that allows development of numerous battery-management solutions. The device is a fully integrated battery manager as shown in the functional block diagram, and performs necessary calculations and control for a fully functional battery management system. The device provides flexible user specific settings which are stored in single-write non-volatile memory

The bq28300 determines battery capacity by monitoring the amount of charge input or removal from 2 or 3 cell Li-Ion rechargeable batteries via a small value series sense resistor. The device then controls and reports the battery status using corrections for environmental and operating conditions. Additional control and monitoring is implemented for individual cell voltages, temperature, and current.

PRODUCT PREVIEW

FEATURE SET

Safety Features

The bq28300 supports a wide range of battery and system protection features that can be configured. The primary safety features include:

- Cell over/undervoltage protection
- Overcurrent during charge and discharge
- Short Circuit
- Overtemperature during charge and discharge
- Device watchdog timer

The secondary safety features used to indicate more serious faults which can be used to control FET state or blow an in-line fuse to permanently disable the battery pack include:

- Safety overvoltage
- Safety undervoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge, pre-charge, and discharge FET fault
- Cell imbalance detection
- Internal AFE register and communications fault

Charge Control

The bq28300 charge control features include:

- Reporting charging current needed for constant current charging and charging voltage needed for constant voltage charging to a smart charger using SMBµs communications.
- Supports pre-charging/0-volt charging.
- Support fast charging.
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms.

Gas Gauging

The device uses advanced CEDV (Compensated End-of-Discharge Voltage) technology to measure and calculate the available charge capacity in battery cells under system use and environmental conditions. The device accumulates a measure of charge and discharge currents, then compensates the charge current measurement for temperature and the state-of-charge of the battery. The bq28300 further estimates battery self-discharge, adjusts the self-discharge estimation for temperature, and then updates internal status registers. These internal registers and made available to system host via the 2-wire SMBµs.

The general-purpose SRAM where the gas gauging registers are kept and updated, can be powered by the RBI pin of the bq28300 if power is lost. Typically, a 0.1µF capacitor provides the necessary voltage to the SRAM array during inadvertent momentary power loss.

See the bq28300 technical reference guide for further details.

6.4 Lifetime Data Logging

The bq28300 maintains the highest temperature value from the last bq28300 reset.

Power Modes

The bq28300 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the device performs measurements, calculations, protection decisions, and data updates in 1 second intervals. Between these intervals, the device is in a reduced power stage.

- In Sleep Mode, the bq28300 performs measurements, calculations, protection decisions and data updates in longer intervals. Between these intervals, the device is in a reduced power stage.
  - A wake function operates so that an exit from Sleep mode occurs when current flow, detection of failure, or SMBμs activity detected.
- In Shutdown Mode the bq28300 is completely disabled by turning off all FETs and powering down the bq28300. If power is lost during this time, the bq28300 will power-up with initial User Settings provided during the Commit writing process.

User Settings and Program Execution

The bq28300 user configuration and calibration settings are developed and stored in bq28300 non-volatile memory during the User Setting Commit process. This memory can only be written to in a single instance and is non-erasable. All program execution is then performed using the bq28300 Instruction memory and the fixed user setting memory. During operation, dynamic operational parameters are stored in the bq28300 RAM and these values will be lost if power is removed except. A Permanent Fail condition is retained in non-volatile memory and is not affected by power loss or reset.

CONFIGURATION

Oscillator Function

The bq28300 fully integrates the system oscillator; therefore, no external components are required for this feature.

System Present Operation

The device checks the $\overline{\text{PRES}}$ pin periodically. If the $\overline{\text{PRES}}$ pin input is pulled to ground by external system, the bq28300 detects this event as the presence of the system.

2 or 3 Cell Configuration

The bq28300 can support either 2 or 3 cell battery pack configurations. In a 2-cell configuration, VC1 is shorted to VC2

Cell Balancing Configuration

If cell balancing is required, the bq28300 cell balance control allows a weak, internal pull-down for each VCx pin. The purpose of this weak pull-down is to enable an external FET for current bypass. Series resistors placed between the input VCx pins and the positive battery cell terminals control the VGS of the external FET. (Further details are provided in the APPLICATION INFORMATION section of this document)

BATTERY PARAMETER MEASUREMENTS

The bq28300 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell voltage, battery voltage, and temperature measurements. The individual cell voltages, *Voltage, Current, AverageCurrent, and Temperature* are updated in 1 second intervals during normal operation.

Charge and Discharge Counting

The integrating ADC measures the charge and discharge flow of the battery by monitoring a small-value sense resistor between the SRP and SRN pins. The bq28300 integrating ADC measures bipolar signals across the SRP and SRN pins from -0.20V to 0.25V induced by current through the sense resistor (typically 5 mΩ to 20 mΩ). Charge activity is detected when $V_{SR} = V_{SRP} - V_{SRN}$ is positive and discharge activity when $V_{SR} = V_{SRP} - V_{SRN}$ is negative. The bq28300 continuously integrates the signal over time, using an internal counter and updates *RemainingCapacity* with the charge or discharge amount every second.

Voltage

While monitoring the SRP and SRN pins for charge and discharge currents, the bq28300 monitors the individual series cell voltages. The internal bq28300 ADC then measures the voltage, scales, applies offsets, and calibrates it appropriately.

PRODUCT PREVIEW

NOTE: For accurate differential voltage sensing, the VSS ground should be connected directly to the most negative terminal of the battery stack, not to the positive side of the sense resistor. This minimizes the voltage drop across the PCB trace.

Voltage Calibration and Accuracy

The bq28300 is calibrated for voltage prior to shipping from TI. The bq28300 voltage measurement signal chain (ADC, high voltage translation, circuit interconnect) will be calibrated for each cell. The external filter resistors, connected from each cell to the VCx input of the bq3060, are required to be 1kΩ. If different voltage accuracy is desired, customer voltage calibration is required prior to the Commit process.

Current

The bq28300 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5 mΩ to 20 mΩ typical sense resistor.

Temperature

The bq28300 has an internal temperature sensor and input pin for an external temperature sensor. The bq28300 can be configured to use either the internal or external temperature sensor. Default setting for the bq28300 is for a Semitec 103AT thermistor as input to the TS1 pin. Reporting of measured temperature is available by way of the SBS Temperature command.

COMMUNICATIONS

The bq28300 uses SMBus v1.1 in Slave Mode per the SBS specification.

SBS Commands

Table 1. SBS COMMANDS

SBS Command	Mode	Name	Format	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	H2	0x0000	0xffff	-	
0x03	R/W	BatteryMode	H2	0x0000	0xe383	-	
0x08	R	Temperature	U2	0	65535	-	0.1degK
0x09	R	Voltage	U2	0	65535	-	mV
0x0a	R	Current	I2	-32768	32767	-	mA
0x0b	R	AverageCurrent	I2	-32768	32767	-	mA
0x0d	R	RelativeStateOfCharge	U1	0	100	-	%
0x0f	R/W	RemainingCapacity	U2	0	65535	-	mAh or 10mWh
0x10	R	FullChargeCapacity	U2	0	65535	7200	mAh
0x14	R	ChargingCurrent	U2	0	65534	2500	mA
0x15	R	ChargingVoltage	U2	0	65534	12600	mV
0x16	R	BatteryStatus	U2	0x0000	0xdbff	-	
0x17	R/W	CycleCount	U2	0	65535	0	
0x18	R/W	DesignCapacity	U2	0	65535	7200	mAh
0x19	R/W	DesignVoltage	U2	0	65535	10800	mV
0x1a	R/W	SpecificationInfo	H2	0x0000	0xffff	0x0031	
0x1b	R/W	ManufactureDate	U2	-	-	0	ASCII
0x1c	R/W	SerialNumber	H2	0x0000	0xffff	0x0001	
0x20	R/W	ManufacturerName	S12	-	-	Texas Inst.	ASCII
0x21	R/W	DeviceName	S8	-	-	bq28300	ASCII
0x22	R/W	DeviceChemistry	S5	-	-	LION	ASCII
0x23	R/W	ManufacturerData	S9	-	-	-	ASCII
0x3d	R	CellVoltage3	U2	0	65535	-	mV
0x3e	R	CellVoltage2	U2	0	65535	-	mV
0x3f	R	CellVoltage1	U2	0	65535	-	mV

PRODUCT PREVIEW

APPLICATION INFORMATION

Run Time to Empty

To predict how much run time the battery pack can supply to host system, a “Run Time To Empty” value can be calculated.

The SBS host system will need to read, store, and update the following values during a discharging period and average them over a user determined period of time:

- DSG bit of BatteryStatus register (ensure in discharge mode)
- AverageCurrent (mA)
  - Positive value = charge current
  - Negative value = discharge current
  - One minute rolling average of current - the user may wish to accumulate this time and average for larger granularity)
- RemainingCapacity (mAh)

Then calculating:

RunTimeToEmpty = RemainingCapacity(avg mAh) ÷ AverageCurrent(avg mA) (the result will be In hours, the user may wish to take result above and divide by 60 for minutes)

Charging Time to Full

To predict how much charging time before the battery pack will be fully charged, a “Run Time To Full” value can be calculated.

The SBS host system will need to read, store, and update the following values during a charging period and average them over a user determined period of time:

- DSG bit of BatteryStatus register (specify in charge mode)
- AverageCurrent (mA)
  - Positive value = charge current
  - Negative value = discharge current
  - One minute rolling average of current - the user may wish to accumulate this time and average for larger granularity)
- RemainingCapacity (mAh)

Then calculating:

RunTimeToFull = [FullChargeCapacity(avg mAh) - RemainingCapacity(avg mAh)] ÷ AverageCurrent(avg mA)

Remaining Capacity Alert

To provide enough time for action to be taken when battery is below a pre-determined capacity, the user may wish to implement in SMBµs host system a remaining capacity alarm alert. To do this, a SMBµs read of the *RemainingCapacity* value should be completed then compared by the SMBµs host to a user selected value. If the read *RemainingCapacity* value is < the users Remaining Capacity then the host system should instruct battery user of what action is needed.

Remaining Time Alert

Similar to the Remaining Capacity Notification, system operation may desire an alarm notification based on time rather than remaining capacity. To do this, a determination of the *EndTimeToEmpty* (as discussed below) and compared by SMB host to a user selected remaining time limit value. If the *RemainingTimeLimit* value is < *EndTimeToEmpty*, then the host system should instruct battery user of the action to be taken.

Cell Balancing

The need for cell balancing comes from the fact which cell-to-cell differences in self-discharge, capacity, and impedance can lead to different charge states among the cells. However, the charger terminates the charge based on the summed voltage only, which may leave some cells undercharged and others overcharged. To remedy this imbalance and to achieve the goal of having all cells reaching 100% state-of-charge at charge termination, it is necessary to reduce the charge added to the overcharged cells by creating a current bypass during charging.

Cell balancing in the bq28300 is accomplished by connecting an external parallel bypass load to each cell and enabling the bypass load depending on each individual cell's charge state. The bypass load is typically formed by a P-ch MOSFET and a resistor. The series resistors that connect the cell tabs to VC1~VC3 pins of the bq28300 are required to be 1KΩ. The bq28300 balances the cells during charge by discharging those cells above the threshold set in *Cell Balance Threshold*, if the maximum difference in cell voltages exceeds the value programmed in *Cell Balance Min*. During cell balancing, the bq28300 measures the cell voltages at an interval set in *Cell Balance Interval*. On the basis of the cell voltages, the bq28300 either selects the appropriate cell to discharge or adjusts the cell balance threshold up by the value programmed in *Cell Balance Window* when all cells exceed the cell balance threshold or the highest cell exceeds the cell balance threshold by the cell balance window.

Cell balancing only occurs when charging current is detected and the cell balance threshold is reset to the value in *Cell Balance Threshold* at the start of every charge cycle. The threshold is only adjusted once during any balance interval.

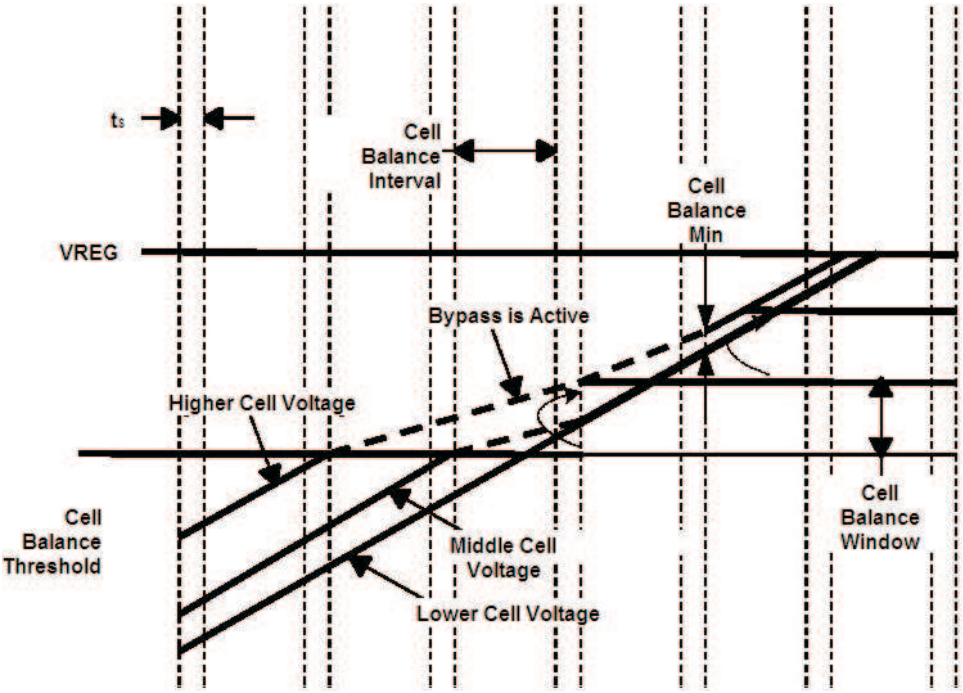
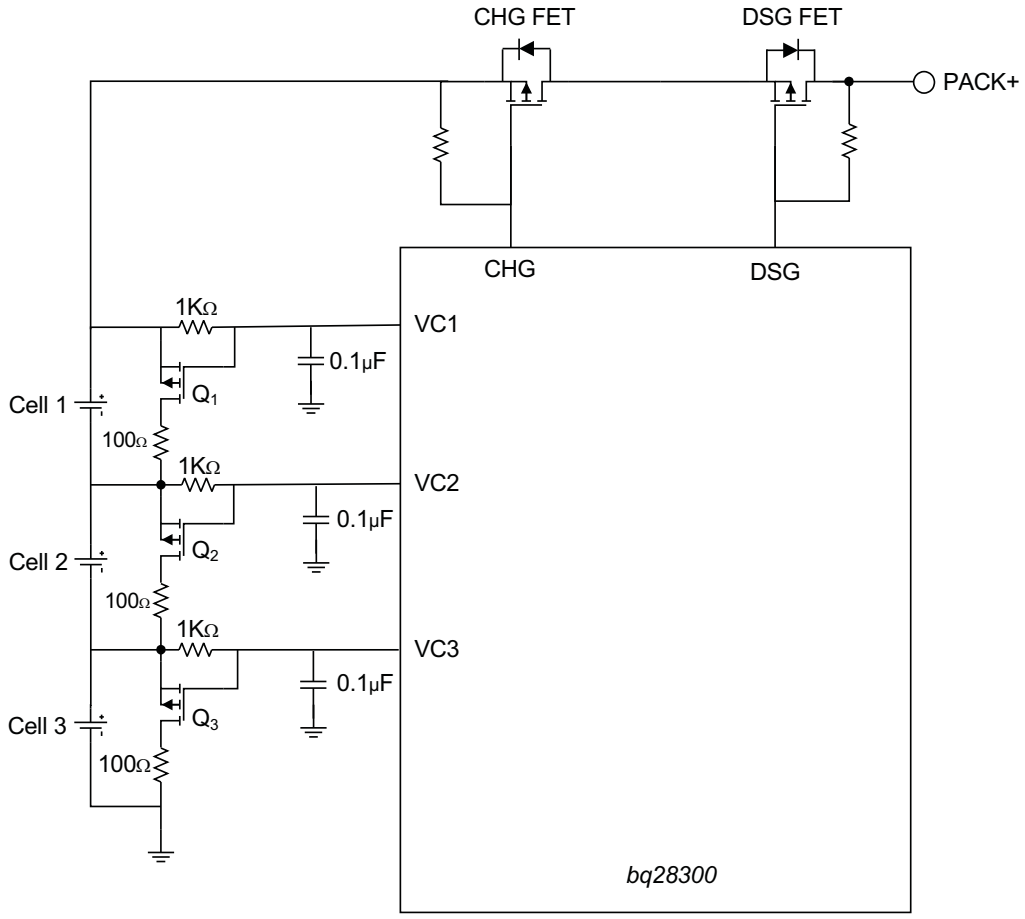


Figure 2. Cell Balance

The bq28300 supports cell balancing using external MOSFET as illustrated in Figure 3.

Figure 3 shows an example of a cell-balancing circuit for a 3-cell application. In this circuit, Q1, Q2, and Q3 are the external MOSFETs, specifically, Si1023 P-channel MOSFETs. This FET was chosen because of its low gate-to-source threshold voltage.

PRODUCT PREVIEW



NOTE: *Q1, Q2, and Q3 are Si1023 type P-ch FETs*

A. Q1, Q2, and Q3 are Si1023 type P-ch FETs.

Figure 3. Cell Balancing Circuit

Layout Recommendations

For an accurate differential voltage sensing, the VSS ground should be connected directly to the most negative terminal of the battery stack, not to the positive side of the sense resistor. This minimizes the voltage drop across the PCB trace.

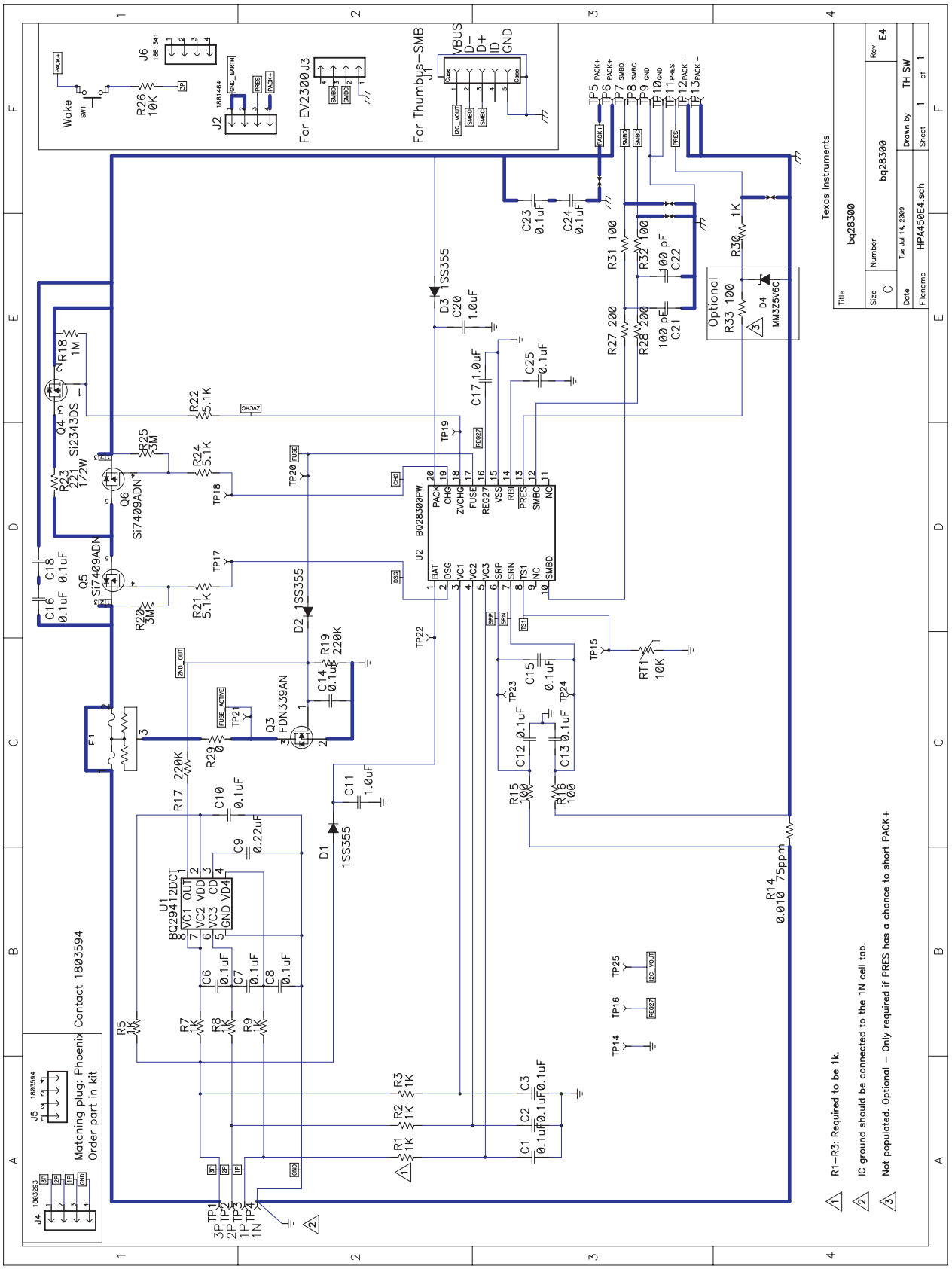


Figure 4. Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ28300PW	PREVIEW	TSSOP	PW	20	70	TBD	Call TI	Call TI
BQ28300PWR	PREVIEW	TSSOP	PW	20	2000	TBD	Call TI	Call TI

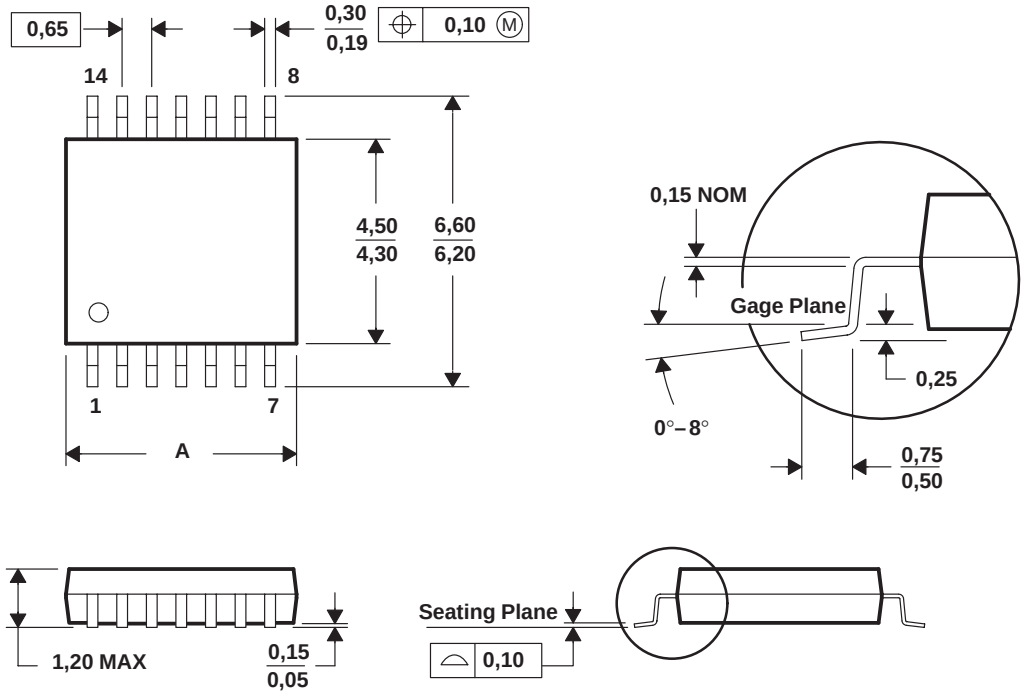
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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