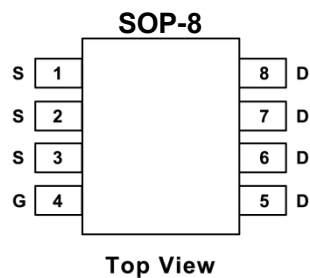
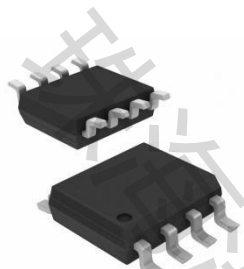


IRF7304TRPBF-HX

Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	Q _g (Typ.)	I _D (A)
-30	0.018 at V _{GS} = -10 V	17nC	-7.3
	0.018 at V _{GS} = -0.45 V		-6.3



FEATURES

- 100 % UIS Tested
- 100 % R_g Tested

APPLICATIONS

- Load Switches

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	-7.1	A
		-5.6	
Pulsed Drain Current ^C	I _{DM}	-40	
Avalanche Current ^C	I _{AS} , I _{AR}	-27	A
Avalanche energy L=0.1mH ^C	E _{AS} , E _{AR}	36	mJ
Power Dissipation ^B	P _D	2	W
		1.3	
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	R _{θJA}	48	62.5	°C/W
Maximum Junction-to-Ambient ^{AD}		74	90	°C/W
Maximum Junction-to-Lead	R _{θJL}	32	40	°C/W

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Ma	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$T_J=55^{\circ}\text{C}$			-5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 10	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.5	-2.0	-2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-7.1\text{A}$		17	25	m Ω
		$T_J=125^{\circ}\text{C}$		24	33	
		$V_{GS}=-4.5\text{V}$, $I_D=-5.6\text{A}$		27	40	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-7.1\text{A}$		24		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		104	125	pF
C_{oss}	Output Capacitance			180		pF
C_{rss}	Reverse Transfer Capacitance			125	175	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	2	4	6	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-7.1\text{A}$		19		nC
$Q_g(4.5\text{V})$	Total Gate Charge			9.6		nC
Q_{gs}	Gate Source Charge			3.6		nC
Q_{gd}	Gate Drain Charge			4.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=2.2\Omega$, $R_{GEN}=3\Omega$		10		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			26		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-7.1\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		11.		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-7.1\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		25		nC

Notes

- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.
- B. The power dissipation PD is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using.

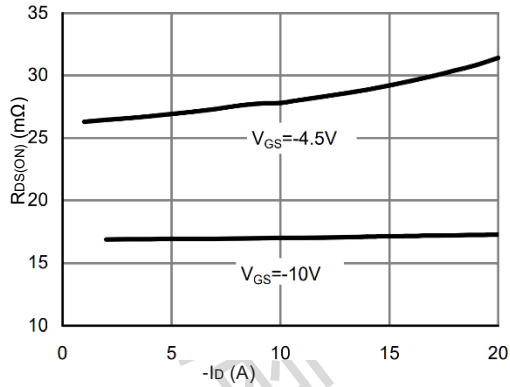


Fig 1. On-Resistance vs. Drain Current and Gate Voltage

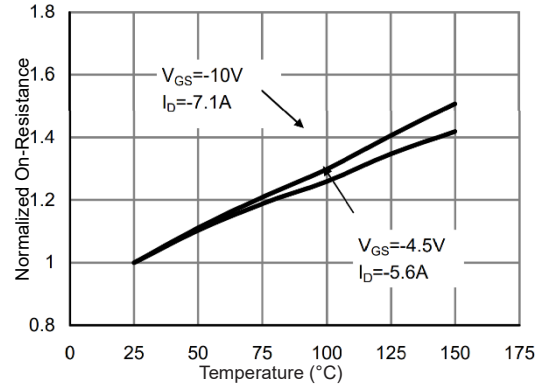


Fig 2. On-Resistance vs. Junction Temperature

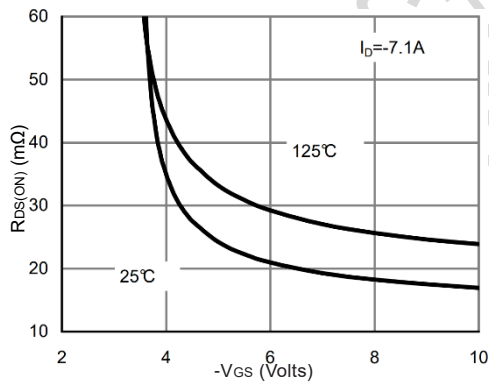


Fig 3. On-Resistance vs. Gate-Source Voltage

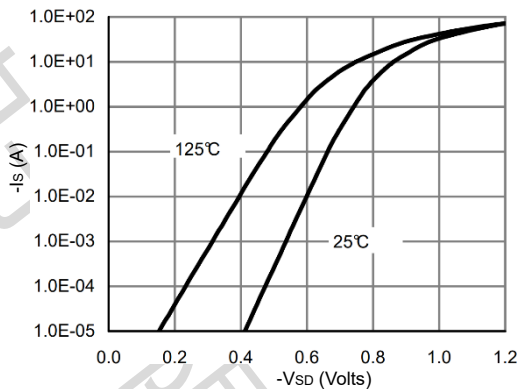


Fig 4. Body-Diode Characteristics

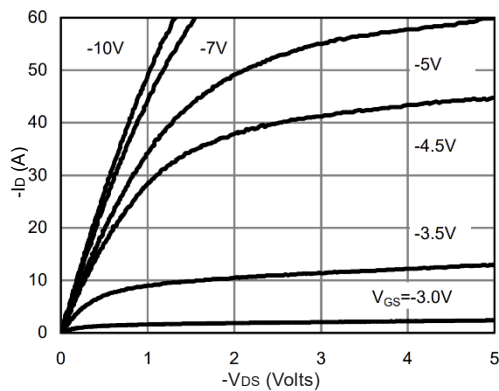


Fig 5. On-Region Characteristics

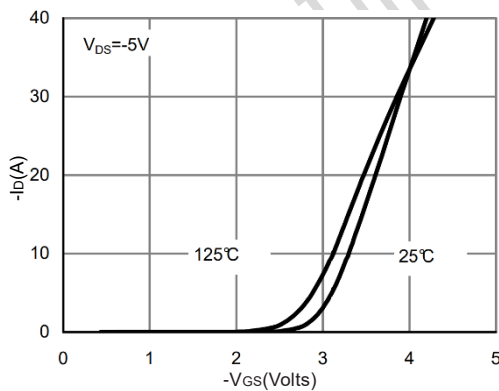


Fig 6. Transfer Characteristics

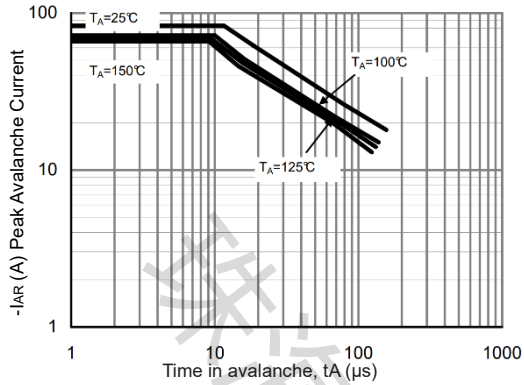


Fig 7. Single Pulse Avalanche capability

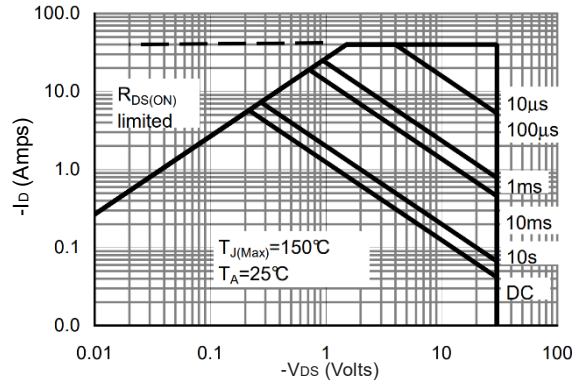


Fig 8. Maximum Forward Biased Safe Operating Area

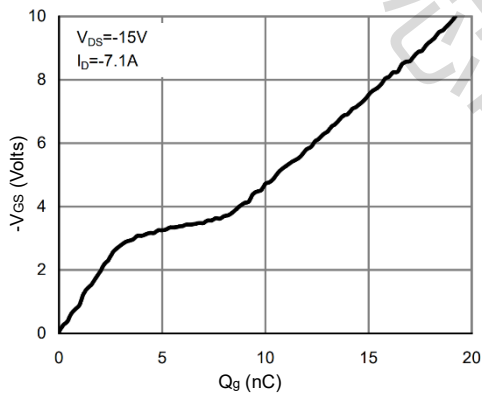


Fig 9. Gate-Charge Characteristics

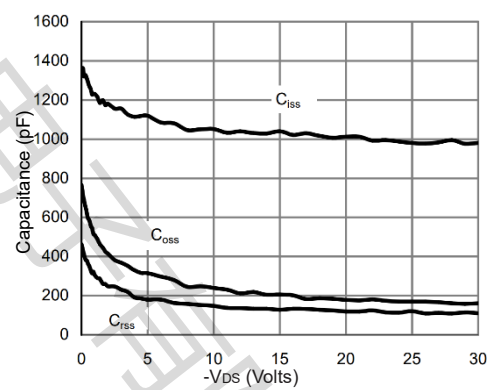


Fig 10. Capacitance Characteristics

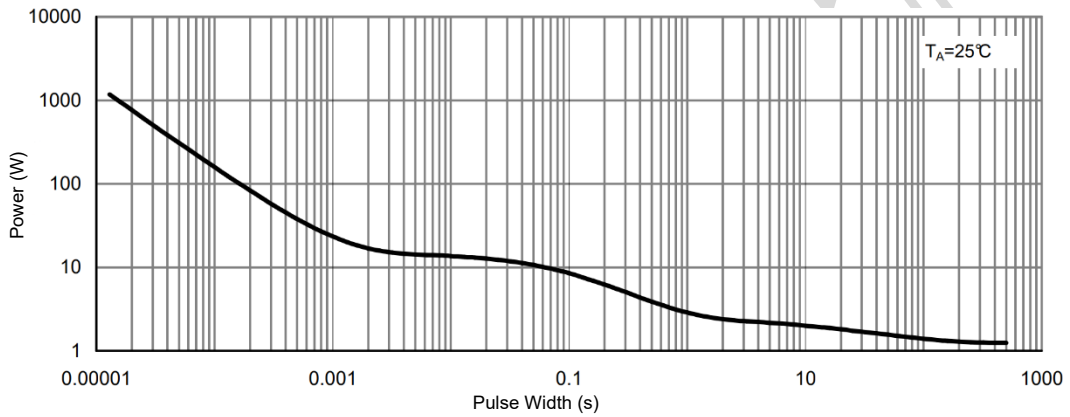


Fig 11. Single Pulse Power Rating Junction-to-Ambient

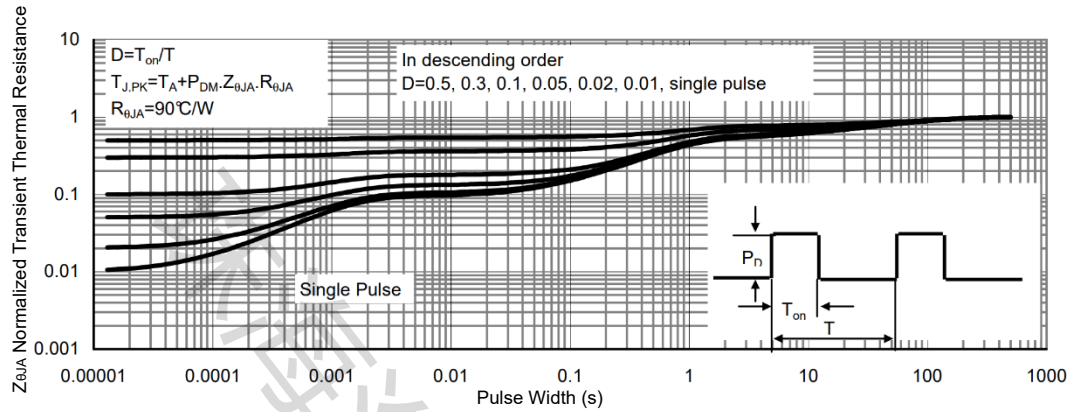
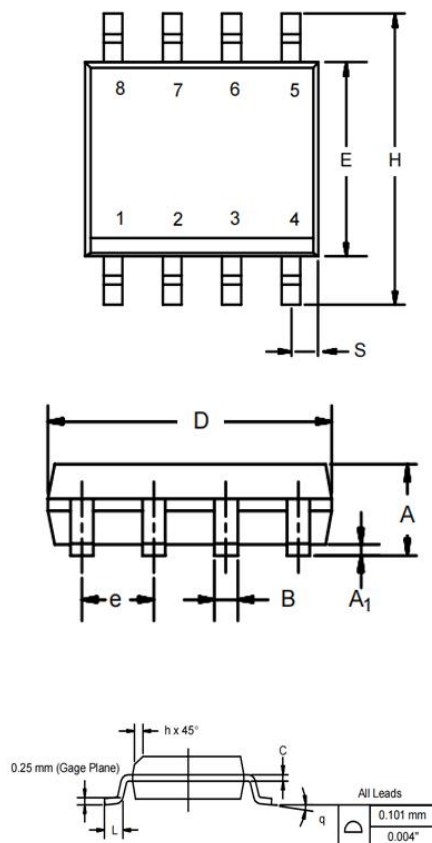


Fig 12. Normalized Maximum Transient Thermal Impedance

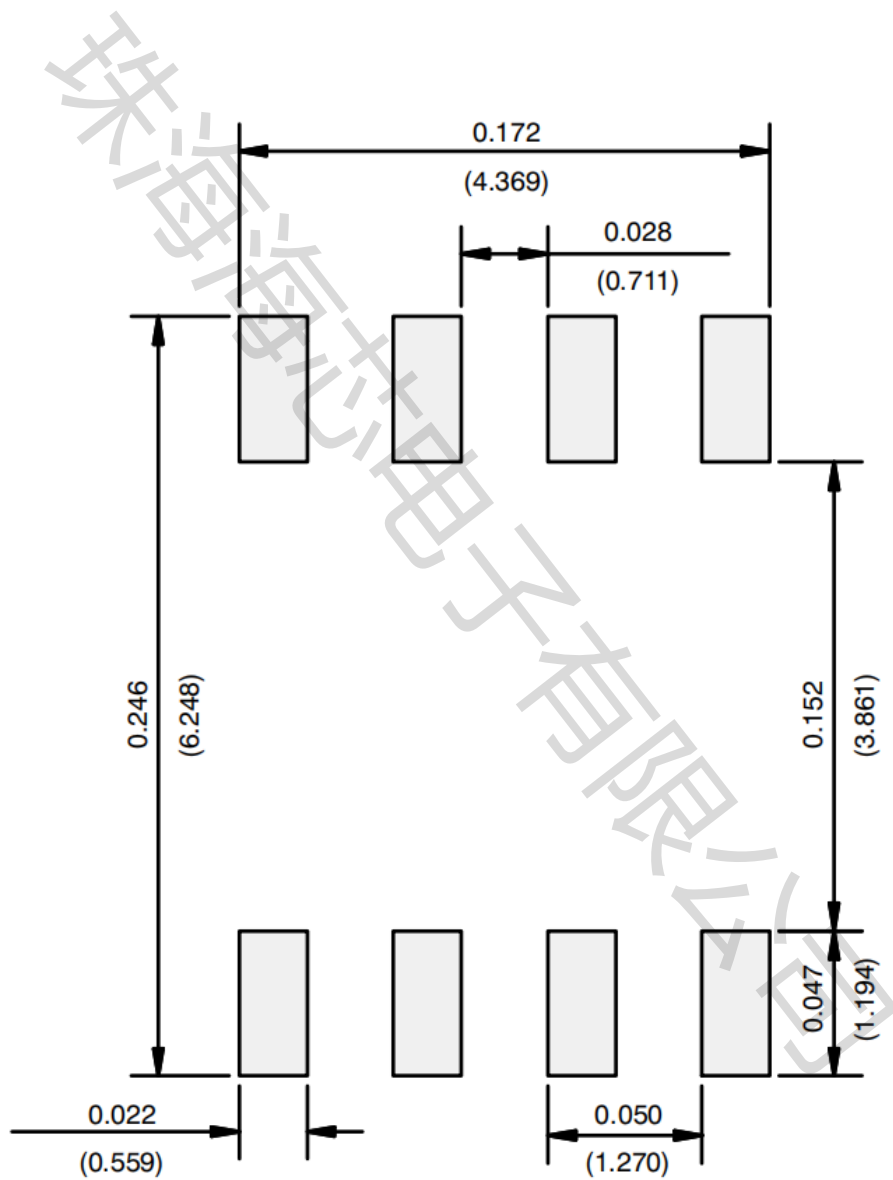
SOP-8 Package Outline

Dimensions are shown in millimeters (inches)



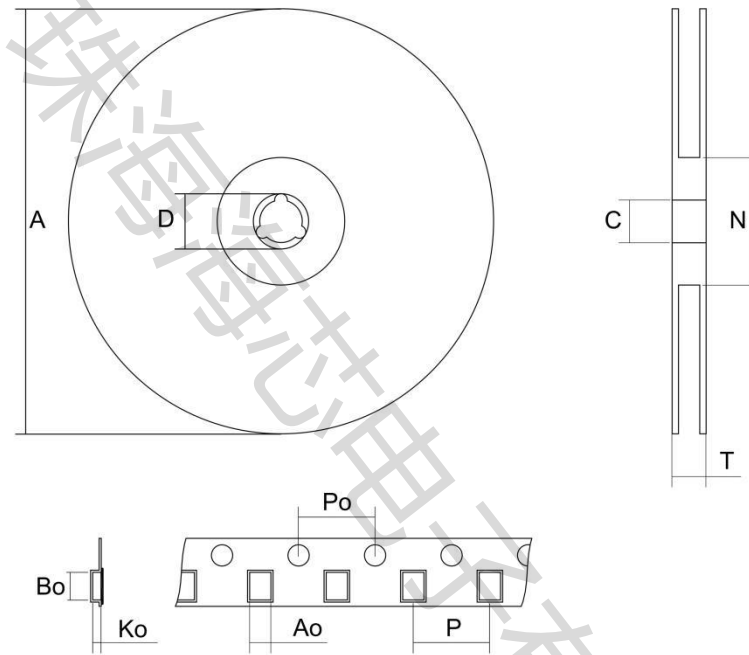
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

RECOMMENDED MINIMUM PADS FOR SOP-8

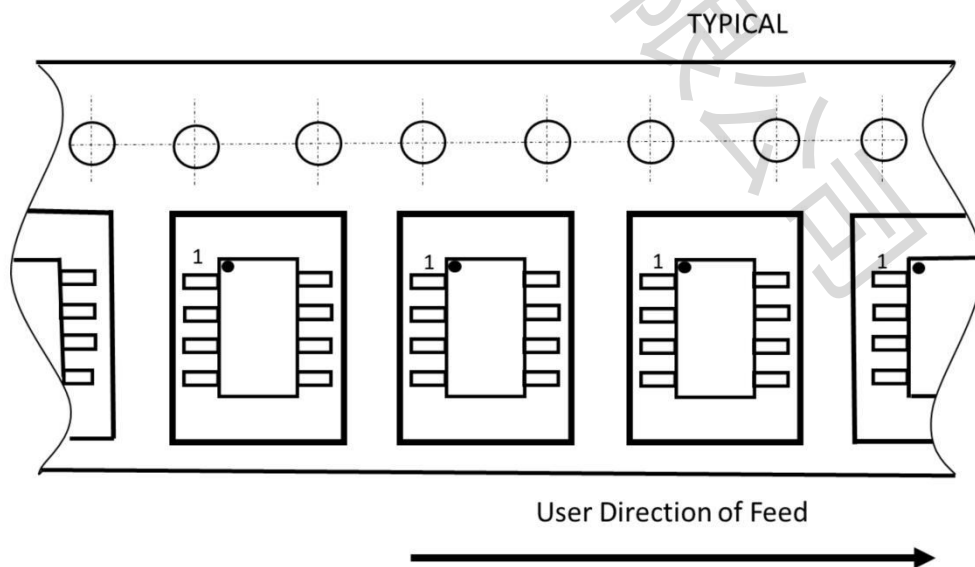


SOP-8 packing information

SOP-8 tape and reel



Tape orientation



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