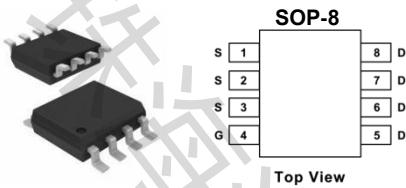


IRF7240TRPBF-HX P-Channel 40-V(D-S)MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	Q _g (Typ.)	I _D (A)
-40	0.010 at V _{GS} =-10 V	33nC	-16.1
	0.014 at V _{GS} =-4.5V		-13.3



FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g Tested

APPLICATIONS

- Load Switch
- Battery Switch
- Adapter switch
- Motor drive control

ABSOLUTE MAXIMUM RATINGS(T_A=25°C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-40	V
Gate-source voltage	V _{GS}	±20	
Continuous drain current(T _J =150°C)	I _D	T _C =25°C	A
		T _C =70°C	
		T _A =25°C	
		T _A =70°C	
Pulsed drain current(t=100μs)	I _{DM}	-80 ^a	mJ
Continuous source-drain diode current	I _S	T _C =25°C	
		T _A =70°C	
Single pulse avalanche current	L=0.1 mH	I _{AS}	
Single pulse avalanche energy	E _{AS}	20	
Maximum power dissipation	P _D	T _C =25°C	W
		T _C =70°C	
		T _A =25°C	
		T _A =70°C	
Operating junction and storage temperature range	T _J , T _{stg}	-55to+150	°C
Soldering recommendations(peak temperature)		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b,d}	R _{thJA}	40	50	°C/W
Maximum junction-to-foot(drain)	R _{thJF}	21	25	

Notes

- Package limited
- Surface mounted on 1"x 1"FR4 board
- t=10 s
- Maximum under steady state conditions is 85°C/W
- T_C=25°C

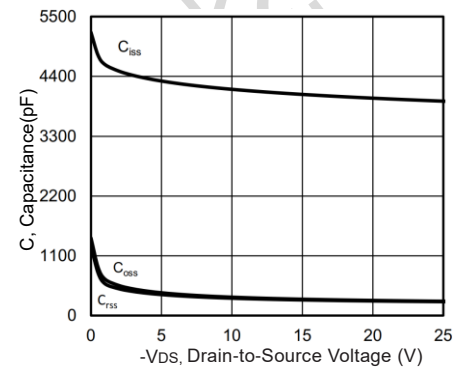
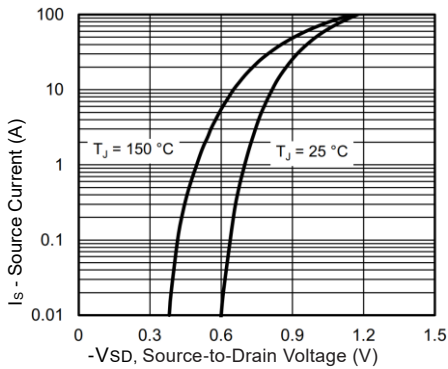
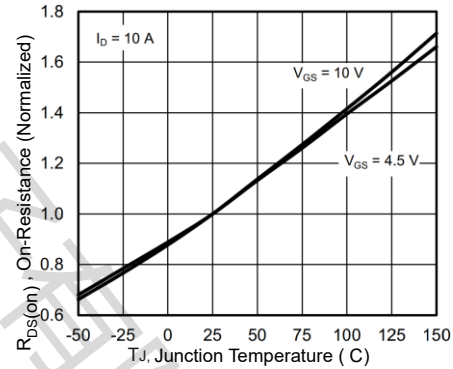
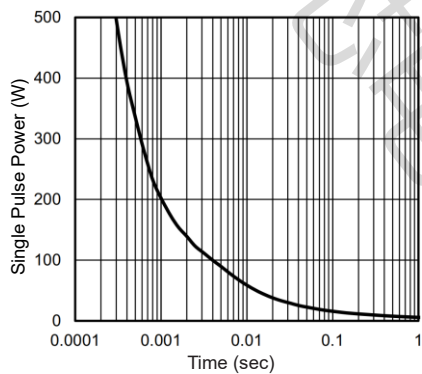
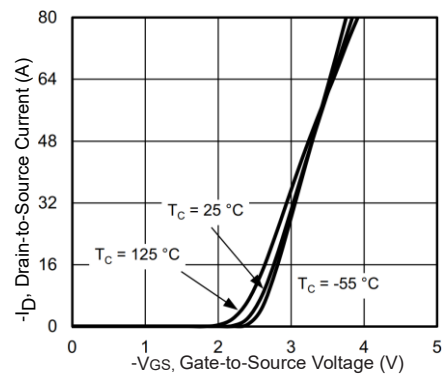
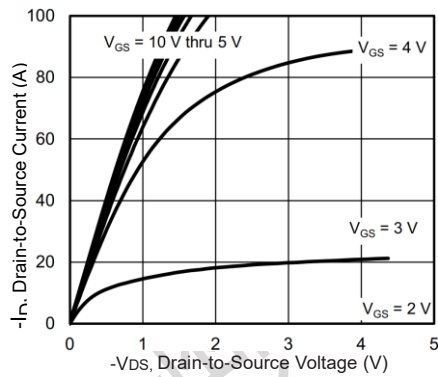
SPECIFICATIONS($T_J=25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS}=0\text{ V}, I_D=-250\mu\text{A}$	-40	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D=-250\mu\text{A}$	-	-33	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	4.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-	-2.3	V
Gate-source leakage	I_{GSS}	$V_{DS}=0\text{ V}, V_{GS}=\pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-40\text{ V}, V_{GS}=0\text{ V}$	-	-	-1	μA
		$V_{DS}=-40\text{ V}, V_{GS}=0\text{ V}, T_J=55^\circ\text{C}$	-	-	-10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS}\leq -5\text{ V}, V_{GS}=0\text{ V}$	-10	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS}=-10\text{ V}, I_D=-10\text{ A}$	-	0.0118	0.0142	Ω
		$V_{GS}=-4.5\text{ V}, I_D=-10\text{ A}$	-	0.0150	0.0183	
Forward transconductance ^a	g_{fs}	$V_{DS}=-10\text{ V}, I_D=-10\text{ A}$	-	45	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS}=-20\text{ V},$ $V_{GS}=0\text{ V},$ $f=1\text{ MHz}$	-	4000	-	pF
Output capacitance	C_{oss}		-	280	-	
Reverse transfer capacitance	C_{rss}		-	270	-	
Total gate charge	Q_g	$V_{DS}=-20\text{ V}, V_{GS}=-10\text{ V}, I_D=-10\text{ A}$	-	66	100	nC
		$V_{DS}=-20\text{ V}, V_{GS}=-4.5\text{ V}, I_D=-10\text{ A}$	-	31	47	
Gate-source charge	Q_{gs}	$V_{DS}=-20\text{ V}, V_{GS}=-4.5\text{ V}, I_D=-10\text{ A}$	-	9.8	-	
Gate-drain charge	Q_{gd}		-	10	-	
Gate resistance	R_g	$f=1\text{ MHz}$	0.5	1.6	3	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20\text{ V},$ $R_L=2\Omega, I_D=-10\text{ A},$ $V_{GEN}=-10\text{ V}, R_g=1\Omega$	-	12	24	ns
Rise time	t_r		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	44	88	
Fall time	t_f		-	6	12	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20\text{ V},$ $R_L=2\Omega, I_D=-10\text{ A},$ $V_{GEN}=-4.5\text{ V}, R_g=1\Omega$	-	27	54	
Rise time	t_r		-	75	150	
Turn-off delay time	$t_{d(off)}$		-	39	78	
Fall time	t_f		-	39	78	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C=25^\circ\text{C}$	-	-	-4.5	A
Pulse diode forward current	I_{SM}		-	-	-80	
Body diode voltage	V_{SD}	$I_S=-5\text{ A}, V_{GS}=0\text{ V}$	-	-0.77	-1.1	V
Body diode reverse recovery time	t_{rr}	$I_F=-10\text{ A},$ $di/dt=100\text{ A}/\mu\text{s},$ $T_J=25^\circ\text{C}$	-	24	48	ns
Body diode reverse recovery charge	Q_{rr}		-	16	32	nC
Reverse recovery fall time	t_a		-	12	-	ns
Reverse recovery rise time	t_b		-	12	-	

Notes

a. Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$ b. Guaranteed by design, not subject to production testing

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



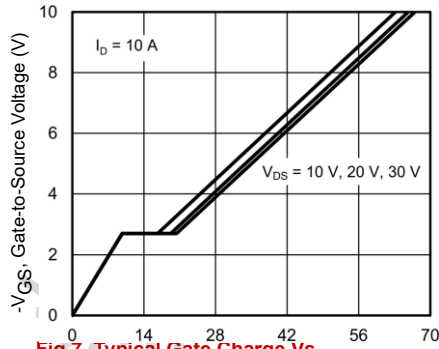


Fig 7. Typical Gate Charge Vs. Gate-to-Source Voltage

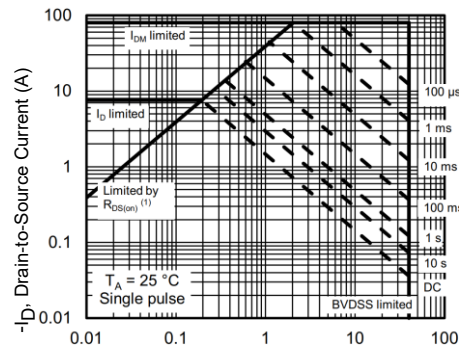


Fig 8. Maximum Safe Operating Area

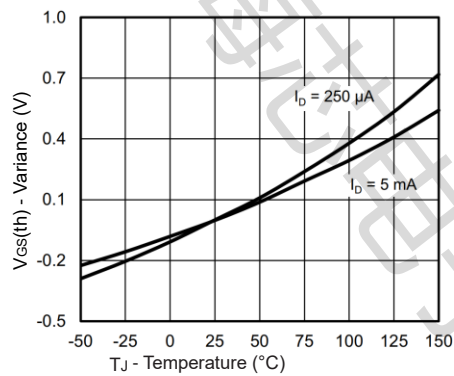


Fig 9. Threshold Voltage

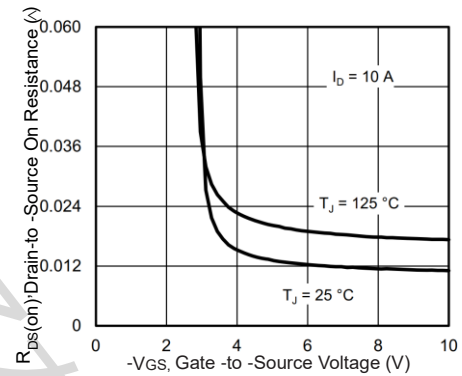


Fig 10. Typical On-Resistance Vs. Gate Voltage

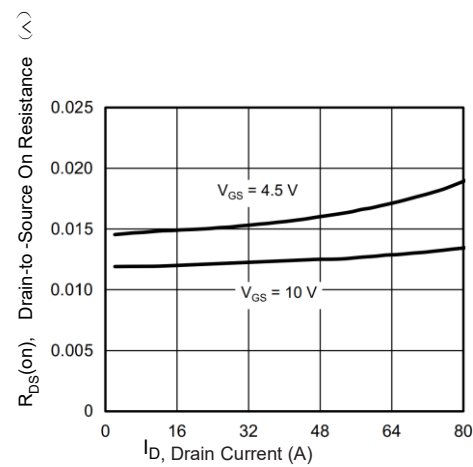


Fig 11. Typical On-Resistance Vs. Drain Current

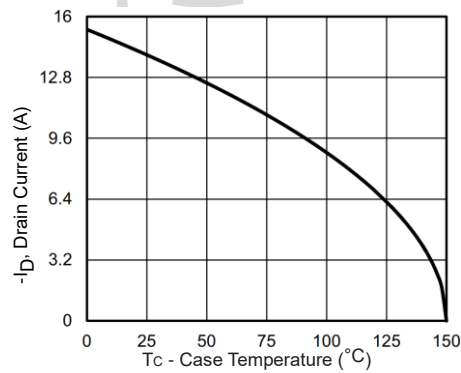


Fig 12. Current Derating^a

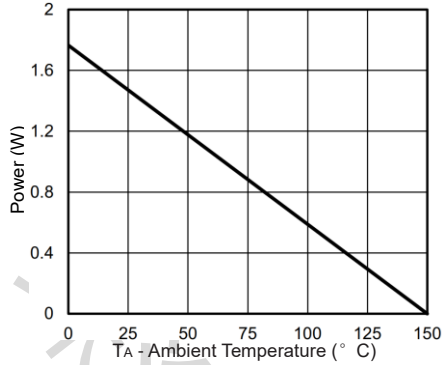


Fig 13. Power, Junction-to-Foot

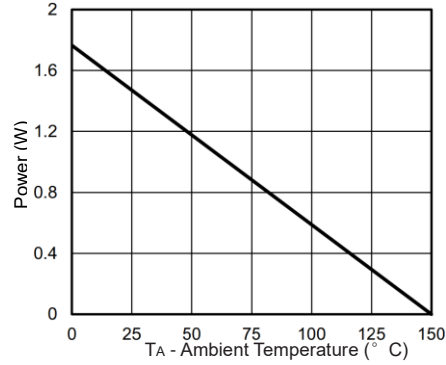


Fig 14. Power, Junction-to-Ambient

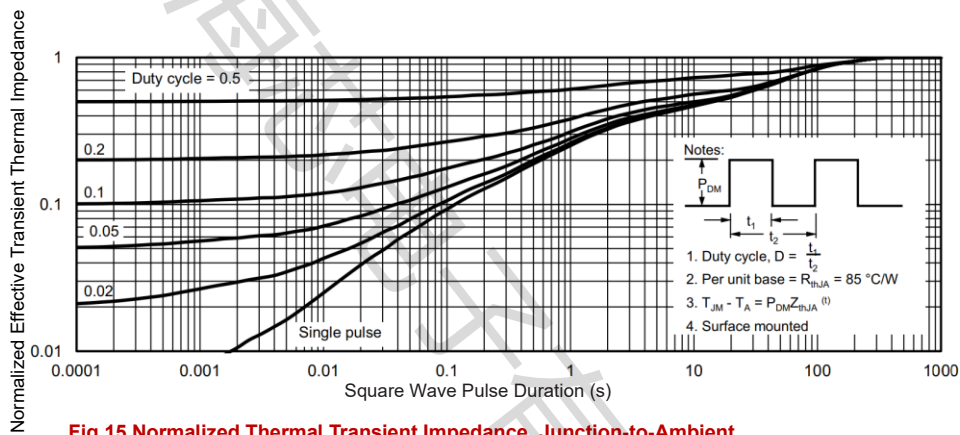


Fig 15. Normalized Thermal Transient Impedance, Junction-to-Ambient

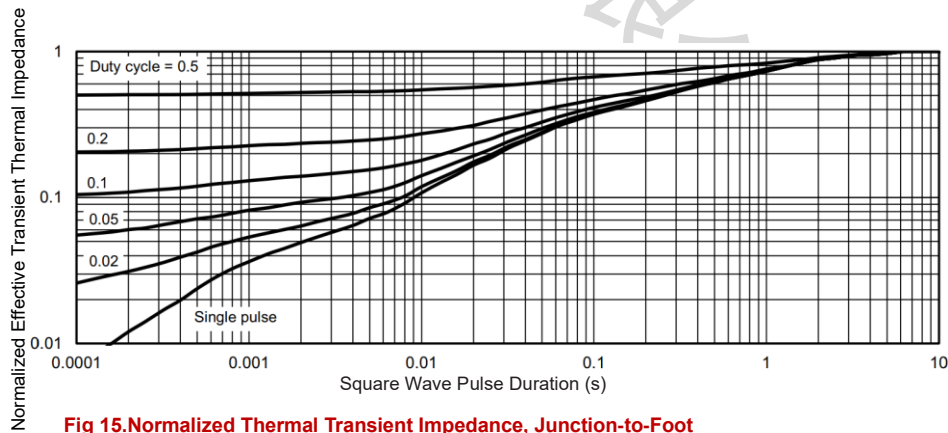


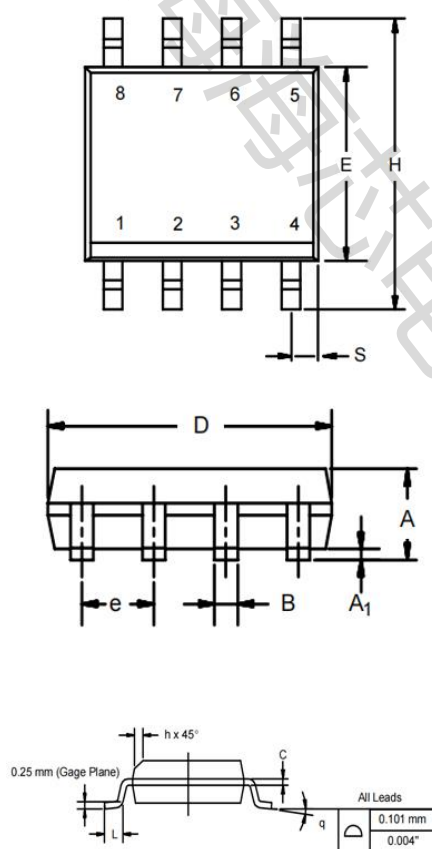
Fig 15. Normalized Thermal Transient Impedance, Junction-to-Foot

Note

- The power dissipation PD is based on $T_J \text{ max.} = 25^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

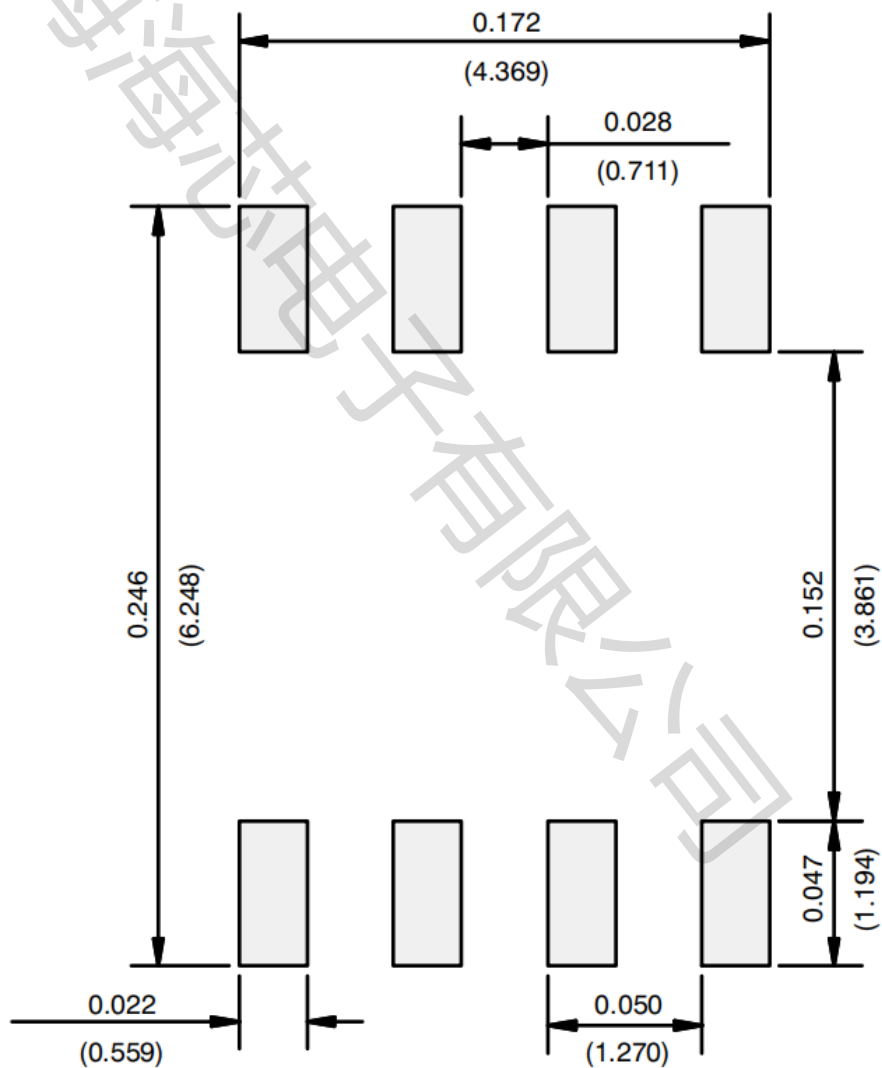
SOP-8 Package Outline

Dimensions are shown in millimeters(inches)



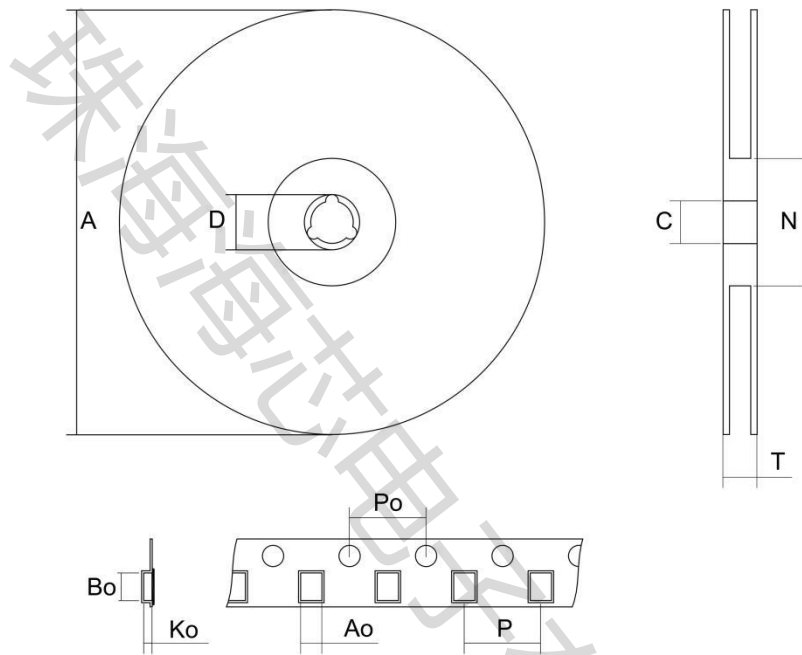
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

RECOMMENDED MINIMUM PADS FOR SOP-8

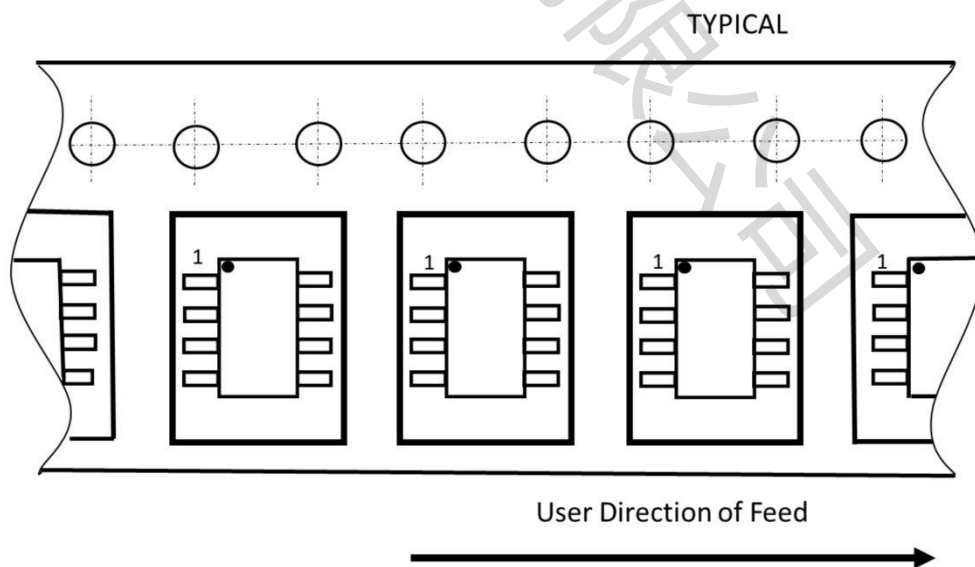


SOP-8 packing information

SOP-8 tape and reel



Tape orientation



Disclaimer

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