ANALOG DEVICES

DSP Microcomputer
ADSP-2115

FEATURES
Complete DSP Microcomputer
  ADSP-2101 Memory Variant
  1K Words of On-Chip Program Memory RAM
  512 Words of On-Chip Data Memory RAM
60 ns Instruction Cycle Time from 16.67 MHz Crystal
ADSP-2100 Family Code & Function Compatible
Two Double-Buffered Serial Ports Featuring
  Companding Hardware, Automatic Data Buffering
  and Multichannel Operation
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from
  Byte-Wide External Memory, e.g., EPROM
Single-Cycle Instruction Execution
Multifunction Instructions
Up to Three Edge- or Level-Sensitive External
  Interrupts
Low Power Dissipation in Standby Mode
Pin Compatible with ADSP-2101 and ADSP-2105
68-Lead PLCC, 80-Lead PQFP

GENERAL DESCRIPTION
The ADSP-2115 is a single chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications. Its instruction set is fully compatible with all other ADSP-2100 family processors. It combines the complete ADSP-2100 base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a programmable timer, extensive interrupt capabilities and on-chip program and data memory. The ADSP-2115 has 512 words of (16-bit) data memory RAM and 1K words of (24-bit) program memory RAM on chip.

Fabricated in a high speed, double layer metal CMOS process, the ADSP-2115 operates with a 60 ns instruction cycle time. Every instruction can execute in a single cycle.

The flexible architecture and comprehensive instruction set of the ADSP-2115 supports a high degree of operational parallelism. In one cycle the ADSP-2115 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive and transmit data via the two serial ports

FUNCTIONAL BLOCK DIAGRAM

ADSP-2100 BASE ARCHITECTURE
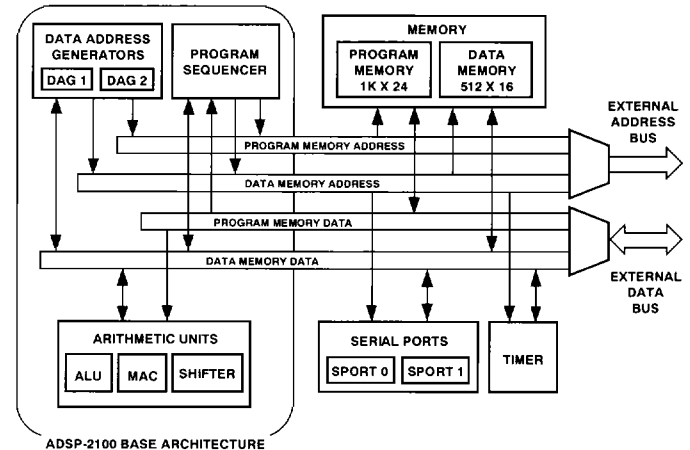
Development System
The ADSP-2115 is supported by a complete set of tools for software and hardware system development. The development software is a set of modules that supports all ADSP-2100 family processors. The system builder provides a high level method for defining the architecture of systems under development. The assembler produces object code, and the linker combines object modules and library calls into an executable file. The simulator provides an interactive instruction level simulation with a reconfigurable user interface. A PROM splitter generates PROM programmer compatible files. The C compiler generates ADSP-21xx assembly source code.

Additional Information
This data sheet provides a general overview of ADSP-2115 functionality. Please refer to the ADSP-2101 data sheet for complete ADSP-2115 specifications. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2101 User's Manual* or the *ADSP-2100 Family User's Manual*. For more information about the development system and programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals*.

Program Memory Interface
The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip data memory address (DMA) and data memory data (DMD) buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words, of which 1K is on-chip. The data bus is bidirectional and 24 bits wide to external program memory. Program memory may contain code and data.

AND1S005

ADSP-2115

The program memory select ($\overline{\text{PMS}}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-2115 writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps
Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 1 shows the two configurations. When MMAP = 0, internal RAM occupies 1K words beginning at address 0x0000. (Locations 0x0400 to 0x07FF are reserved and cannot be specified for use.) External program memory uses the remaining 14K words beginning at address 0x0800.

When MMAP = 1, 14K words of external program memory begin at address 0x0000. Internal RAM is located in the 1K word block, beginning at address 0x3800. In this configuration, program memory is not loaded although it can be written to and read from under program control. Locations 0x3C00 through 0x3FFF are reserved and cannot be specified for use.
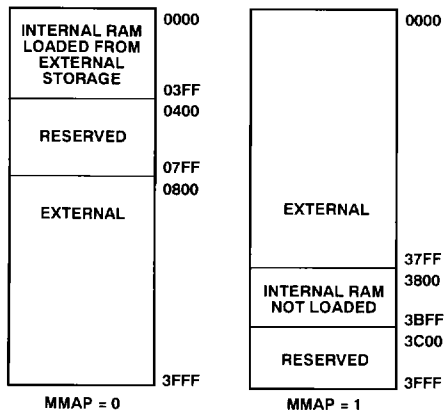

Figure 1. ADSP-2115 Program Memory Maps

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Data Memory Interface
The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{\text{DMS}}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-2115 supports memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
The on-chip data memory RAM resides in the 512 words of data memory beginning at address 0x3800, as shown in Figure 2. In addition, data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration, and serial port operations are located in this region of memory.
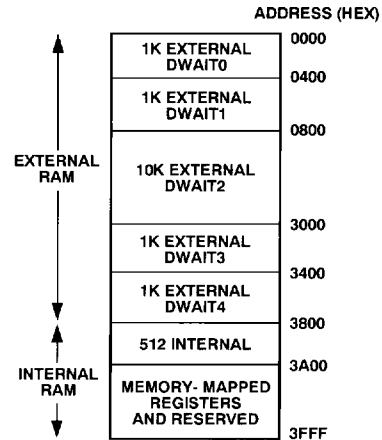

Figure 2. ADSP-2115 Data Memory Map

The remaining data memory is external. External data memory is divided into five zones, each associated with its own wait state generator. This allows slower peripherals to be memory mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{\text{RESET}}$.

IN-CIRCUIT EMULATORS
ADSP-2115 systems can be debugged using the ADSP-2101 EZ-ICE or the full-featured ADSP-2101 Emulator.

SPECIFICATIONS
Please refer to the ADSP-2101 data sheet for complete ADSP-2115 specifications including electrical characteristics, timing parameters, power dissipation, emulator restrictions, package dimensions and pin configurations.

Additional Specifications
There are two ADSP-2115 specifications that differ from the specifications found in the ADSP-2101 data sheet. These concern the operation of the serial ports. The ADSP-2115 SPORTs are specified for 13.824 Mb/s maximum data transfer rate. The ADSP-2101-50 timing and switching parameters should be used except for the following two changes:

t_{SCK} 72.3 ns minimum

t_{SCP} 28 ns minimum

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package
ADSP-2115KP-40	0°C to +70°C	10.24	68-Lead PLCC
ADSP-2115KP-55	0°C to +70°C	13.824	68-Lead PLCC
ADSP-2115KP-66	0°C to +70°C	16.67	68-Lead PLCC
ADSP-2115KS-40	0°C to +70°C	10.24	80-Lead PQFP
ADSP-2115KS-55	0°C to +70°C	13.824	80-Lead PQFP
ADSP-2115KS-66	0°C to +70°C	16.67	80-Lead PQFP
ADSP-2115BP-40	−40°C to +85°C	10.24	68-Lead PLCC
ADSP-2115BP-55	−40°C to +85°C	13.824	68-Lead PLCC
ADSP-2115BS-40	−40°C to +85°C	10.24	80-Lead PQFP
ADSP-2115BS-55	−40°C to +85°C	13.824	80-Lead PQFP