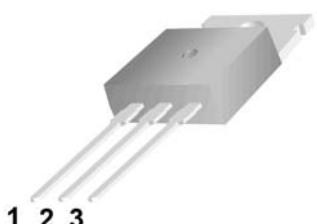
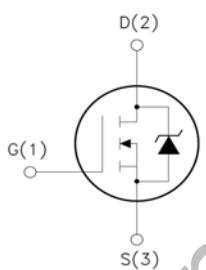


 <b>WGP50N06A</b> 60V N-Channel MOSFET	<b>TO-220</b>    <p> 1. Gate (G)  2. Drain (D)  3. Source (S) </p>
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### Absolute Maximum Ratings\* (T<sub>c</sub>=25°C Unless otherwise noted)

Symbol	PARAMETER	Value	Unit
V <sub>DSS</sub>	Drain-Source Voltage	60	V
I <sub>D</sub>	Drain Current	T <sub>c</sub> =25°C	50
		T <sub>c</sub> =100°C	35.4
V <sub>GSS</sub>	Gate Threshold Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (note1)	300	mJ
I <sub>AR</sub>	Avalanche Current (note2)	50	A
P <sub>D</sub>	Power Dissipation (T <sub>c</sub> =25°C)	85	W
T <sub>j</sub>	Junction Temperature(MAX)	175	°C
T <sub>stg</sub>	Storage Temperature	-55~+175	°C
T <sub>L</sub>	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	PARAMETER	Typ.	MAX.	Unit
R <sub>θJC</sub>	Thermal Resistance,Junction to Case	-	1.8	°C/W
R <sub>θJA</sub>	Thermal Resistance,Junction to Ambient	-	-	°C/W
R <sub>θCS</sub>	Thermal Resistance,Case to Sink	-	110	°C/W

**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	$\text{nA}$
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2.0	-	4.0	V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	7.8	12	$\text{m}\Omega$
Forward Transconductance	$g_{\text{fs}}$	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=20\text{A}$	18	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	2050	-	PF
Output Capacitance	$C_{\text{oss}}$		-	158	-	PF
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	120	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=30\text{V}, R_{\text{L}}=6.7\Omega$ $V_{\text{GS}}=10\text{V}, R_{\text{G}}=3\Omega$	-	7.4	-	nS
Turn-on Rise Time	$t_{\text{r}}$		-	5.1	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	28.2	-	nS
Turn-Off Fall Time	$t_{\text{f}}$		-	5.5	-	nS
Total Gate Charge	$Q_{\text{g}}$	$V_{\text{DS}}=30\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=10\text{V}$	-	50	-	nC
Gate-Source Charge	$Q_{\text{gs}}$		-	6	-	nC
Gate-Drain Charge	$Q_{\text{gd}}$		-	15	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{\text{SD}}$	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-		1.2	V
Diode Forward Current (Note 2)	$I_{\text{S}}$		-	-	50	A
Reverse Recovery Time	$t_{\text{rr}}$	$T_J = 25^\circ\text{C}, IF = 20\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ (Note 3)	-	28	-	nS
Reverse Recovery Charge	$Q_{\text{rr}}$		-	40	-	nC
Forward Turn-On Time	$t_{\text{on}}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_j=25^\circ\text{C}, V_{\text{DD}}=30\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

## Typical Characteristics

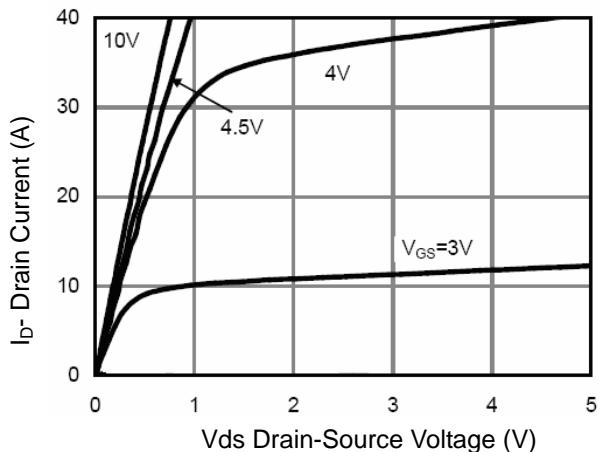


Figure 1 Output Characteristics

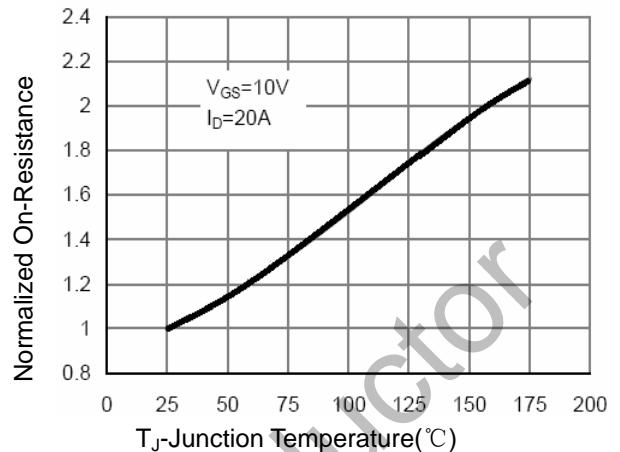


Figure 4 Rdson-Junction Temperature

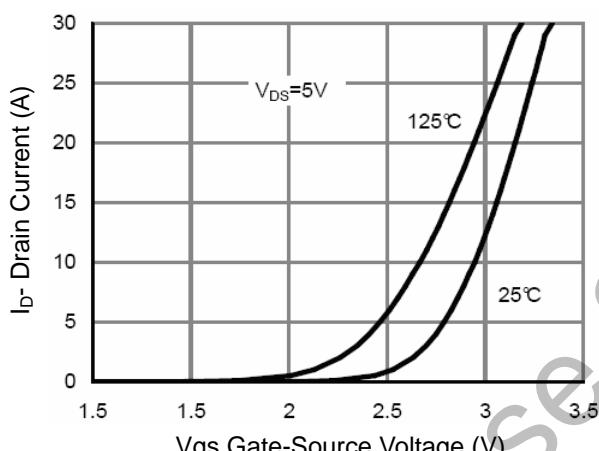


Figure 2 Transfer Characteristics

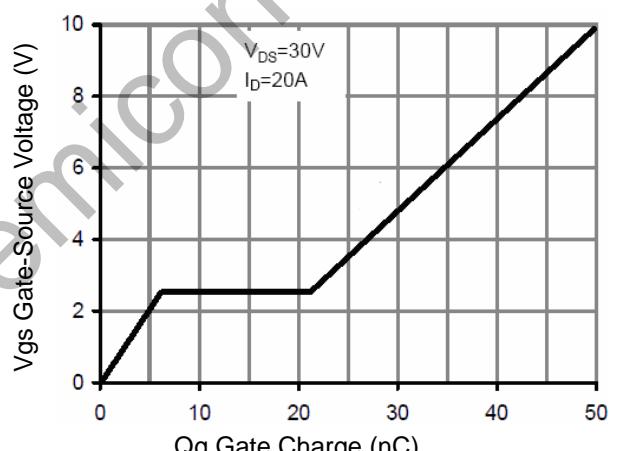


Figure 5 Gate Charge

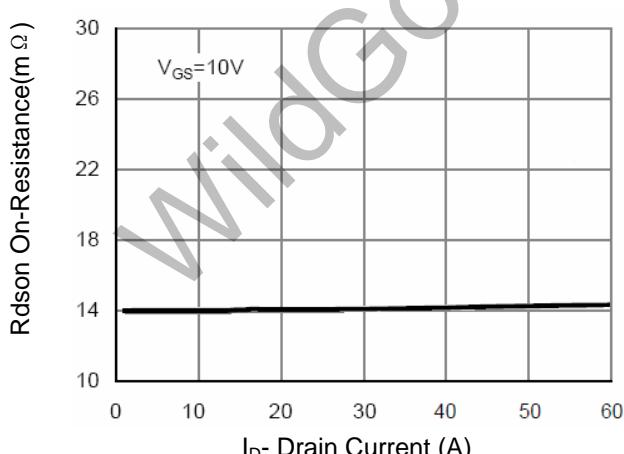


Figure 3 Rdson- Drain Current

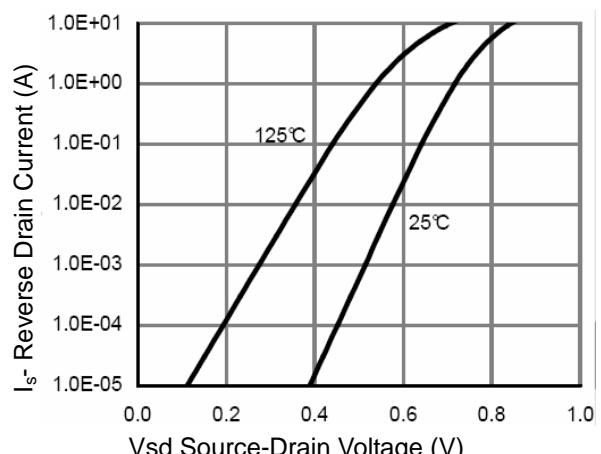


Figure 6 Source- Drain Diode Forward

## Typical Characteristics (Continued)

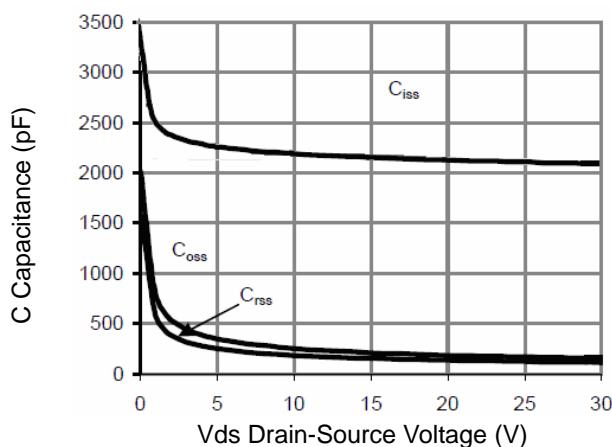


Figure 7 Capacitance vs Vds

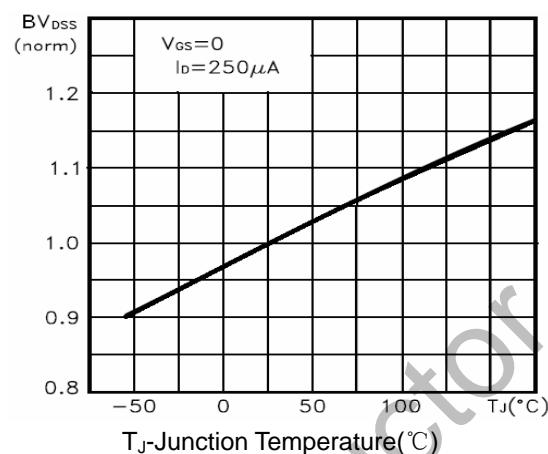
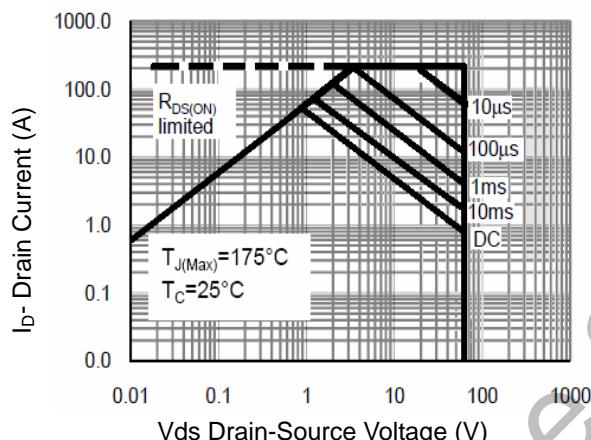
Figure 9  $BV_{DSS}$  vs Junction Temperature

Figure 8 Safe Operation Area

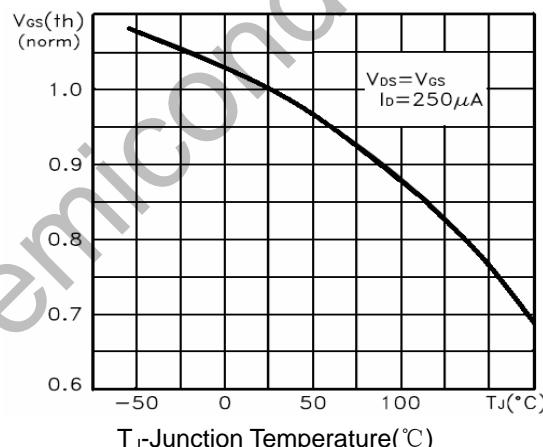
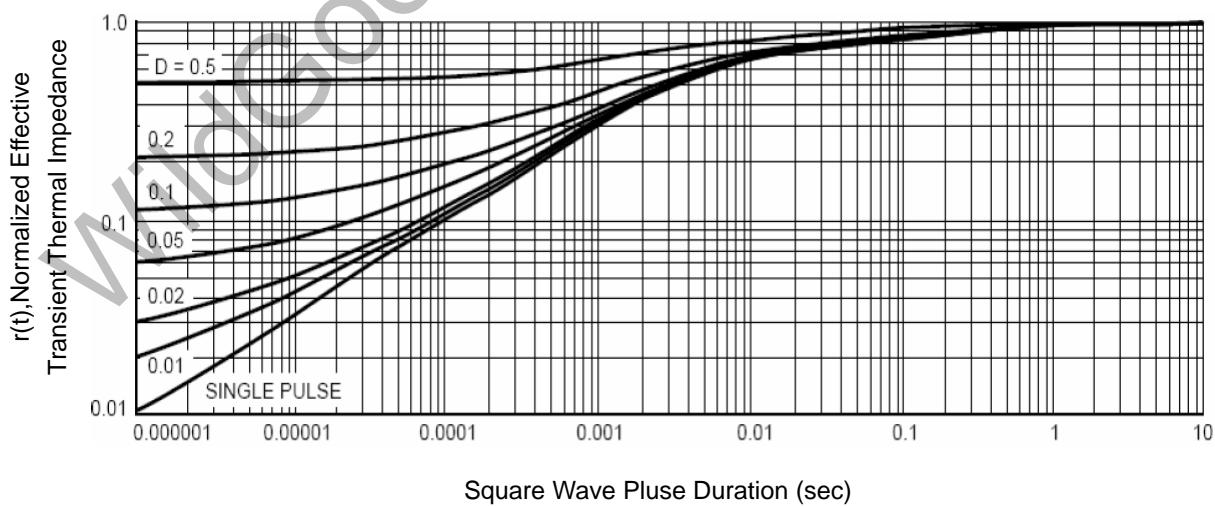
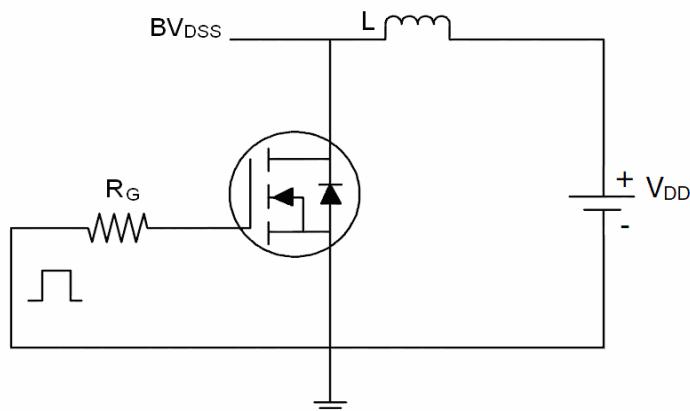
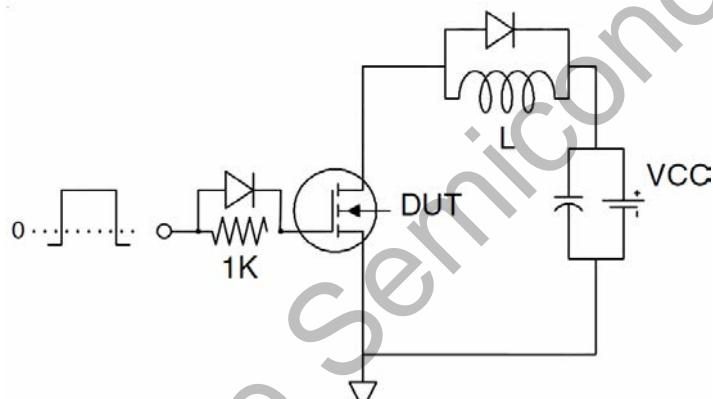
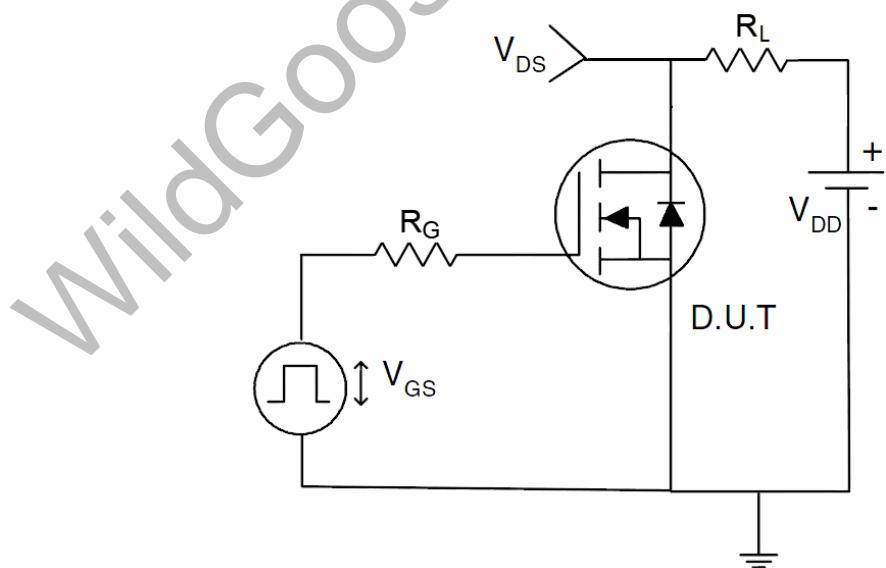
Figure 10  $V_{GS(\text{th})}$  vs Junction Temperature

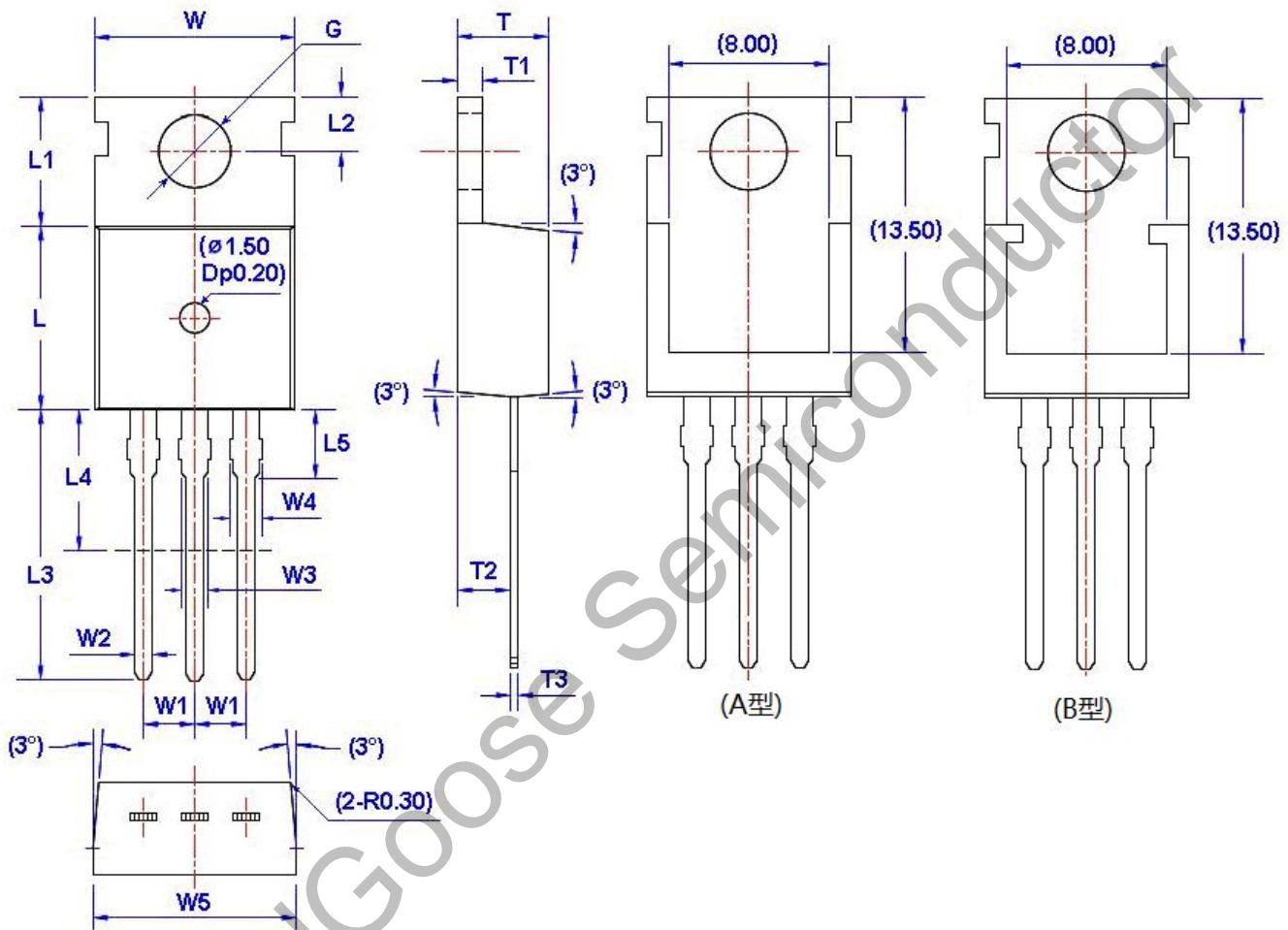
Figure 11 Normalized Maximum Transient Thermal Impedance

**Test Circuit****1) AS test Circuit****2) Gate charge test Circuit****3)witch Time Test Circuit**

Package Dimension

TO-220

Unit:mm



Symbol	Size		Symbol	Size		Symbol	Size		Symbol	Size	
	Min	Max		Min	Max		Min	Max		Min	Max
W	9.66	10.28	W5	9.80	10.20	L4**	6.20	6.60	T3	0.45	0.60
W1	2.54 (TYP)		L	9.00	9.40	L5	2.79	3.30	G(Φ)	3.50	3.70
W2	0.70	0.95	L1	6.40	6.80	T	4.30	4.70			
W3	1.17	1.37	L2	2.70	2.90	T1	1.15	1.40			
W4*	1.32	1.72	L3	12.70	14.27	T2	2.20	2.60			