1. DESCRIPTION

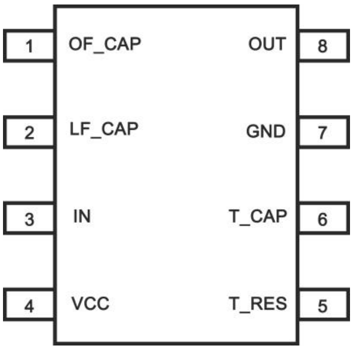
The XD567 and XL567 are general-purpose speech decoders designed to switch saturating transistors to ground when an input signal is present in the passband. The circuits contain I and Q detectors driven by a voltage controlled oscillator which determines the centre frequency of the decoder. External components are used to independently set the centre frequency, bandwidth and output delay.

2. FEATURES

- Frequency range of 20:1 (adjustable with external resistors)
- Logic-compatible output with 100mA sink current capability
- Bandwidth adjustable from 0% to 14%
- Effective suppression of out-of-band signals and noise
- Resistant to spurious signal interference
- Highly stable centre frequency
- Centre frequency adjustable from 0.01Hz to Adjustable centre frequency from 0.01Hz to 500kHz

3. PIN CONFIGURATIONS AND FUNCTIONS

XD567
XL567



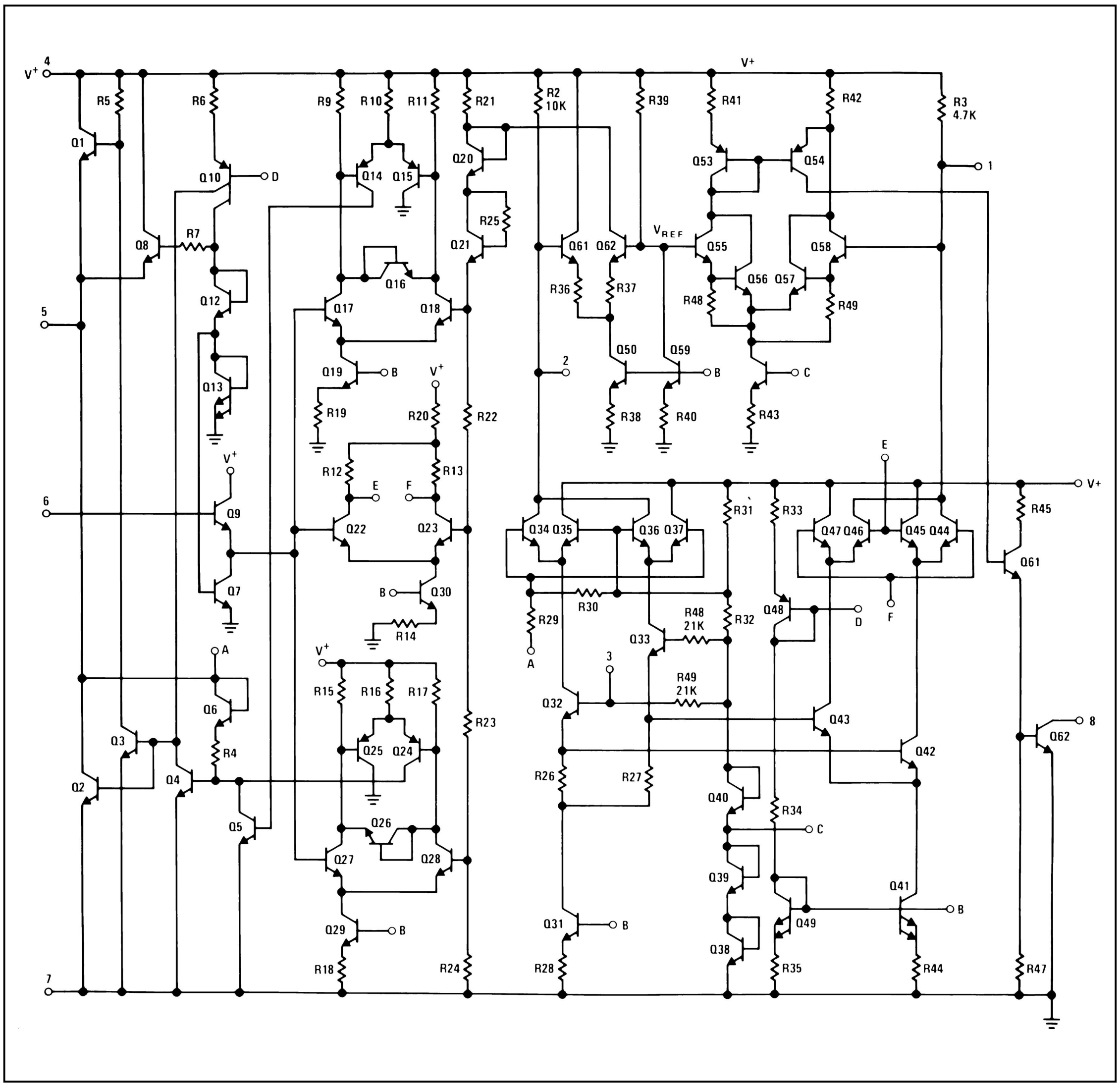
(Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OF_CAP	1	I	Output filter capacitor pin.
LF_CAP	2	I	Loop filter capacitor pin (LPF of the PLL).
IN	3	I	Device input.
VCC	4	P	Voltage supply pin.
T_RES	5	I	Timing resistor connection pin.
T_CAP	6	I	Timing capacitor connection pin.
GND	7	P	Circuit ground.
OUT	8	O	Device output.

4. FUNCTIONAL BLOCK DIAGRAM

The XL/XD567 is a general purpose tone decoder. The circuit consists of I and Q detectors driven by a voltage controlled oscillator which determines the center frequency of the decoder. This device is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. Center frequency is set by an external timing circuit composed by a capacitor and a resistor. Bandwidth and output delay are set by external capacitors.



Functional Block Diagram

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

			MIN	MAX	UNIT
Supply Voltage Pin				9	V
Power Dissipation(1)				1100	mW
V_8				15	V
V_3				−10	V
V_3				$V_4 + 0.5$	V
Operating Temperature Range	XL/XD567		0	70	℃
	DIP Package	Soldering (10 s)		260	℃
	SOP Package	Vapor Phase (60 s)		215	℃
		Infrared (15 s)		220	℃
Storage temperature range, T_{stg}			-50	150	℃

[1] Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Recommended Operating Conditions. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

5.2. Thermal Resistance Characteristics

THERMAL METRIC		XL/XD567		UNIT
		SOP	DIP	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	53.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.6	42.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	30.2	
ψ_{JT}	Junction-to-top characterization parameter	10.0	19.6	
ψ_{JB}	Junction-to-board characterization parameter	47.0	30.1	

5.3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	3.5	8.5	V
V_{IN}	Input Voltage Level	−8.5	8.5	V
T_A	Operating Temperature Range	0	70	℃

5.4. Electrical Characteristics

AC Test Circuit, TA = 25°C, V^+ = 5 V

PARAMETER	TEST CONDITIONS	XL/XD567			UNIT
		MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	10	mA
Power Supply Current Activated	R_L = 20k		11	15	mA
Input Resistance		18	20		k
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		6		dB
Largest Detection Bandwidth		12	14	16	% of f_o
Largest Detection Bandwidth Skew			1	2	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 – 6.75 V		±1	±2	%V
Highest Center Frequency		100	500		kHz
Center Frequency Stability (4.75 – 5.75 V)	0 < T_A < 70 55 < T_A < +125		35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75 V – 6.75 V 4.75 V – 9 V		0.5	1.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20		
Output Leakage Current	V_8 = 15 V		0.01	25	µA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0	V
Output Fall Time			30		ns
Output Rise Time			150		ns

[1] The maximum junction temperature of the XD567 and XL567 is 150°C. For operating at elevated temperatures, devices in the DIP package must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the SOP package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

5.5. Typical Characteristics

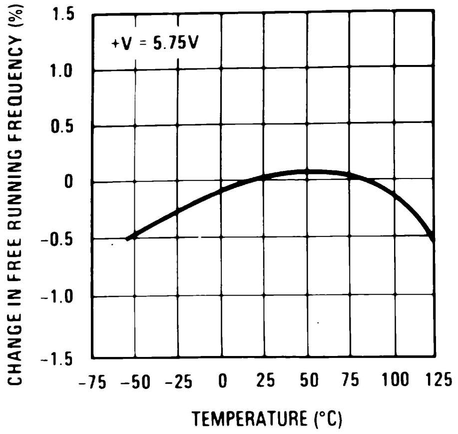


Figure 5-1. Typical Frequency Drift

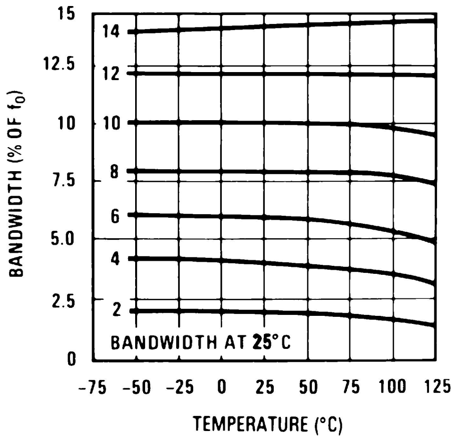


Figure5-2. Typical Bandwidth Variation

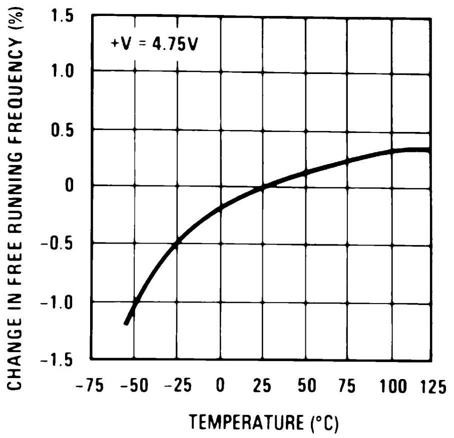


Figure 5-3. Typical Frequency Drift

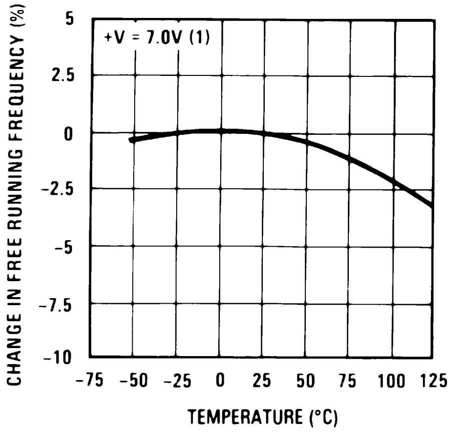


Figure 5-4. Typical Frequency Drift

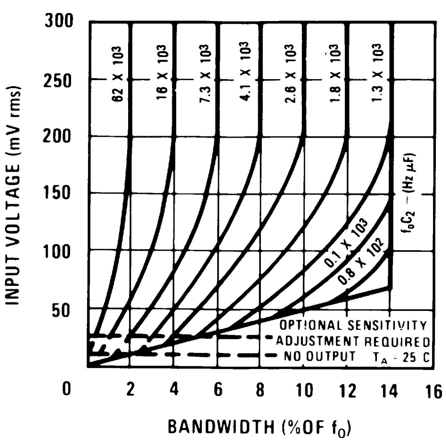


Figure 5-5. Bandwidth vs Input Signal Amplitude

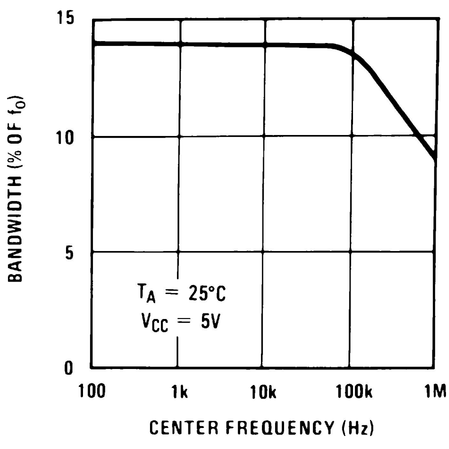


Figure 5-6. Largest Detection Bandwidth

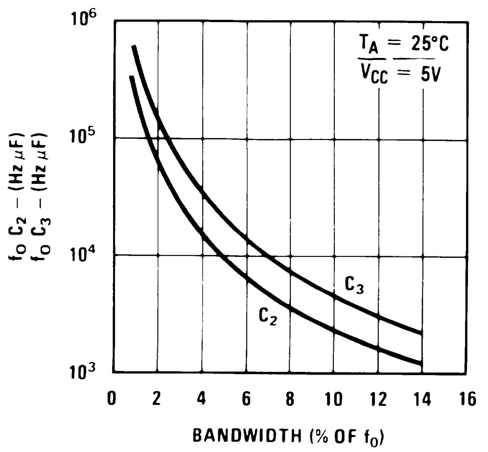


Figure 5-7. Detection Bandwidth as a Function of C_2 and C_3 vs

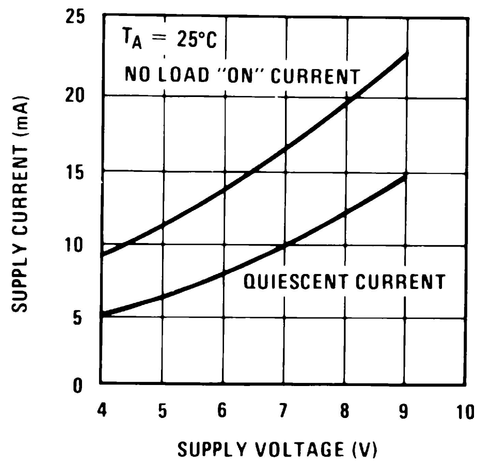


Figure 5-8. Typical Supply Current Supply Voltage

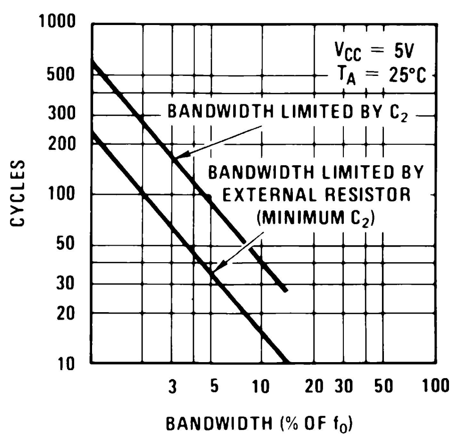


Figure 5-9. Greatest Number of Cycles Before Output

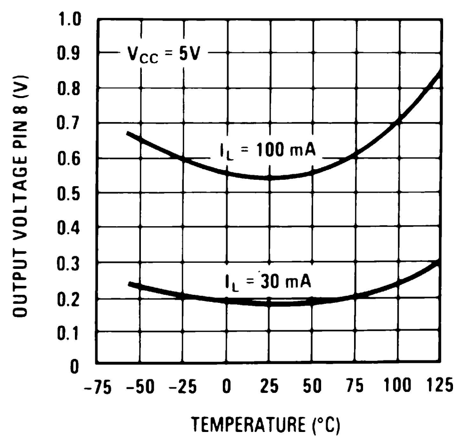


Figure 5-10. Typical Output Voltage vs Temperature

6. Parameter Measurement Information

All parameters are measured according to the conditions described in the Specifications section.

7. Detailed Description

7.1. Feature Description

7.1.1. Center Frequency

The center frequency of the XL/XD567 tone decoder is equal to the free running frequency of the voltage controlled oscillator. In order to set this frequency, external components should be placed externally. The component values are given by:

$$f_o \simeq 1 / (1.1 \times R_1 \times C_1)$$

where

- R1 = Timing Resistor
- C1 = Timing Capacitor

7.1.2. Output Filter

To eliminate undesired signals that could trigger the output stage, a post detection filter is featured in the XL/XD567. This filter consists of an internal resistor (4.7K-Ω) and an external capacitor. Although typically external capacitor value is not critical, it is recommended to be at least twice the value of the loop filter capacitor. If the output filter capacitor value is too large, the turn-on and turn off-time of the output will present a delay until the voltage across this capacitor reaches the threshold level.

7.1.3. Loop Filter

The phase locked loop (PLL) included in the XL/XD567 has a pin for connecting the low pass loop filter capacitor. The selection of the capacitor for the filter depends on the desired bandwidth. The device bandwidth selection is different according to the input voltage level. Refer to the Operation With Vi < 200m – VRMS section and the Operation With Vi > 200m – VRMS section for more information about the loop filter capacitor selection.

7.1.4. Logic Output

The XL/XD567 is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. The logic output is an open collector power transistor that requires an external load resistor that is used to regulate the output current level.

7.2. Device Functional Modes

7.2.1. Operation With Vi < 200m – VRMS

When the input signal is below a threshold voltage, typically 200m-VRMS, the bandwidth of the detection band should be calculated equation 2.

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

where

- Vi = Input voltage (volts rms), Vi ≤ 200mV
- C2 = Capacitance at Pin 2(μF)

7.2.2. Operation With Vi > 200m – VRMS

For input voltages greater than 200m-VRMS, the bandwidth depends directly from the loop filter capacitance and free running frequency product. Bandwidth is represented as a percentage of the free running frequency, and according to the product of f0·C2, it can have a variation from 2 to 14%. Table 9-2 shows the approximate values for bandwidth in function of the product result.

Table 7-2. Detection Bandwidth in Function of $f_o \times C_2$

$f_o \times C_2$ (kHzμF)	Bandwidth (% of f_o)
62	2
16	4
7.3	6
4.1	8
2.6	10
1.8	12
1.3	14
< 1.3	14

8. Application and Implementation

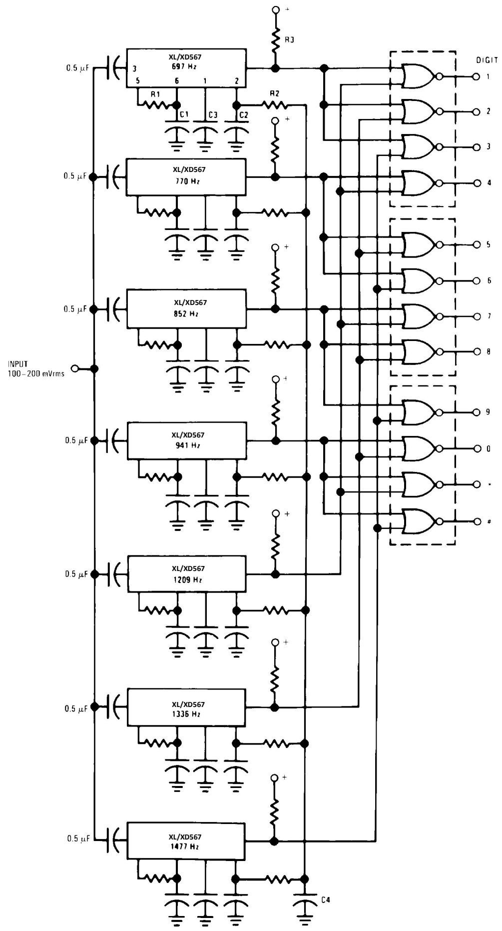
8.1. Application Information

The XL/XD567 tone decoder is a device capable of detecting if an input signal is inside a selectable range of detection. The device has an open collector transistor output, so an external resistor is required to achieve proper logic levels. When the input signal is inside the detection band, the device output will go to a LOW state. The internal VCO free running frequency establishes the detection band central frequency. An external RC filter is required to set this frequency. The bandwidth in which the device will detect the desired frequency depends on the capacitance of loop filter terminal. Typically a 1μF capacitor is connected to this pin. The device detection band has a different behavior for low and high input voltage levels. Refer to the Operation With Vi < 200m – VRMS section and the Operation With Vi > 200m – VRMS section for more information.

- Key tone decoding
- Precision Oscillator
- Frequency monitoring and control
- Wideband FSK modulation
- Ultrasonic control
- Carrier Current Remote Control
- Communication Paging Decoder

8.2. Typical Applications

8.2.1. Touch-Tone Decoder



Component values (typ) R1 6.8 to 15k R2 4.7k R3 20k C1 0.10 mfd C2 1.0 mfd 6V C3 2.2 mfd 6V C4 250 mfd 6V

Figure 8-1. Touch-Tone Decoder

8.2.2. Design Requirements

PARAMETERS	VALUES
Supply Voltage Range	3.5 V to 8.5 V
Input Voltage Range	20 mV_{RMS} to VCC + 0.5
Input Frequency	1 Hz to 500 kHz
Output Current	Max. 15 mA

8.2.3. Detailed Design Procedure

8.2.3.1 Timing Components

To calculate the timing components for an approximated desired central detection frequency (f0), the timing capacitor value (C1) should be stated in order to calculate the timing resistor value (R1). Typically for most applications, a 0.1-μF capacitor is used.

$$fo = 1 / (1.1 \times R1 \times C1) \quad (2)$$

8.2.3.2 Bandwidth

Detection bandwidth is represented as a percentage of f0. It can be selected based on the input voltage levels (Vi). For Vi < 200 mVRMS,

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o \quad (3)$$

For Vi > 200 mVRMS, refer to Table 7-2 or Figure 5-5.

8.2.3.3 Output Filter

The output filter selection is made considering the capacitor value to be at least twice the Loop filter capacitor.

$$C_3 \geqslant 2C_2 \quad (4)$$

8.2.3.4 Application Curve

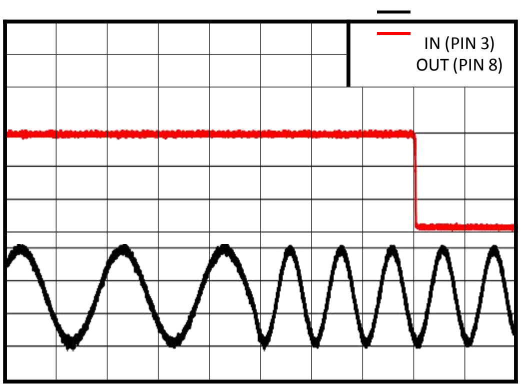
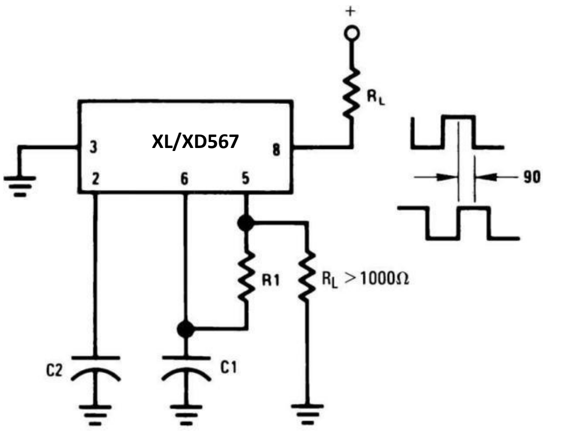


Figure 8-2. Frequency Detection

8.2.4. Oscillator with Quadrature Output



Connect Pin 3 to 2.8V to Invert Output

Figure 8-3. Oscillator with Quadrature Output

8.2.4.1 Design Requirements

Refer to the previous Design Requirements section.

8.2.4.2 Detailed Design Procedure

Refer to the previous Detailed Design Procedure section.

8.2.4.3 Application Curve

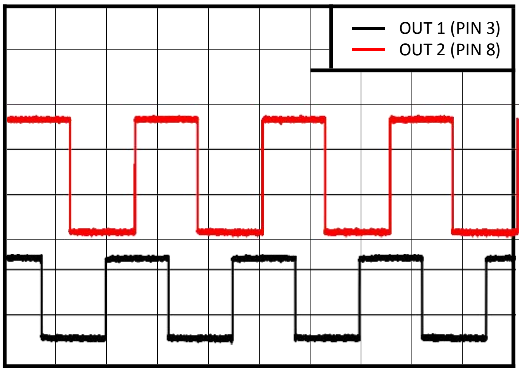


Figure 8-4. Quadrature Output

8.2.5. Oscillator with Double Frequency Output

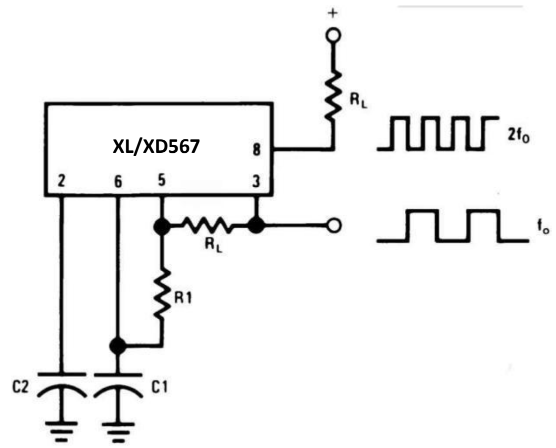


Figure 8-5. Oscillator with Double Frequency Output

8.2.5.1 Design Requirements

Refer to the previous Design Requirements section.

8.2.5.2 Detailed Design Procedure

Refer to the previous Detailed Design Procedure section.

8.2.5.3 Application Curve

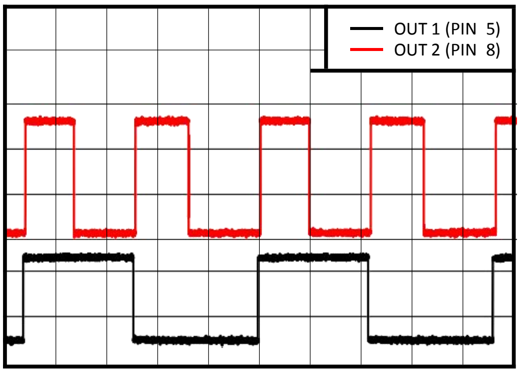


Figure 8-6. Double Frequency Output

8.2.6. Precision Oscillator Drive 100-mA Loads

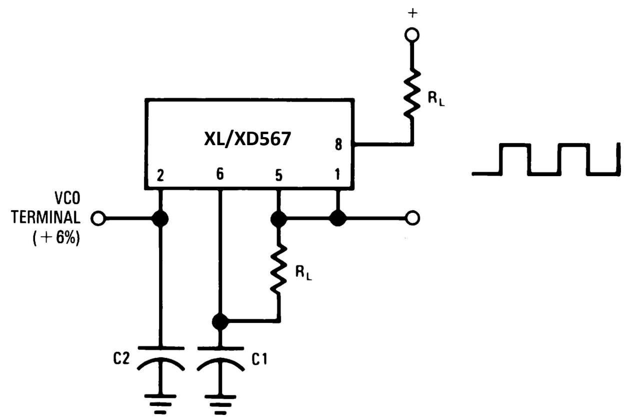


Figure 8-7. Precision Oscillator Drive 100-mA Loads

8.2.6.1 Design Requirements

Refer to the previous Design Requirements section.

8.2.6.2 Detailed Design Procedure

Refer to the previous Detailed Design Procedure section.

8.2.6.3 Application Curve

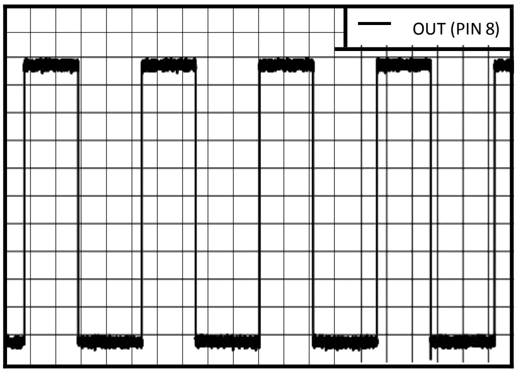
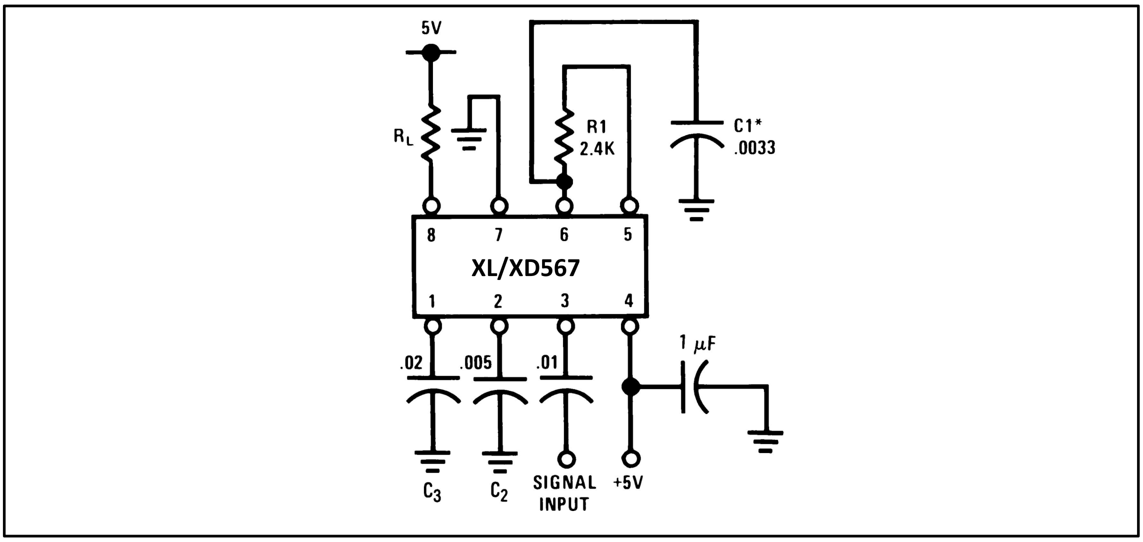


Figure 10-8. Output for 100-mA Load

8.2.7. AC Test Circuit



f_i = 100 kHz + 5 V

***Note:** Adjust for f_o = 100 kHz.

8.2.7.1. Design Requirements

Refer to the previous Design Requirements section.

8.2.7.2. Detailed Design Procedure

Refer to the previous Detailed Design Procedure section.

8.2.7.3. Application Curve

Refer to the previous Application Curve section.

9. Power Supply Recommendations

The XL/XD567 is designed to operate with a power supply up to 9 V. It is recommended to have a well regulated power supply. As the operating frequency of the device could be very high for some applications, the decoupling of power supply becomes critical, so is required to place a proper decoupling capacitor as close as possible to VCC pin.

9.1. Layout

9.1.1. Layout Guidelines

The VCC pin of the XL/XD567 should be decoupled to ground plane as the device can work with high switching speeds. The decoupling capacitor should be placed as close as possible to the device. Traces length for the timing and external filter components should be kept at minimum in order to avoid any possible interference from other close traces.

9.1.2. Layout Example

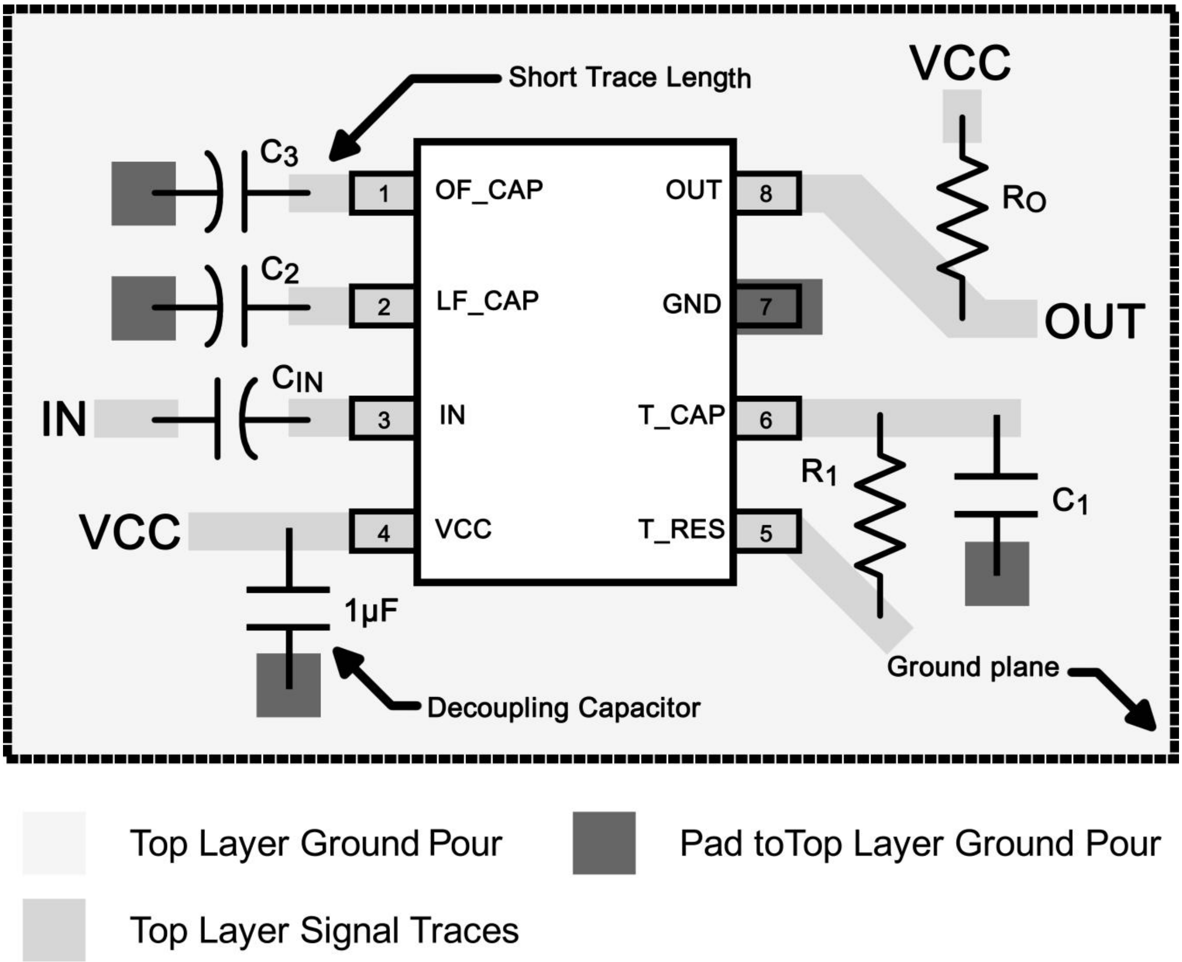


Figure 9-1. XL567 Layout Example

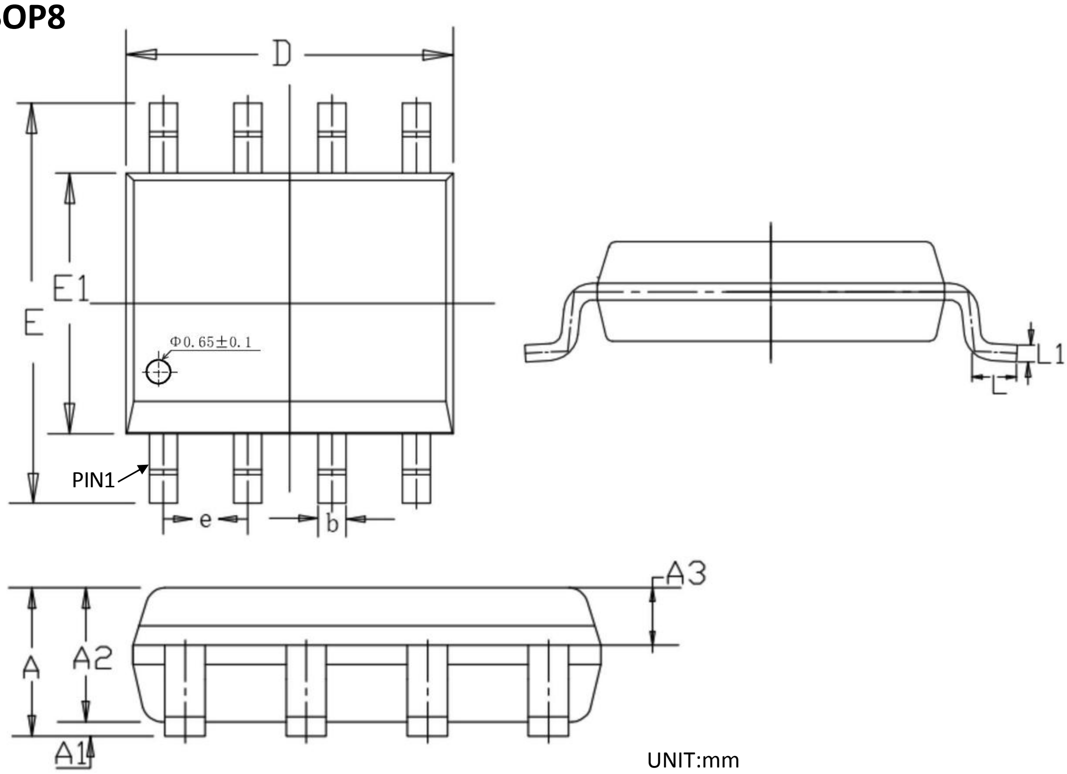
10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL567	XL567	SOP8	4.90 * 3.90	0 to +70	MSL3	T&R	2500
XD567	XD567	DIP8	9.25 * 6.38	0 to +70	MSL3	Tube 50	2000

11. DIMENSIONAL DRAWINGS

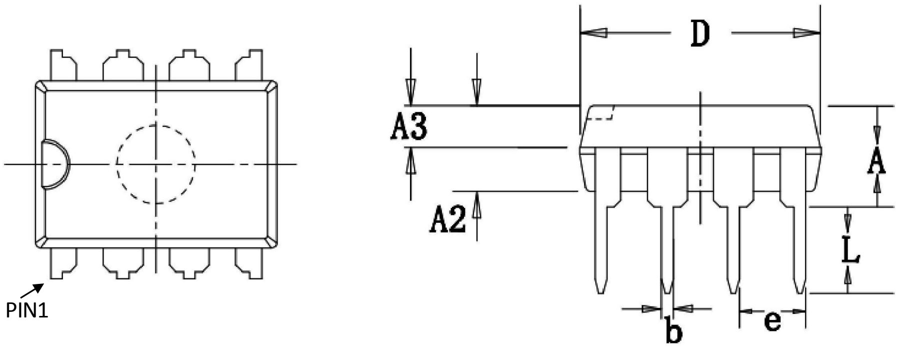
SOP8

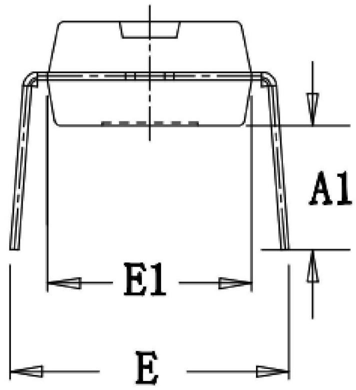


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–