1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Proprietary "SaΦic™" technology, a non-PLL phase controlled Active EMI management architecture
- Generates a 1X low EMI Phase Modulated replication of the input signal
- Vdd 1.65V - 2.0V 10 MHz to 38 MHz
- Vdd 2.5V - 3.6V 10 MHz to 38 MHz
- Multiple Deviation Selections
- Minimum frequency deviation selection capability
- Power Down Mode
- 8-pin WDFN package
- Supports automotive reliability standard: **AEC-Q100 Grade 1** and **Grade 2** certified

Product Description

The LX304 is a versatile 1x Active EMI management IC designed to provide system wide reduction of Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) from clock and data sources. The LX304 allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The LX30x family of mobile active EMI management ICs is unique in it's design and is based on LFC's proprietary "SaΦic" phase controlled Active EMI management technology. This allows operation on aperiodic as well periodic signals. By the precise placement of the edges of the reconstructed input signal, the peak energy of the output is distributed over a wider and controlled energy band thereby significantly lowering system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators.

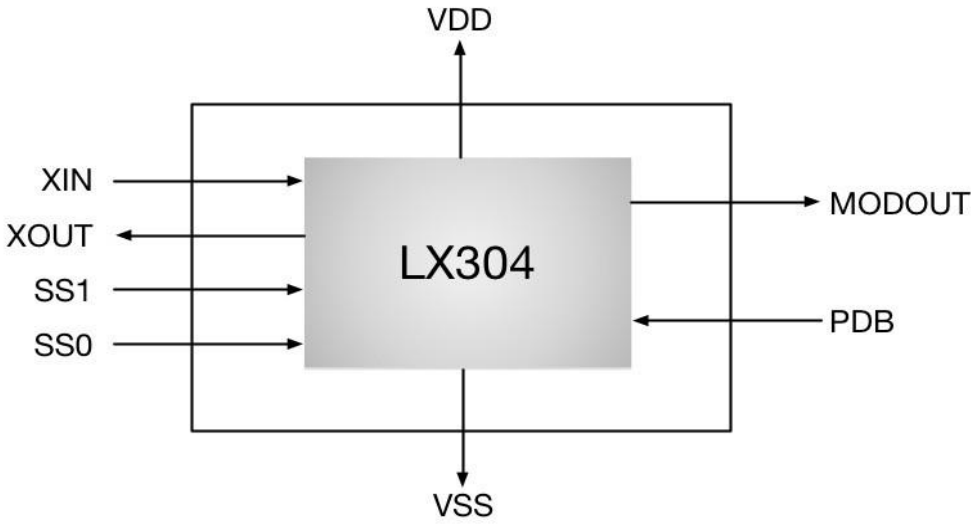
The LX304 has an input frequency range of 10 MHZ to 38MHz over a wide voltage range of 1.65V to 3.6V. The device can be placed in a "power save mode" by setting the PDB pin to GND where in it draws typically 40uA and also sets the MODOUT pin to a High-Z state. The device has two "deviation control pins" SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well as in system design.

The device is available in an 8 pin DFN package.

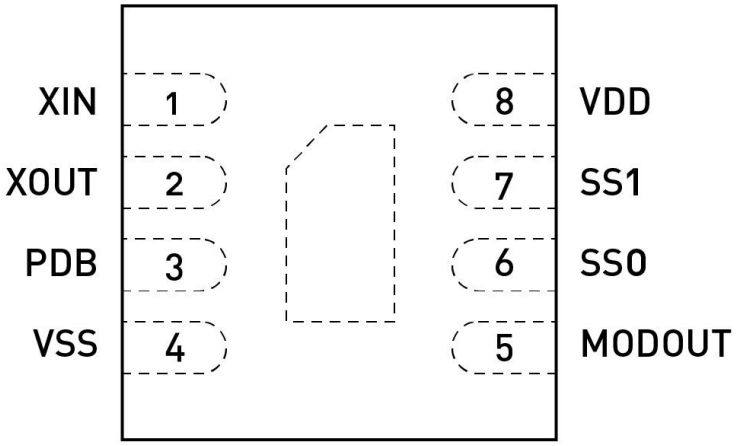
Applications

The LX304 is targeted towards mobile platforms such as cell phones, MIDs, notebooks and other "power and space" sensitive applications.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN	I	Crystal Oscillator Input.
2	XOUT	O	Crystal Oscillator Output.
3	PDB	I	Power Down pin. Active Low. Forces MODOUT to High-Z. Internal Pull-Up resistor.
4	VSS	P	System ground reference input.
5	MODOUT	O	1X phase modulated buffered output.
6	SS0	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Up Resistor. Recommend external Pull-Down Resistor 0Ω.
7	SS1	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Up Resistor. Recommend external Pull-Down Resistor 0Ω.
8	VDD	O	System Power Supply Pin.

Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD(3.3V)}$	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+125	°C
C_L	Load Capacitance		20	pF
C_{IN}	Input Capacitance		5	pF

Note: Please refer to ordering information for T_A

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{in}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_S	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied nor guaranteed for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Functional Table

Vdd(V)	Freq. Range (MHz)	Freq. (MHz)	Deviation (%)							
			SS1	SS0	SS1	SS0	SS1	SS0	SS1	SS0
			0	0	0	1	1	0	1	1
1.8	10~38	12	±0.11		±0.17		±0.21		±0.32	
1.8		24	±0.21		±0.32		±0.40		±0.62	
1.8		27	±0.23		±0.36		±0.45		±0.69	
1.8		37	±0.31		±0.49		±0.41		±0.66	
3.3	10~38	12	±0.06		±0.09		±0.11		±1.50	
3.3		24	±0.11		±0.15		±0.19		±0.29	
3.3		27	±0.12		±0.17		±0.22		±0.32	
3.3		37	±0.15		±0.24		±0.20		±0.31	

Note: Specified at VDD 1.8V/3.3V and room temperature. Frequency deviation can vary over voltage and temperature by +/-20%

DC Electrical Characteristics (3.3V +/-0.3V)

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IN}	Input HIGH Voltage			0.66*Vdd			V
V_{IL}	Input LOW Voltage					0.33*Vdd	V
I_{IH}	Input HIGH Current (pin 3/6/7)	V_{IN} = V_{DD}				10	µA
I_{IL}	Input LOW Current (pin 3/6/7)	V_{IN} = 0V				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		0.75*Vdd			V
V_{OL}	Output LOW Voltage	I_{OL} = +8mA				0.25*Vdd	V
I_{CC}	Static Supply Current	PDB = VSS			40	50	µA
I_{DD}	Dynamic Supply Current (SS1=1,SS0=1)	27MHZ	Unloaded		7.0	8.0	mA
			10pF load		8.0	9.0	
Z_O	Output Impedance				25		Ω

Switching Characteristics (3.3V +/-0.3V)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	38	MHz
MODOUT	Output Frequency		10	24	38	
T_d	Duty Cycle [1,2] = (t_2 / t_1) * 100	Measured at V_{DD} /2	45	50	55	%
T_3	Output Rise Time [1,2]	Measured between 20% to 80%	0.6	1.5	2.5	nS
T_4	Output Fall Time [1,2]	Measured between 80% to 20%	0.6	1.5	2.5	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27 MHz		+/-250		pS

Notes:
1. All parameters specified with 27MHz without loaded outputs and VDD 3.3V
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

DC Electrical Characteristics (1.8V +/-0.15V)

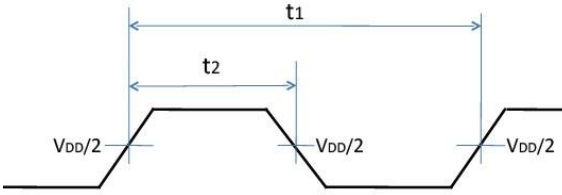
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			1.65	1.8	1.95	V
V_{IH}	Input HIGH Voltage			0.66*Vdd			V
V_{IL}	Input LOW Voltage					0.33*Vdd	V
I_{IH}	Input HIGH Current (pins 3/6/7)	V_{IN} = V_{DDDD}				10	µA
I_{IL}	Input LOW Current (pins 3/6/7)	V_{IN} = 0V				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA		0.75*Vdd			V
V_{OL}	Output LOW Voltage	I_{OL} = +4mA				0.25*Vdd	V
I_{CC}	Static Supply Current	PDB = VSS			20	30	µA
I_{DD}	Dynamic Supply Current (SS1=1,SS0=0)	27MHZ	Unloaded		3.0	4.0	mA
			10pF load		3.5	4.5	
Z_O	Output Impedance				25		Ω

Switching Characteristics (1.8V +/-0.15V)

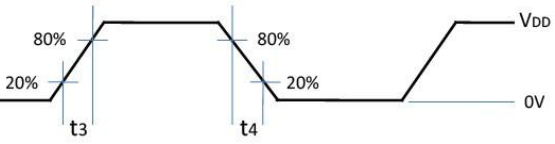
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	38	MHz
MODOUT	Output Frequency		10	24	38	
T_d	Duty Cycle [1,2] = (t_2 / t_1) * 100	Measured at V_{DD} /2	45	50	55	%
t_3	Output Rise Time [1,2]	Measured between 20% to 80%	1.0	2.0	3.0	nS
t_4	Output Fall Time [1,2]	Measured between 80% to 20%	1.0	2.0	3.0	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27 MHz		+/-250		pS

Notes:
1. All parameters specified with 27MHz without loaded outputs and VDD 1.8V
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

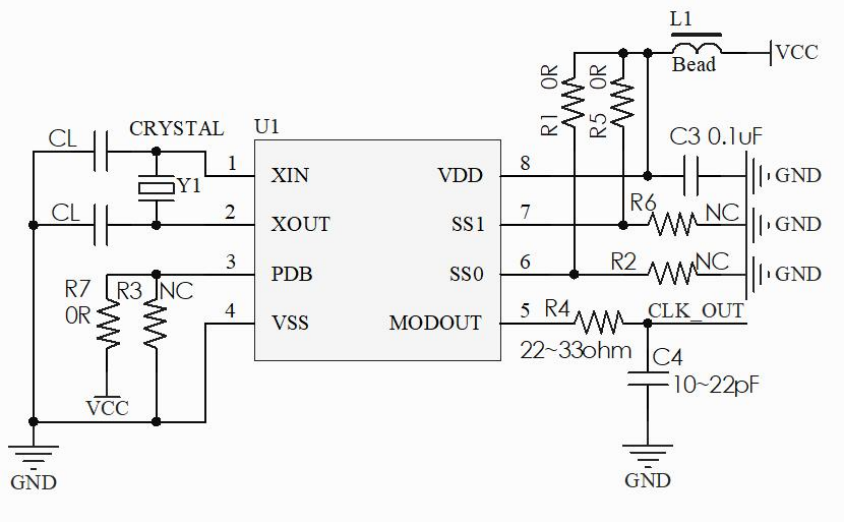
Duty Cycle Timing



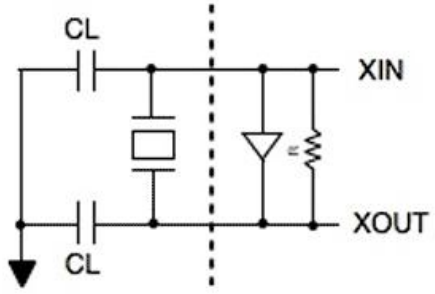
All Outputs Rise/Fall Time



Application Schematic

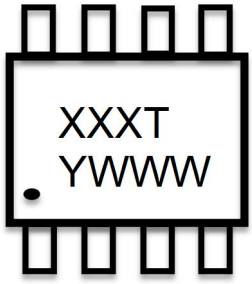


Crystal Oscillator Circuit



CL=2x(Cp-Cs)
Cp: load capacitance of Crystal
Cs: Stray capacitance (PCB trace + Input cap. of IC)

Marking Information



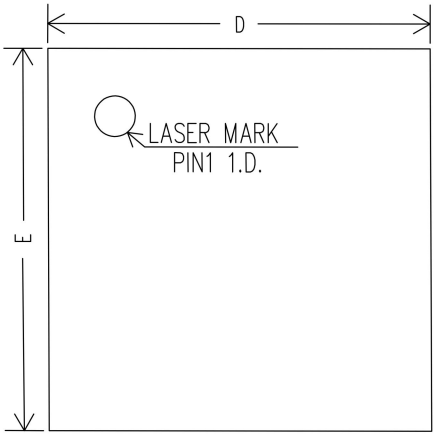
XXX: Part Number
T: Temperature Grade
Y: Year of Production
WWW: Work Order No.

Ordering Information

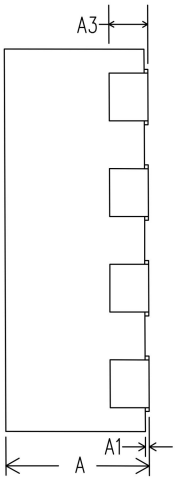
Part Number	Temp. Grade Indicator	Temp Grade	Temp Range	IC Marking	IC Package	Tape & Reel
LX304C	C	Commercial	0°~70°C	304C	2mm x 2mm 8L WDFN	4,000pcs/Reel
LX304I	I	Industrial	-20°~85°C	304I		
LX304E	E	Automotive AEC Q100 Grade 2	-40°~105°C	304E		
LX304A	A	Automotive AEC Q100 Grade 1	-40°~125°C	304A		

Package Dimension

WDFN



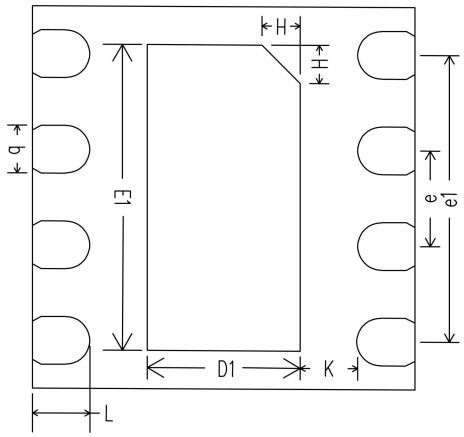
TOP VIEW



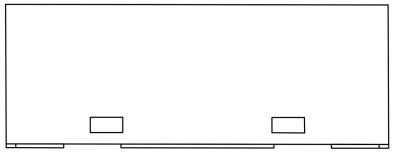
SIDE VIEW

COMMON DEMENSIONS
(UNITS OF MEASURE = MILLIMETER

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
B	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	0.75	0.80	0.85
E1	1.55	1.60	1.65
e	0.40	0.50	0.60
E1	1.40	1.50	1.60
H		0.20REF	
K	0.20	0.30	0.40
L	0.25	0.30	0.35



BOTTOM VIEW



SIDE VIEW

Revision History

Revision Number	Date of Release	Changes
2.1	3/1/2019	1) Input frequency range 2) AC Characteristics 3) Device Marking Spec 4) Addition of AEC-Q100 Grade 1 & Grade 2
2.2	8/20/2019	1) Add +/- tolerance 0.05mm to package dimension D and E
2.3	11/26/2019	1) Deviation updates
2.4	7/16/2020	1) t_3/t_4 updates
2.5	5/13/2021	1) Update D2, L and E2 package dimension
2.6	9/24/2021	1) Application schematic update 2) Static current update 3) PDB pin update 4) SS1 pin update
2.7	7/23/2023	1) Update the application schematic 2) Update the deviation

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