EMI Reduction Oscillator

## Features

- FCC approved method of EMI attenuation
- Proprietary SaΦic™ technology, a non-PLL phase modulation implementation and algorithm Supply
- Voltage 1.65V~1.95V
- Frequency range 20~30Mhz
- CMOS Output
- Modulated clock output Enable/Disable Function
- Low EMI buffer for enhanced EMI reduction
- RoHS compliant & Pb free
- Products available in AEC-Q100 compliant
- Package 2.5x2.0mm, 3.2x2.5mm

## Applications

- SATA, Ethernet, PCI express, Video, Wireless
- Computing, Storage, Networking, Telecom, Industrial Control

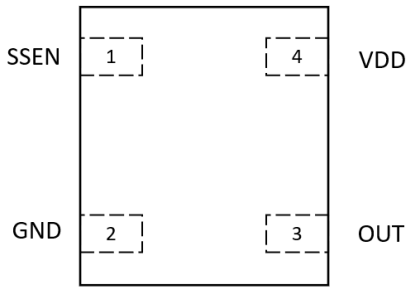
## Table1. Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit. | Condition |
|---|---|---|---|---|---|---|
| Output Frequency Range | F | 20 | - | 30 | MHz | $V_{DD}$=1.8V |
| Frequency Stability | F_stab | -30 | | +30 | PPM | Inclusive of initial tolerance at 25 ºC，and variations over operating temperature, rated power supply voltage and load. |
| | | -50 | | +50 | | |
| | | -60 | | +60 | | |
| | | -100 | | +100 | | |
| Operating Temperature Range | $T_{USE}$ | -40 | | +125 | ºC | |
| Supply Volage | $V_{DD}$ | 1.65 | 1.8 | 1.95 | V | |
| Output Load | $C_L$ | | | 9 | pF | |
| Current Consumption | $I_{DD}$ | - | 4.0 | 5.0 | mA | 9pF Load, f=27MHz, $V_{DD}$ =1.8V |
| SSEN mode current | $I_{SS}$ | | 3.0 | 3.5 | mA | When SSEN=GND, 9pF Load, f=27MHz, $V_{DD}$ =1.8V output is Pulled Down |
| Duty Cycle | DC | 45 | | 55 | % | |
| Rise/Fall Time | $T_r$ | 5.5 | 6.0 | 7.0 | nS | 9pF load, 10%~90% $V_{DD}$, high drive ($V_{DD}$=1.8V) |
| | $T_f$ | 6.0 | 6.5 | 7.5 | nS | |
| Output Voltage High | $V_{OH}$ | 0.75* $V_{DD}$ | - | - | V | $I_{OH}$=-4mA, $I_{OL}$=4mA |
| Output Voltage Low | $V_{OL}$ | - | - | 0.25* $V_{DD}$ | V | |
| Input Voltage High | $V_{IH}$ | 0.66* $V_{DD}$ | - | - | V | |
| Input Volage Low | $V_{IL}$ | - | - | 0.33* $V_{DD}$ | V | |
| Startup Time | $T_{\_start}$ | - | | 1 | mS | Measure from the time $V_{DD}$ reaches its rated minimum value. |
| RMS Phase Jitter | $T_{\_phj}$ | - | 0.63 | | pS | F=27MHz, integration bandwidth=12KHz to 5MHz, SSEN=GND |
| First year Aging | $F_{\_aging}$ | -1.5 | | +1.5 | PPM | 25 ºC |
| 10-year Aging | | -3 | | +3 | PPM | |

## Table2. Pin Configuration

| Pin | Symbol | Functionality | |
|---|---|---|---|
| 1 | SSEN | Input | Modulation Output Clock Mode Enable Pin<br>H (Logic "1"): Enable<br>L (Logic "0"): Disable<br>Internal pull-high resistor |
| 2 | GND | Power | Electrical ground |
| 3 | OUT | Output | Phase modulated buffered output |
| 4 | VDD | Power | Power supply voltage |

**TOP View**




## Table3. Deviation select Table

| Deviation Select | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Frequency | Deviation | | | |
| 24MHz | ±0.61% | ±0.39% | ±0.28% | ±0.22% |
| 25MHz | ±0.66% | ±0.41% | ±0.30% | ±0.23% |
| 27MHz | ±0.72% | ±0.46% | ±0.34% | ±0.27% |

Notes：1. Please refer to ordering information for deviation select

## Test Circuit and Waveform

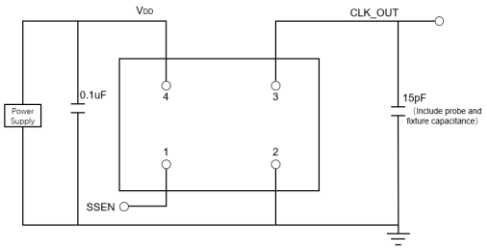



Figure 1. Test Circuit

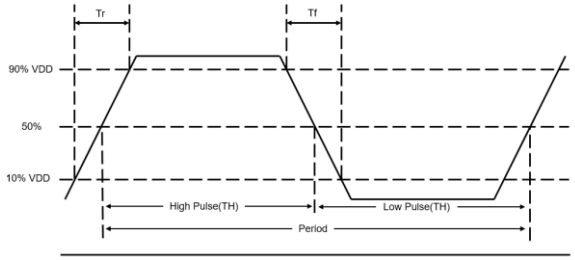
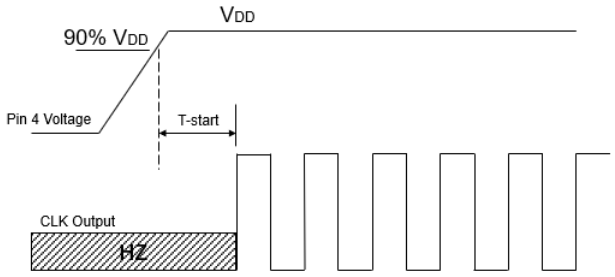



Figure 2. Waveform

Notes:2. Duty Cycle is computed as Duty Cycle = TH/Period.

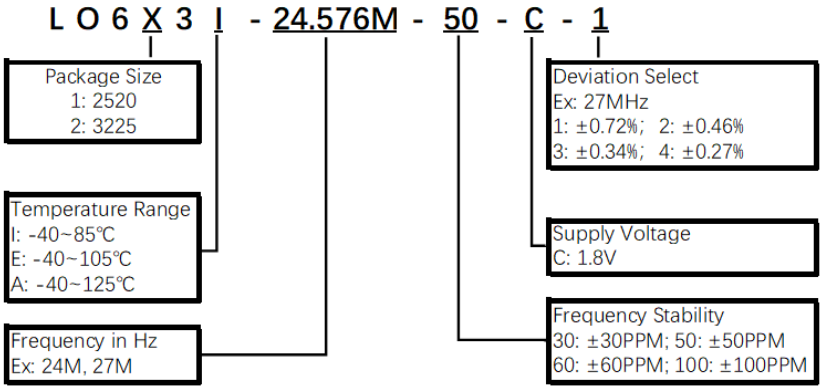
## Timing Diagram



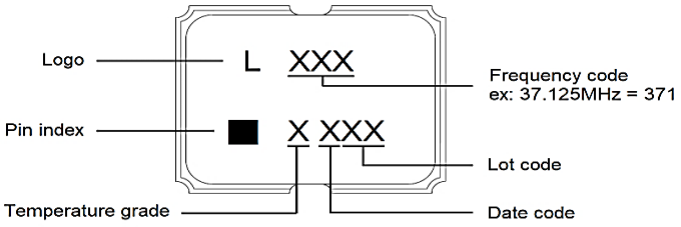

T-start: Time to start from power-off

Figure 3. Startup Timing

## Ordering Information



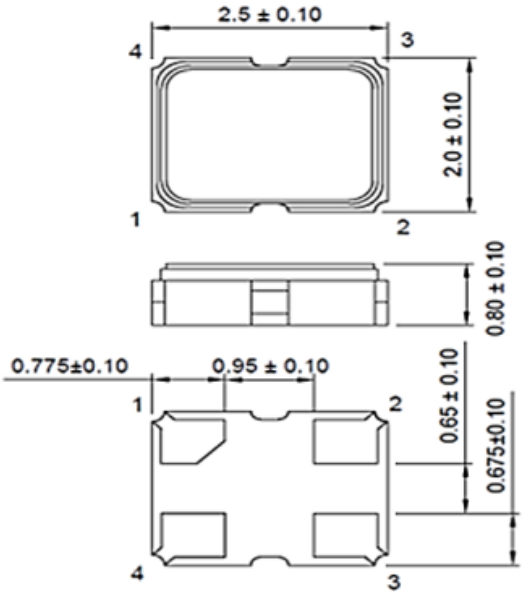

## Marking




| Temperature Grade | Temperature Range | Frequency Stability (PPM) |
|---|---|---|
| I | -40~85℃ | ±30 |
| E | -40~105℃ | ±50 / ±60 |
| A | -40~125℃ | ±50 / ±100 |

## Dimensions

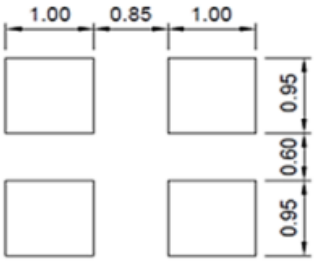
### 2520




**Pad Function**

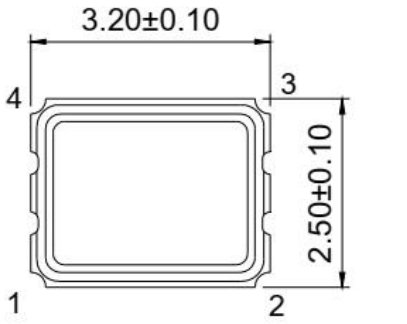
1 EN
2 GND
3 OUTPUT
4 VDD

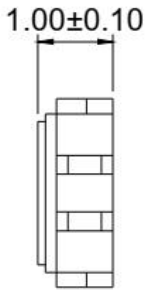
**Suggested Layout**



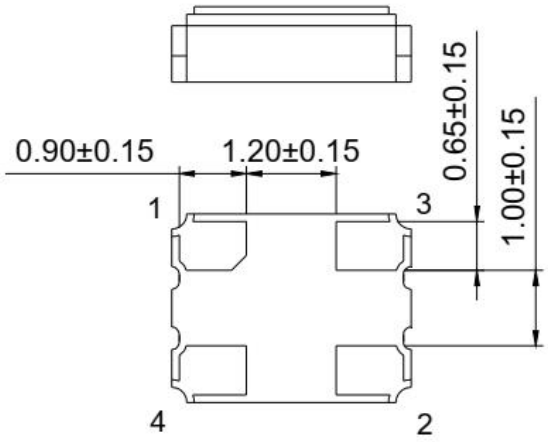

(Unit: mm)

### 3225

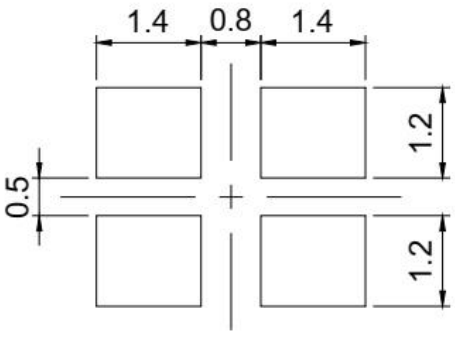



PAD FUNCTION:
1: ENABLE CONTROL
2: GND
3: OUT
4: VDD




Suggested Layout



## Revision History

| Revision Number | Date of Release | Changes |
|---|---|---|
| 1.0 | 04/07/2021 | 1) Preliminary datasheet |
| 1.1 | 06/01/2021 | 1) Modify Pin1 function，frequency range, Tr, Tf. |
| 1.2 | 06/07/2021 | 1) Modify $I_{DD}$, $I_{SS}$ |
| 1.3 | 10/12/2021 | 1) Add Dimensions |
| 1.4 | 11/30/2021 | 1) Delete 2016 package, add 3225 package |