TW2868

FN7796
Rev. 3.00
May 22, 2013

8-Channel Video Decoders and Audio Codecs and Video Encoder for Security Applications

The TW2868 includes eight high quality NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data for security applications. Each channel contains 10-bit ADC and proprietary clamp and gain controllers and utilizes 4H comb filter for separating luminance and chrominance to reduce cross noise artifacts. The TW2868 adopts image enhancement techniques, such as IF compensation filter, CTI and programmable peaking. TW2868 also includes one NTSC/PAL video encoder with two 10-bit DAC's to support CVBS and YC output. The TW2868 also includes audio CODEC, which has ten audio Analog-to-Digital converter processing and one Digital-to-Analog converter. A built-in audio controller can generate digital outputs for recording/mixing and it also accepts digital input for playback.

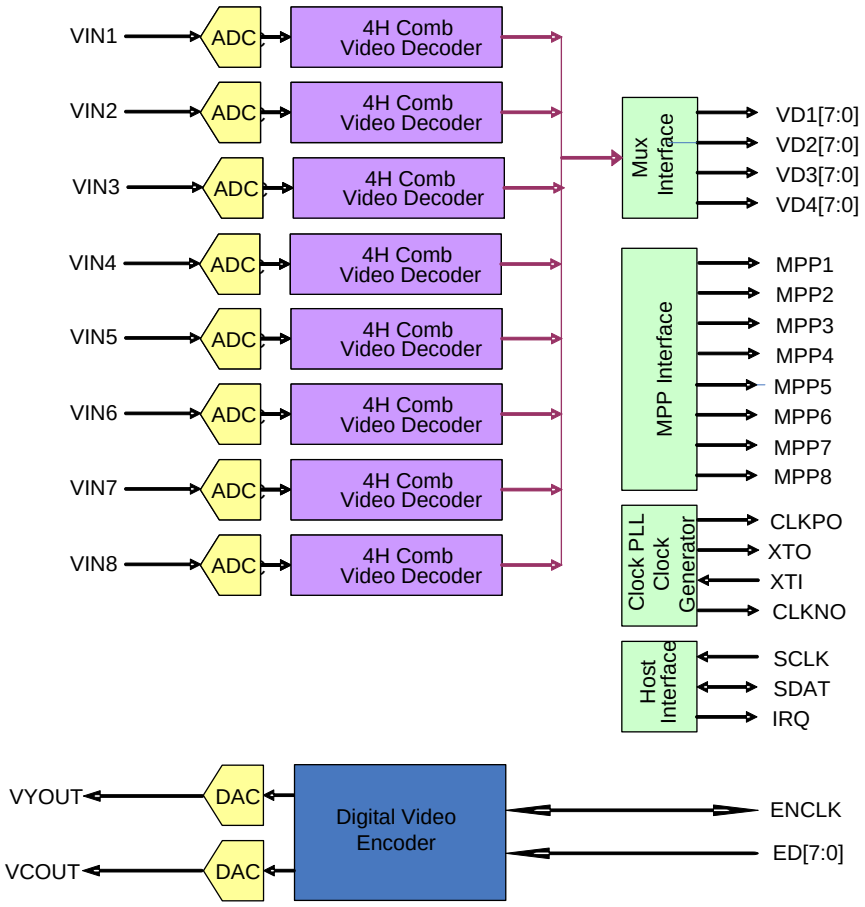
Features

- Accepts all NTSC(M/4.43) / PAL(B/D/G/H/I/K/L/M/N/60)/SECAM standards with auto detection
- Integrated eight video analog anti-aliasing filters and 10 bit CMOS ADCs
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system
- Supports ITU-R BT.656 type time multiplexed output with 54/108MHz
- Provides simultaneous 2x four channel Full D1 with 108MHz and 2x CIF with 54MHz by time-multiplexed output format
- Integrated ten audio ADC processing and one audio DAC
- Provides multi-channel audio mixed analog output
- Supports I2S/DSP Master/Slave interface for record output and playback input
- PCM 8/16-bit and μ-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate, which covers popular frequencies of 8/16/32/44.1/48kHz
- Supports two-wire serial host interface
- Integrated one video encoder and two10-bit video CMOS DACs
- Integrated clock PLL for 108MHz clock output
- Ultra low power consumption (Typical 867.36mW)
- 128 pin LQFP package

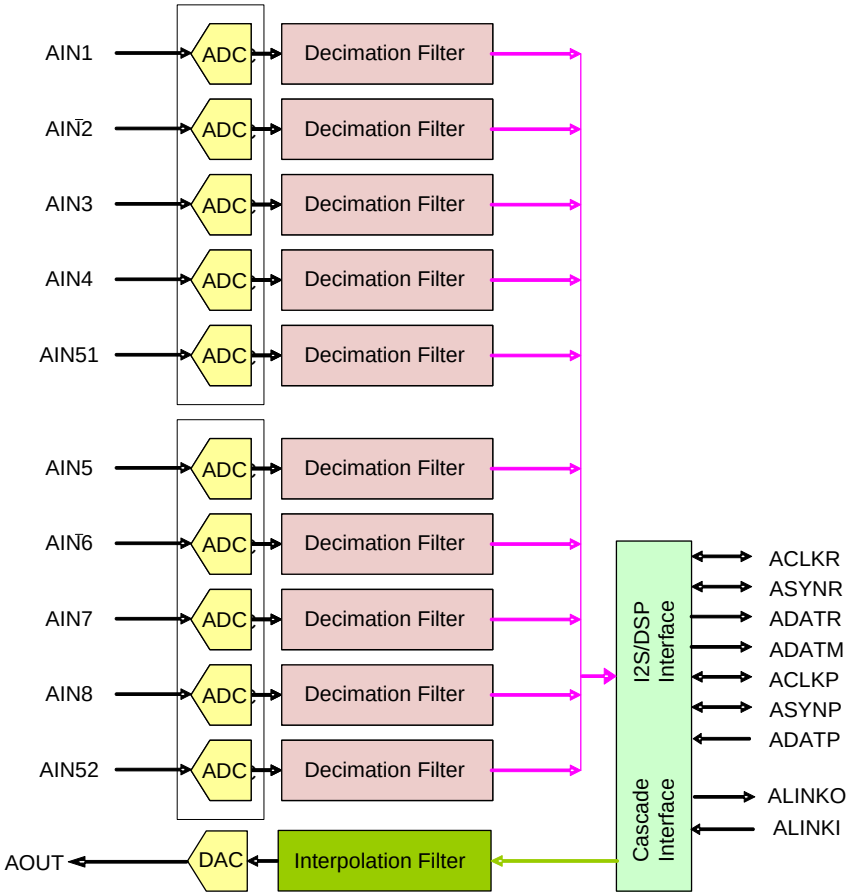
Table of Contents

Block Diagram

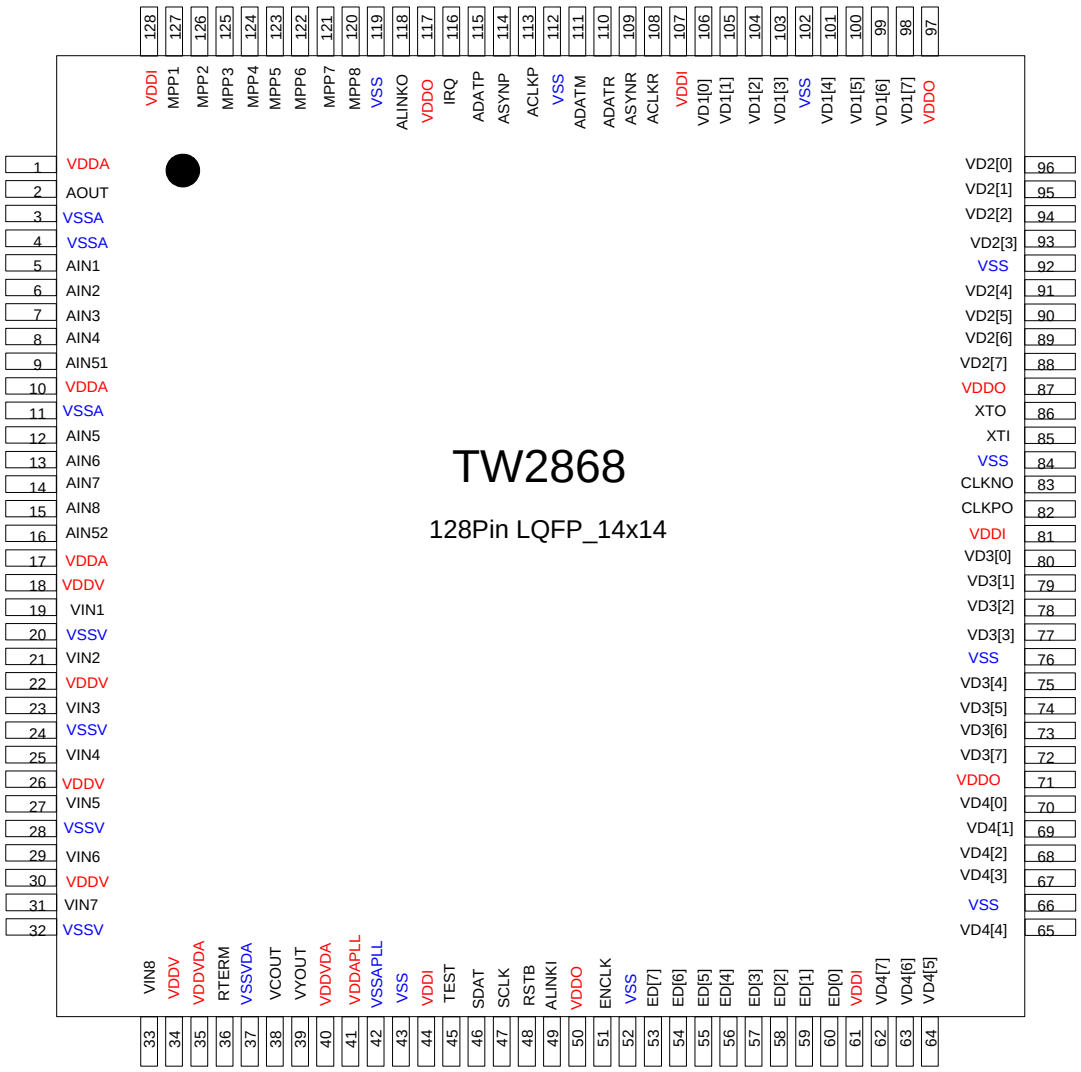
Video, Clock and Host Interface



Audio


AIN1
AIN2
AIN3
AIN4
AIN51
AIN5
AIN6
AIN7
AIN8
AIN52
ADC
Decimation Filter
DAC
Interpolation Filter
AOUT
I2S/DSP Interface
Cascade Interface
ACLKR
ASYNR
ADATR
ADATM
ACLKP
ASYNP
ADATP
ALINKO
ALINKI

Pin Diagram


TW2868
128Pin LQFP_14x14
1 VDDA
2 AOUT
3 VSSA
4 VSSA
5 AIN1
6 AIN2
7 AIN3
8 AIN4
9 AIN51
10 VDDA
11 VSSA
12 AIN5
13 AIN6
14 AIN7
15 AIN8
16 AIN52
17 VDDA
18 VDDV
19 VIN1
20 VSSV
21 VIN2
22 VDDV
23 VIN3
24 VSSV
25 VIN4
26 VDDV
27 VIN5
28 VSSV
29 VIN6
30 VDDV
31 VIN7
32 VSSV
33 VIN8
34 VDDV
35 VDDVDA
36 RTERM
37 VSSVDA
38 VCOUT
39 VYOUT
40 VDDVDA
41 VDDAPLL
42 VSSAPLL
43 VSS
44 VDDI
45 TEST
46 SDAT
47 SCLK
48 RSTB
49 ALINKI
50 VDDO
51 ENCLK
52 VSS
53 ED[7]
54 ED[6]
55 ED[5]
56 ED[4]
57 ED[3]
58 ED[2]
59 ED[1]
60 ED[0]
61 VDDI
62 VD4[7]
63 VD4[6]
64 VD4[5]
65 VD4[4]
66 VSS
67 VD4[3]
68 VD4[2]
69 VD4[1]
70 VD4[0]
71 VDDO
72 VD3[7]
73 VD3[6]
74 VD3[5]
75 VD3[4]
76 VSS
77 VD3[3]
78 VD3[2]
79 VD3[1]
80 VD3[0]
81 VDDI
82 CLKPO
83 CLKNO
84 VSS
85 XTI
86 XTO
87 VDDO
88 VD2[7]
89 VD2[6]
90 VD2[5]
91 VD2[4]
92 VSS
93 VD2[3]
94 VD2[2]
95 VD2[1]
96 VD2[0]
97 VDDO
98 VD1[7]
99 VD1[6]
100 VD1[5]
101 VD1[4]
102 VSS
103 VD1[3]
104 VD1[2]
105 VD1[1]
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107 VDDI
108 ACLKR
109 ASYNR
110 ADATR
111 ADATM
112 VSS
113 ACLKP
114 ASYNP
115 ADATP
116 IRQ
117 VDDO
118 ALINKO
119 VSS
120 MPP8
121 MPP7
122 MPP6
123 MPP5
124 MPP4
125 MPP3
126 MPP2
127 MPP1
128 VDDI

Pin Descriptions

ANALOG VIDEO/AUDIO INTERFACE PINS

NAME	NUMBER	TYPE	DESCRIPTION
VIN1	19	A	Composite video input of channel 1.
VIN2	21	A	Composite video input of channel 2.
VIN3	23	A	Composite video input of channel 3.
VIN4	25	A	Composite video input of channel 4.
VIN5	27	A	Composite video input of channel 5.
VIN6	29	A	Composite video input of channel 6.
VIN7	31	A	Composite video input of channel 7.
VIN8	33	A	Composite video input of channel 8.
VCOUT	38	A	Analog video output.
VYOUT	39	A	Analog video output.
RTERM	36	A	Analog video DAC resistance term.
AIN1	5	A	Audio input of channel 1.
AIN2	6	A	Audio input of channel 2.
AIN3	7	A	Audio input of channel 3.
AIN4	8	A	Audio input of channel 4.
AIN51	9	A	Audio input of channel 51.
AIN5	12	A	Audio input of channel 5.
AIN6	13	A	Audio input of channel 6.
AIN7	14	A	Audio input of channel 7.
AIN8	15	A	Audio input of channel 8.
AIN52	16	A	Audio input of channel 52.
AOUT	2	A	Analog Audio output.

DIGITAL VIDEO/AUDIO INTERFACE PINS

NAME	NUMBER	TYPE	DESCRIPTION
VD1[7:0]	98,99,100,101, 103,104,105,106	O	Video data output of channel 1.
VD2[7:0]	88,89,90,91, 93,94,95,96	O	Video data output of channel 2.
VD3[7:0]	72,73,74,75, 77,78,79,80	O	Video data output of channel 3.
VD4[7:0]	62,63,64,65, 67,68,69,70	O	Video data output of channel 4.
MPP1	127	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 1.
MPP2	126	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 2.
MPP3	125	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 3.
MPP4	124	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 4.
MPP5	123	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 5.
MPP6	122	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 6.
MPP7	121	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 7.
MPP8	120	O	GPO/HS/VS/FLD/ACTIVE/NOVID of channel 8.
ED[7:0]	53,54,55,56, 57,58,59,60	I	ITU-R656 Video data input.
ACLKR	108	IO	Audio serial clock input/output of record.
ASYNR	109	IO	Audio serial sync input/output of record.
ADATR	110	O	Audio serial data output of record.
ADATM	111	O	Audio serial data output of mixing.
ACLKP	113	IO	Audio serial clock input/output of playback.
ASYNP	114	IO	Audio serial sync input/output of playback.
ADATP	115	I	Audio serial data input of playback.
ALINKI	49	I	Audio Multi-chip operation serial input.
ALINKO	118	O	Audio Multi-chip operation serial output.

SYSTEM CONTROL PINS

NAME	NUMBER	TYPE	DESCRIPTION
RSTB	48	I	System reset.
XTI	85	I	Crystal 27MHz/54MHz connection or 27MHz/54MHz/108MHz clock input.
XTO	86	O	For crystal 27MHz/54MHz connection.
CLKPO	82	O	27/54/108MHz clock output.
CLKNO	83	O	27/54/108MHz clock output.
ENCLK	51	I/O	Input/output clock for ED[7:0] video data input.
TEST	45	I	Test pin. Connect to ground.
SCLK	47	I	Serial control clock line.
SDAT	46	IO	Serial control data line.
IRQ	116	O	Interrupt request output.

POWER AND GROUND PINS

NAME	NUMBER	TYPE	DESCRIPTION
VDDI	44,61,81,107,128	P	1.2V Power for internal logic.
VDDO	50,71,87,97, 117	P	3.3V Power for output driver.
VSS	43,52,66,76,84, 92,102,112,119	G	Ground for internal logic and output driver.
VDDV	18,22,26,30,34	P	3.3V Power for analog video ADC.
VSSV	20,24,28,32	G	Ground for analog video ADC.
VDDVDA	35,40	P	3.3V Power for analog video DAC.
VSSVDA	37	G	Ground for analog video DAC.
VDDA	1,10,17	P	3.3V Power for analog audio.
VSSA	3,4,11	G	Ground for analog audio.
VDDAPLL	41	P	3.3V Power for clock PLL.
VSSAPLL	42	G	Ground for clock PLL.

Ordering Information

PART NUMBER (Note Note:)	PART MARKING	PACKAGE (Pb-free)	PKG DWG. #
TW2868-LA2CR	**TW2868 LA2-CR**	**128 Ld LQFP (14mmx14mm)**	**Q128.14x14**

NOTE:

1. **These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.**

Functional Description

Video Input Formats

The TW2868 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW2868 supports all common video formats as shown in Table 1.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW2868

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Analog Frontend

The TW2868 contains eight 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the V_ADC_PWDN register. The TW2868 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. The following Figure 1 shows the frequency response of the anti-aliasing filter.

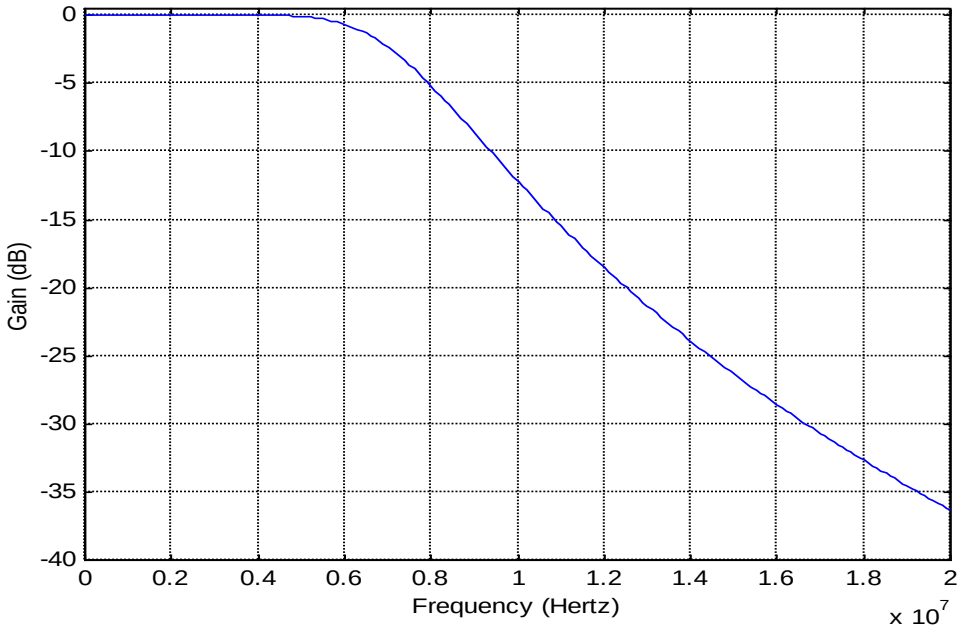


FIGURE 1. THE FREQUENCY RESPONSE OF ANTI-ALIASING FILTER

DECIMATION FILTER

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. Figure 2 shows the characteristic of the decimation filter.

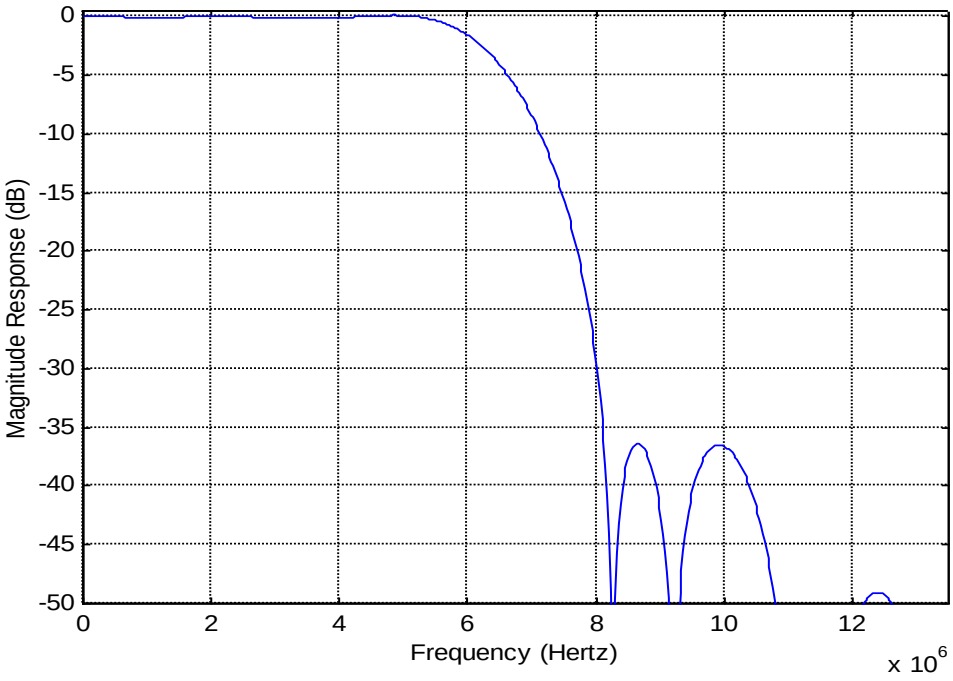


FIGURE 2. THE CHARACTERISTIC OF THE DECIMATION FILTER

Automatic Gain Control and Clamping

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

Sync Processing

The sync processor of TW2868 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the TW2868 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there are always two lines processing delay at the output except for the component input mode which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

The Figure 3 shows the frequency response of notch filter for each system NTSC and PAL. Figure 4 shows the frequency response of Chroma Band Pass Filter Curves.

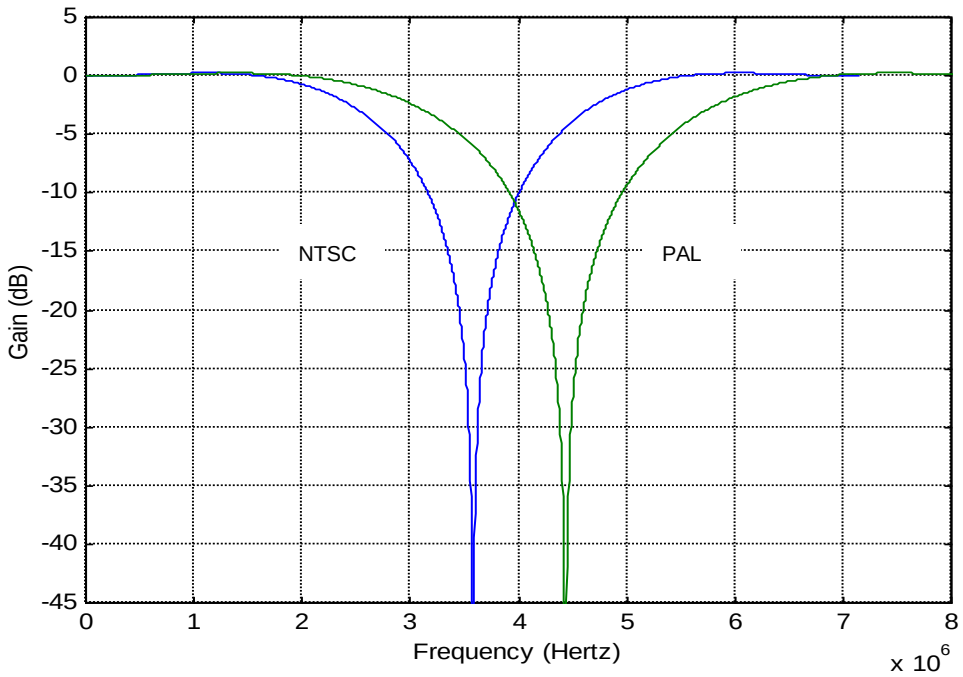


FIGURE 3. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR PAL

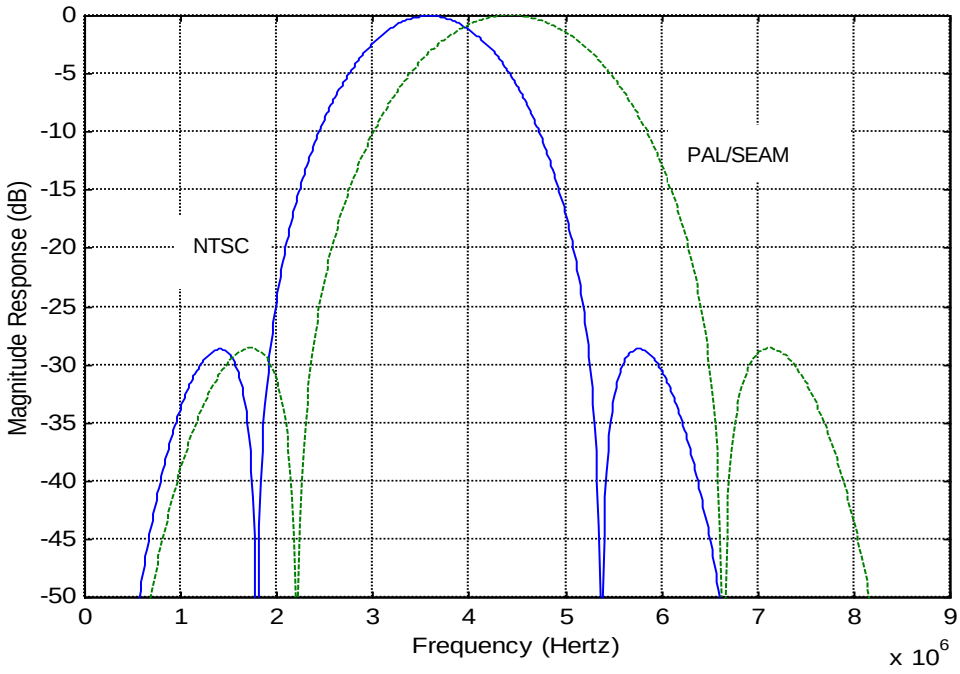


FIGURE 4. CHROMA BAND PASS FILTER CURVES

Color Decoding

CHROMINANCE DEMODULATION

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

The Figure 5 shows the frequency response of Chrominance Low-Pass Filter Curves.

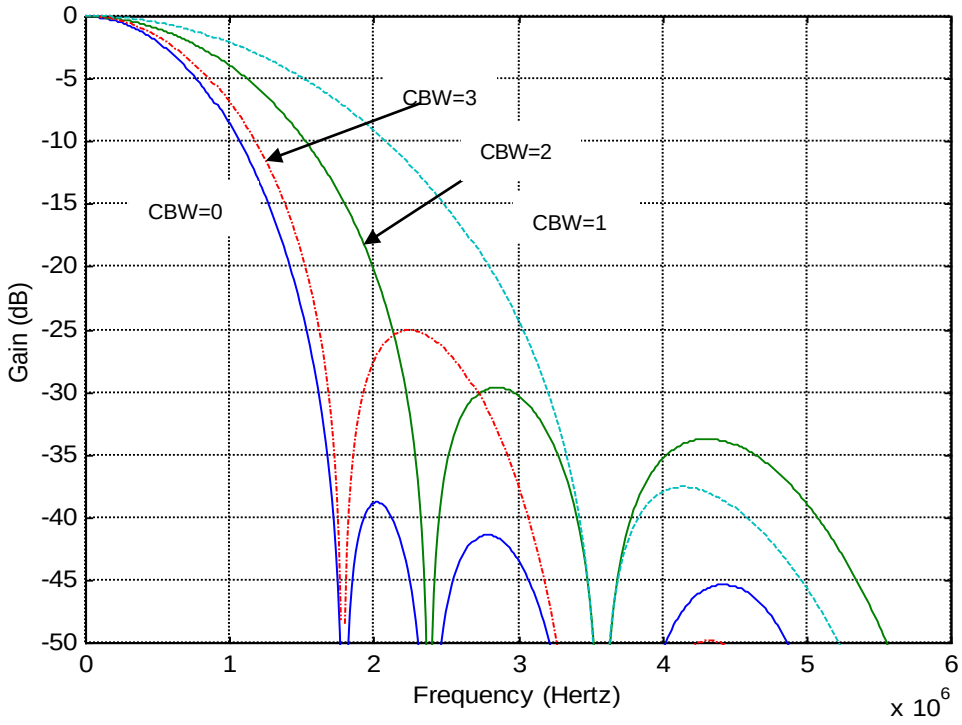


FIGURE 5. CHROMINANCE LOW-PASS FILTER CURVES

ACC (AUTOMATIC COLOR GAIN CONTROL)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The range of ACC control is –6db to +24db.

Chrominance Processing

CHROMINANCE GAIN, OFFSET AND HUE ADJUSTMENT

When decoding NTSC signals, TW2868 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (COLOR TRANSIENT IMPROVEMENT)

The TW2868 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

Luminance Processing

The TW2868 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW2868 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

The Figure 6 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

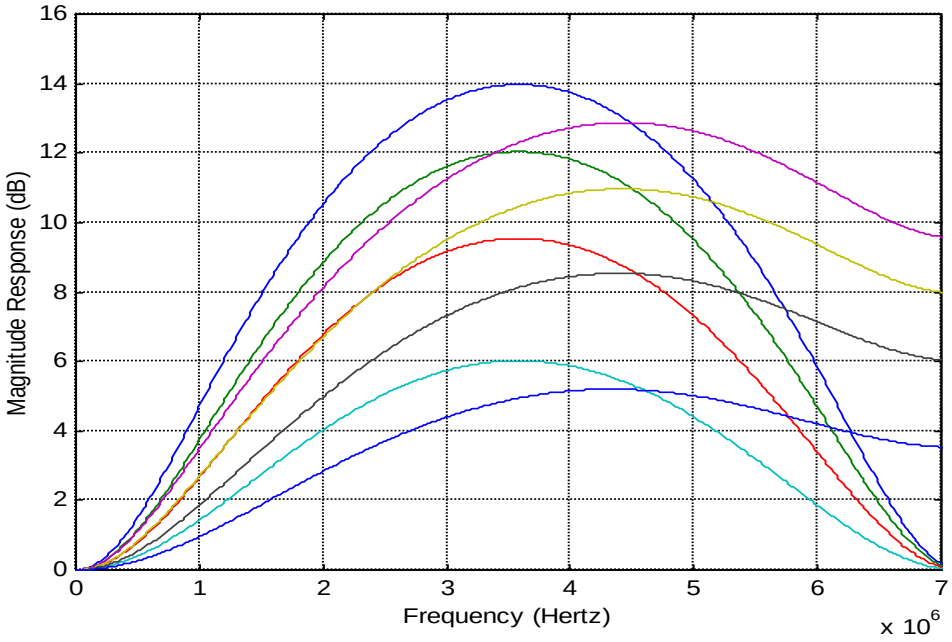


FIGURE 6. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

Video Cropping

Cropping allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig7.The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the un-scaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the un-scaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858.For PAL output at 13.5 MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

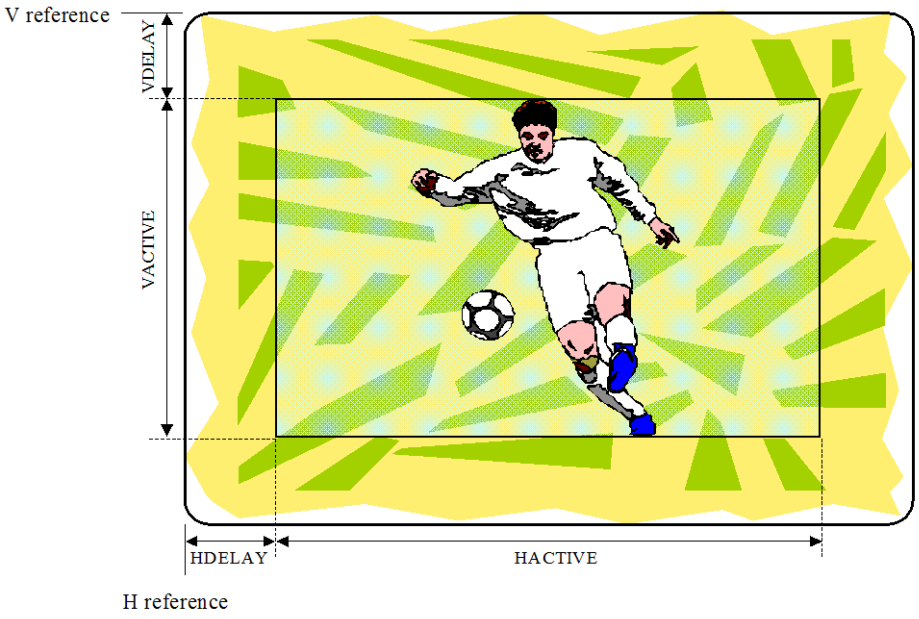


FIGURE 7. THE EFFECT OF CROPPING REGISTERS

Video Scaler

The TW2868 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses simple line dropping algorithm. Therefore, the use of non-integer vertical scaling ratio is not recommended.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW2868 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register, the 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{pixel\_desired}] * 256$

PAL: $HSCALE = [(720/N_{pixel\_desired})] * 256$

Where: $N_{pixel\_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at 320pixel resolution, the HSCALE value can be found as:

HSCALE = [(720/320)] * 256 = 576 = 0x0240

However, to output a SQ compatible NTSC stream at 320pixel resolution, the HSCALE value should be found as:

HSCALE = [(640/320)] * 256 = 512 = 0x200

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW2868. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: $VSCALE = [240/ N_{line\_desired}] * 256$

50Hz system: $VSCALE = [288/ N_{line\_desired}] * 256$

Where: $N_{line\_desired}$ is the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 2. Figure 8 shows Horizontal Scaler Pre-Filter Curves.

TABLE 2. HSCALE AND VSCALE VALUE FOR SOME POPULAR VIDEO FORMATS

SCALING RATIO	FORMAT	TOTAL RESOLUTION	OUTPUT RESOLUTION	HSCALE VALUES	VSCALE (FRAME)
1:1	NTSC SQ	780x525	640x480	0x0100	0x0100
	NTSC CCIR601	858x525	720x480	0x0100	0x0100
	PAL SQ	944x625	768x576	0x0100	0x0100
	PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)	NTSC SQ	390x262	320x240	0x0200	0x0200
	NTSC CCIR601	429x262	360x240	0x0200	0x0200
	PAL SQ	472x312	384x288	0x0200	0x0200
	PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400
	NTSC CCIR601	214x131	180x120	0x0400	0x0400
	PAL SQ	236x156	192x144	0x0400	0x0400
	PAL CCIR601	216x156	180x144	0x0400	0x0400

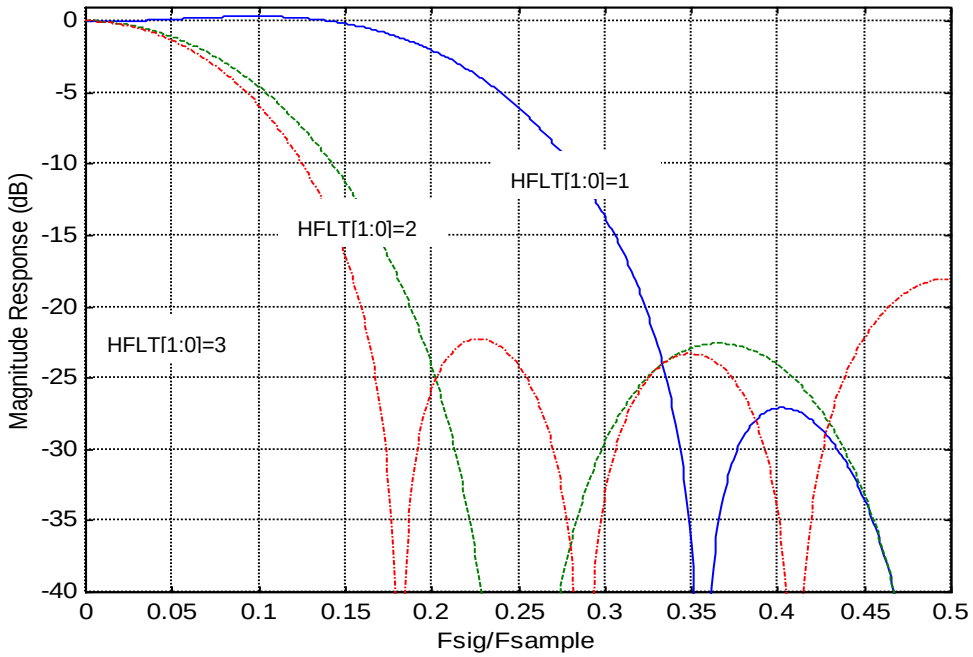


FIGURE 8. HORIZONTAL SCALER PRE-FILTER CURVES

Output Format

The TW2868 output time-multiplexed format. Each video data stream in time-multiplexed format is ITU-R BT.656 compatible data format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data. The phase of CLKPO or CLKNO can be controlled by delay unit via the CLKPO_DEL or CLKNO_DEL registers and polarity inverse cell via the CLKPO_POL or CLKNO_POL registers independently.

CHANNEL ID

The channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Each 656 data stream in 4xD1 output data, 4xCIF output data and 2xD1 output data can have this Sync Code and Blanking Code. Table 3 shows this Channel ID format. Nibble data value m shows Video Decoder number to be output in this video stream.

TABLE 3. THE CHANNEL ID FORMAT FOR 4CH CIF/4 TIME-MULTIPLEXED FORMAT WITH 54MHZ

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
Field	Vtime	Htime	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xFm
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEm
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDm
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xCm
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xBm
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAm
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9m
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x8m

(a) ITU-R BT.656 Sync Code with Channel ID

VIDEO	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
VINn	8'h1m	8'h8m	8'h8m

(b) Horizontal Blanking Code with Channel ID

m =0 Video1 656 data. m=1 Video2 656 data. m=2 Video3 656 data. m=3 Video4 656 data.
m=4 Video5 656 data. m=5 Video6 655.data. m=6 Video7 656 data. m=7 Video8 656 data.
n=m+1.

VIDEO LOSS OUTPUT

When NOVID_656 register is set to 1, bit7 of Fourth byte of SAV/EAV code will be 0 when video signal is lost. This can be an optional set of 656 SAV/EAV code for no-video (video lost) specific application.

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 54MHZ

The TW2868 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz that is useful to security application requiring two channel outputs through one channel video port. When VDnMD register is set to 1, the dual ITU-R BT.656 time-multiplexed format is enable on VDn[7:0] output pins.VDnO1SEL/VDnO2SEL register select CH1/CH2 data to be output on VDn pin from 8 Video Decoder BT.656 data. Figure 9 and Figure 10 illustrate VDn[7:0]/CLKPO/CLKNO pin timing with 54MHz/27MHz clock output mode.

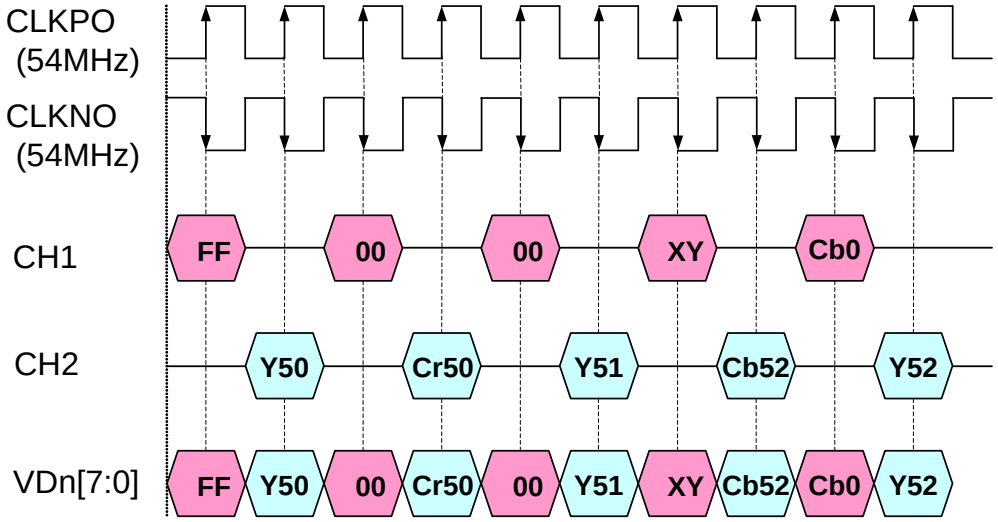


FIGURE 9. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 54MHZ CLOCK.

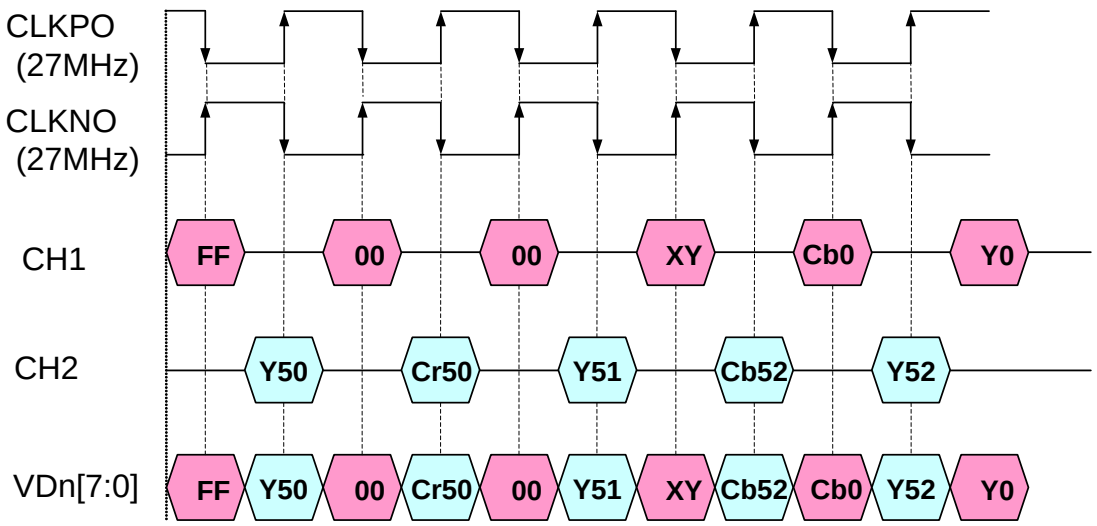


FIGURE 10. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 27MHZ CLOCK

FOUR CHANNEL CIF TIME-MULTIPLEXED FORMAT WITH 54MHZ

Four channel CIF (360x480) time-multiplexed format is also provided for specific security application when VDnMD register is set to 3. For this format, each channel ITU-R BT.656 data stream is down-sampled into 13.5MHz ITU-R BT.656 data stream except the sync code. Optionally, the vertical scaling can also be enabled to support Quad (360x240) format using the VSCL_ENA register. Then, these four 13.5MHz ITU-R BT.656 data stream are time-multiplexed into 54MHz data stream. This format requires only one channel video port to transfer four channel CIF data independently. When VDnMD register is set to 3, TW2868 can support one channel video port to transfer four channels CIF data independently and the other video port to transfer two channel Full D1 ITU-R BT.656 time-multiplexed format or four channel Full D1 ITU-R.656 time-multiplexed format simultaneously. Optionally, when the vertical scaling is enabled, the ITU-R BT.656 sync code will be skipped in the invalid line through the VSCL_SYNC register. Figure 11 illustrates the timing diagram for four channel CIF time-multiplexed format with 54MHz.

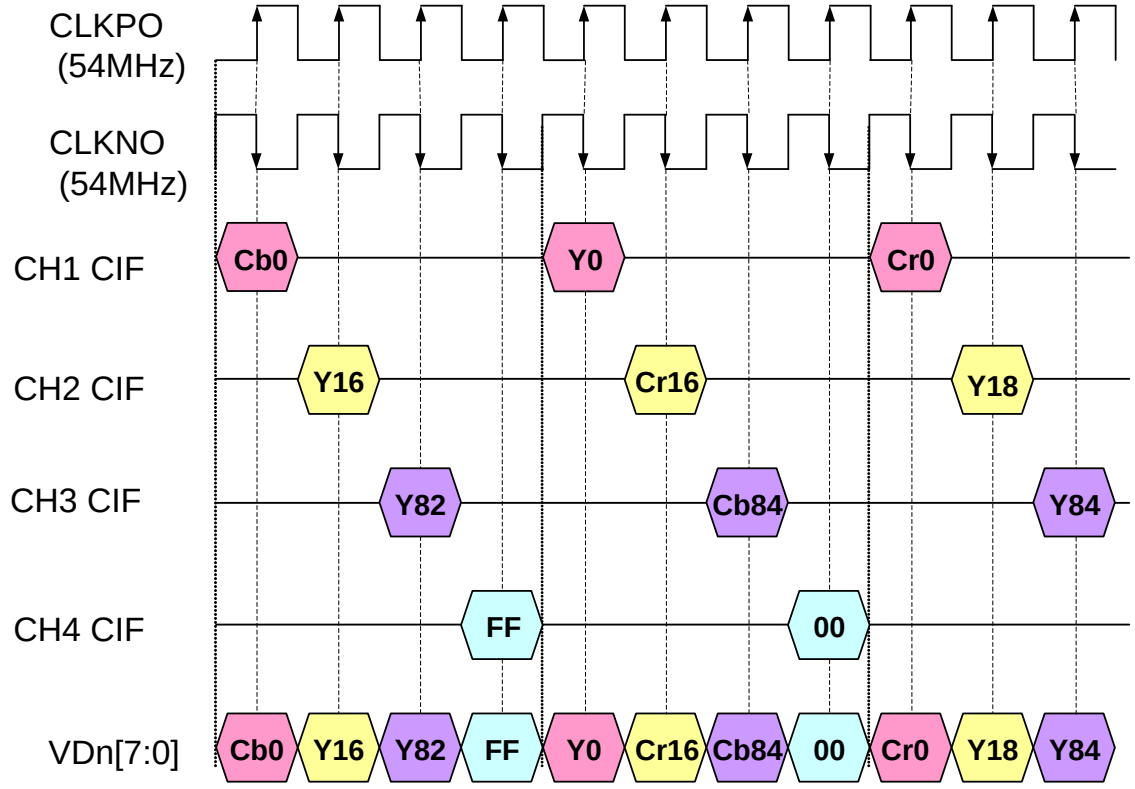


FIGURE 11. PIN OUTPUT TIMING OF 4 CH CIF TIME-MULTIPLEXED FORMAT WITH 54MHZ CLOCK

FOUR CHANNEL D1 TIME-DIVISION-MULTIPLEXED FORMAT WITH 108MHZ

Four channel of D1 (720x480) at 27MHz video stream that are time-division-multiplexed at 108MHz data rate format is implemented in TW2868 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2868 implements single 8 bit bus at 4 times the base band pixel clock rate of 27MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data. When VDnMD register is set to 2,VDn[7:0] pin Is enabling to output this 4xFull D1 data.VDn01SEL/VDn02SEL/VDn03SEL/VDn04SEL register select CH1/CH2/CH3/CH4 output data in Figure 12 from 8 Video Decoder 656 data.

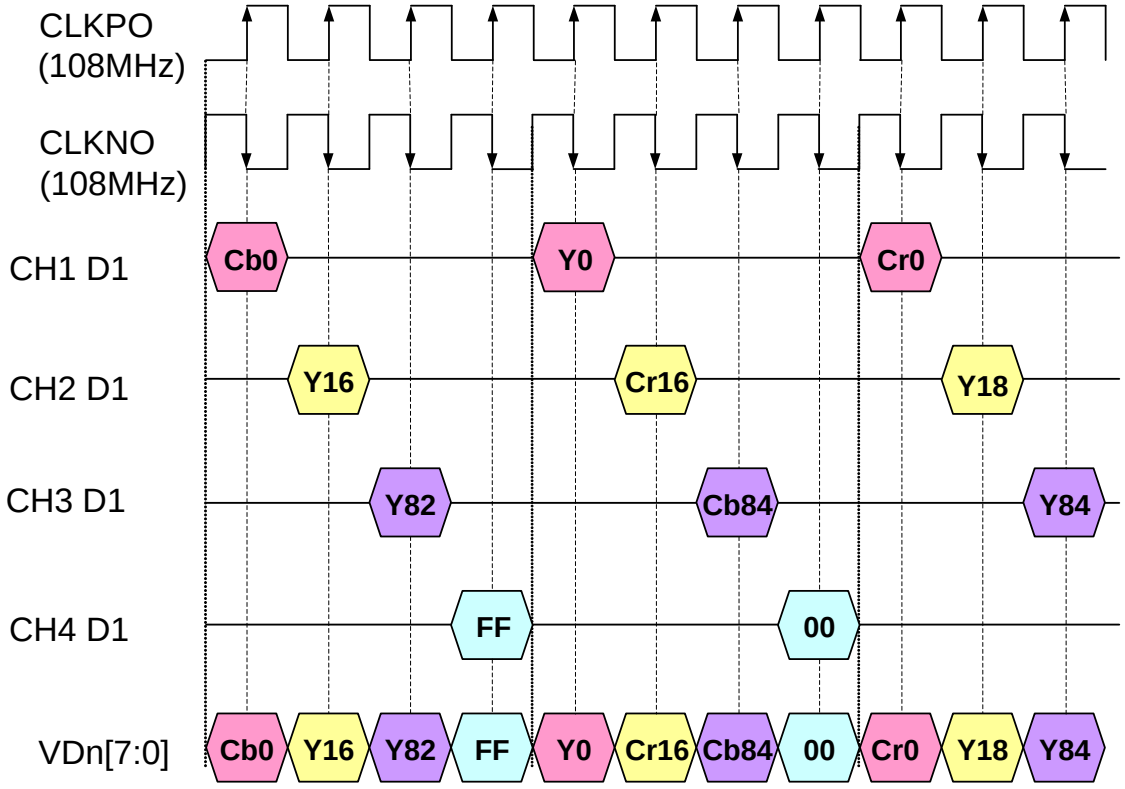


FIGURE 12. PIN OUTPUT TIMING OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 108MHZ CLOCK

OUTPUT ENABLING ACT

After power-up, the TW2868 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, the TW2868 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

MPPN OUTPUT

MPPn pin can be used for GPO output pin or VDLOSS (video lost) signal output. Optionally, additional timing information such as syncs and field flag are also supported through the MPPn pins. The video output timing is illustrated in Figure 13 and Figure 14 TW2868 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VSYNC/FIELD output function. Start of VS timing is controlled by VSHT register(V timing) and OVSDLY register(H timing).End of VS timing is controlled by OVSEND register(V Timing).Start of FLD timing is controlled by OFDLY register(V timing).Start of HS timing is controlled by HSBEGIN register and End of HS timing is controlled by HSEND register.

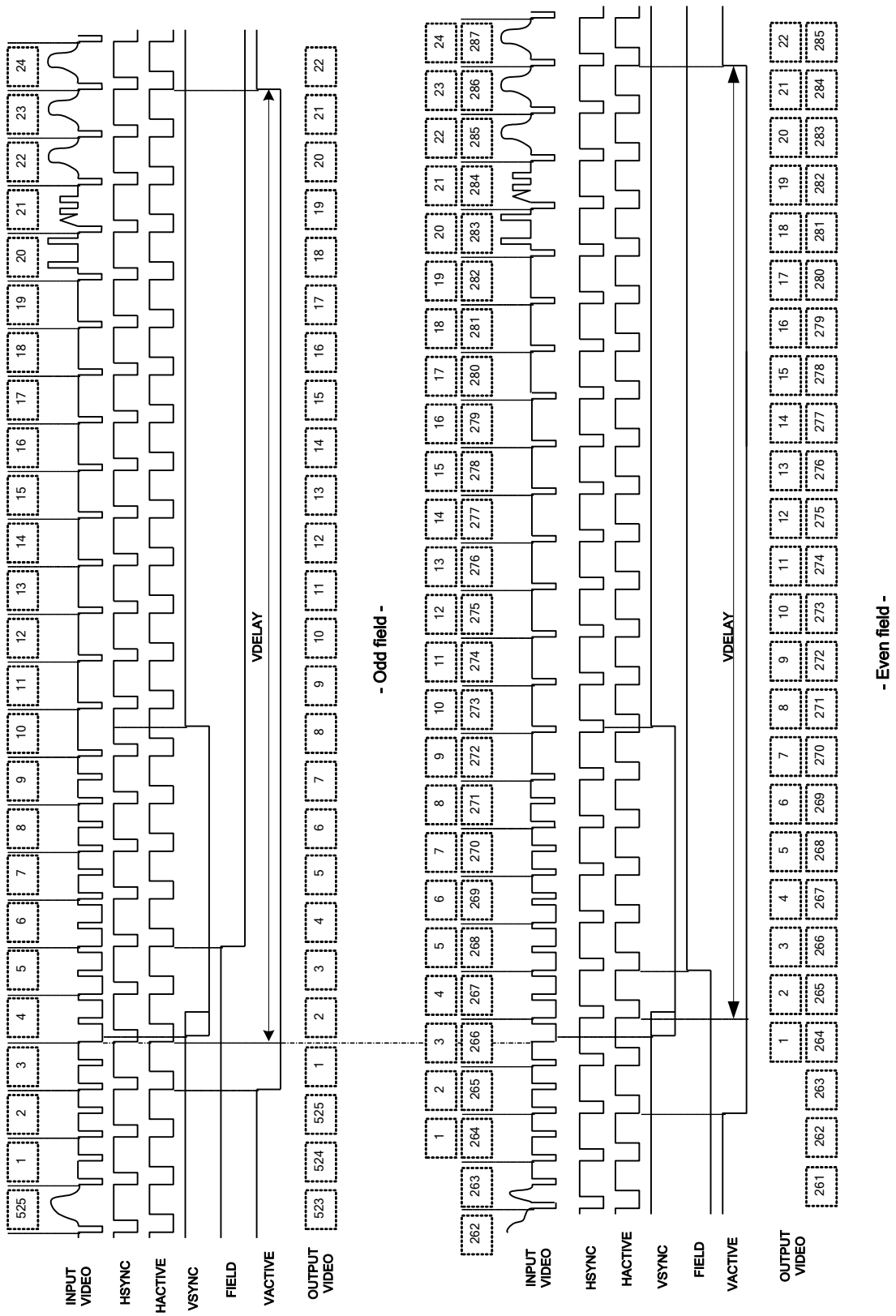


FIGURE 13. VERTICAL TIMING DIAGRAM FOR 60HZ/525 LINE SYSTEM

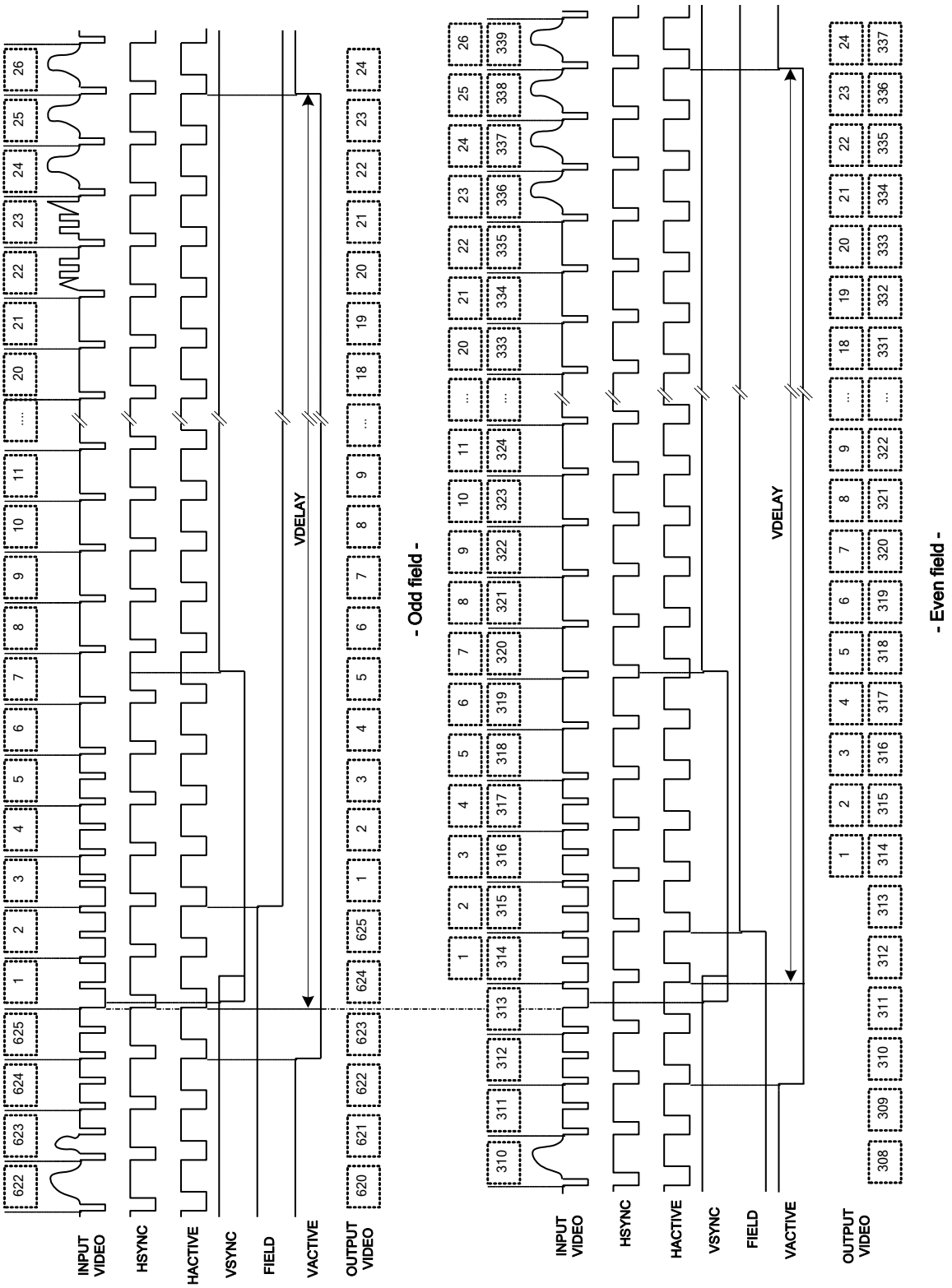


FIGURE 14. VERTICAL TIMING DIAGRAM FOR 50HZ/625 LINE SYSTEM

VIDEO OUTPUT FORMAT/CHANNEL SELECTION

VDnMD register select output format on VDn[7:0] pins.

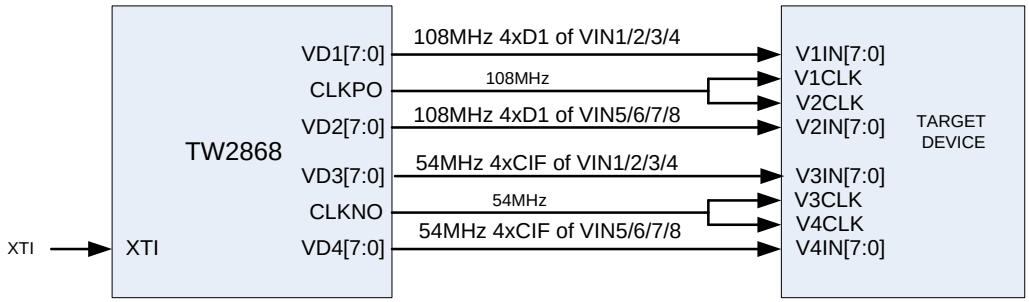
VDnO1SEL/VDnO2SEL/VDnO3SEL/VDnO4SEL registers select CH data in mux video data on VDn[7:0] pin .

TABLE 4. OUTPUT FORMAT AND CH DATA SELECTION

FORMAT	VDNMD	OUTPUT CH DATA SELECTION REGISTER
2xD1 output	1	CH1:VDnO1SEL CH2:VDnO2SEL
4xD1 output	2	CH1:VDnO1SEL CH2:VDnO2SEL CH3:VDnO3SEL CH4:VDnO4SEL
4xCIF output	3	CH1:VDnO1SEL CH2:VDnO2SEL CH3:VDnO3SEL CH4:VDnO4SEL

VIDEO OUTPUT INTERFACE

The followings figures show typical Video Output interface examples. Another interface are also available by more register settings.



XTI (MHz)	SEL _X24	VD1MD	VD2MD	VD3MD	VD4MD	PLL_PD	DECOSC	XTIMD	CLKPO _MD	CLKNO _MD	CLKPO _POL	CLKNO _POL	CLKPO _DS	CLKNO _DS
27	1	2	2	3	3	0	1	3	2	1	0	0	0or1	0or1
54	0	2	2	3	3	0	1	3	2	1	0	0	0or1	0or1
108	X	2	2	3	3	1	0	2	2	1	0	0	0or1	0or1

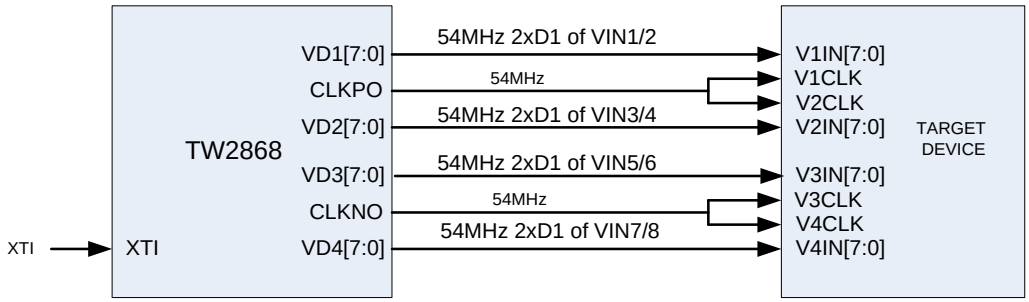
VD1O1SEL	VD1O2SEL	VD1O3SEL	VD1O4SEL
0	1	2	3

VD2O1SEL	VD2O2SEL	VD2O3SEL	VD2O4SEL
4	5	6	7

VD3O1SEL	VD3O2SEL	VD3O3SEL	VD3O4SEL
0	1	2	3

VD4O1SEL	VD4O2SEL	VD4O3SEL	VD4O4SEL
4	5	6	7

FIGURE 15. 2X4D1+2X4CIF VIDEO OUTPUT INTERFACE WHEN TARGET HAS MULTI CLOCK INPUTS



XTI (MHz)	SEL _X24	VD1MD	VD2MD	VD3MD	VD4MD	PLL_PD	DECOSC	XTIMD	CLKPO _MD	CLKNO _MD	CLKPO _POL	CLKNO _POL	CLKPO _DS	CLKNO _DS
27	1	1	1	1	1	0	1	3	1	1	0	1	0or1	0or1
54	X	1	1	1	1	1	0	1	1	1	0	1	0or1	0or1

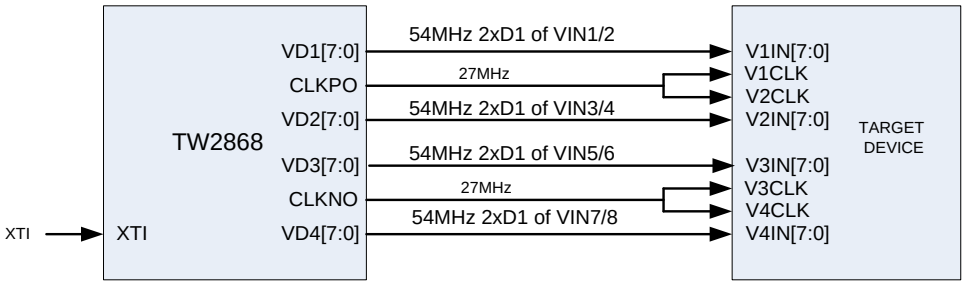
VD1O1SEL	VD1O2SEL	VD1O3SEL	VD1O4SEL
0	1	X	X

VD2O1SEL	VD2O2SEL	VD2O3SEL	VD2O4SEL
2	3	X	X

VD3O1SEL	VD3O2SEL	VD3O3SEL	VD3O4SEL
4	5	X	X

VD4O1SEL	VD4O2SEL	VD4O3SEL	VD4O4SEL
6	7	X	X

FIGURE 16. 4X2D1 WITH 54MHZ CLOCK VIDEO OUTPUT INTERFACE WHEN TARGET HAS MULTI CLOCK INPUTS



XTI (MHz)	SEL _X24	VD1MD	VD2MD	VD3MD	VD4MD	PLL_PD	DECOSC	XTIMD	CLKPO _MD	CLKNO _MD	CLKPO _POL	CLKNO _POL	CLKPO _DS	CLKNO _DS	CKIPOL
27	1	1	1	1	1	0	1	3	0	0	0	1	0or1	0or1	1
54	X	1	1	1	1	1	0	1	0	0	0	1	0or1	0or1	0

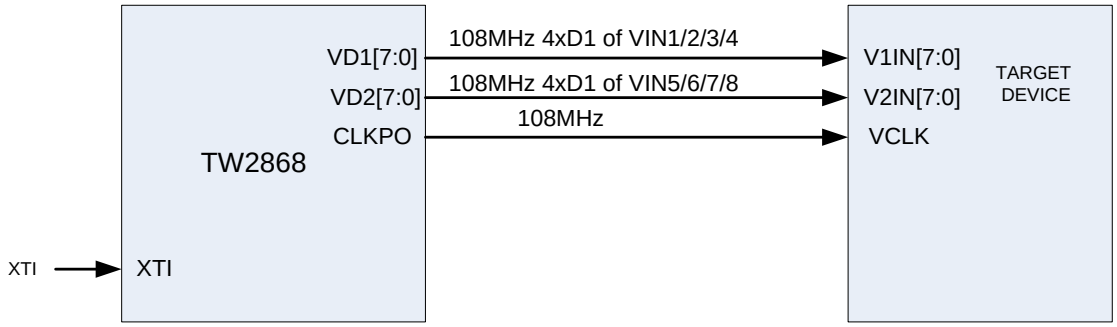
VD1O1SEL	VD1O2SEL	VD1O3SEL	VD1O4SEL
0	1	X	X

VD2O1SEL	VD2O2SEL	VD2O3SEL	VD2O4SEL
2	3	X	X

VD3O1SEL	VD3O2SEL	VD3O3SEL	VD3O4SEL
4	5	X	X

VD4O1SEL	VD4O2SEL	VD4O3SEL	VD4O4SEL
6	7	X	X

FIGURE 17. 4X2D1 WITH 27MHZ CLOCK VIDEO OUTPUT INTERFACE WHEN TARGET HAS MULTI CLOCK INPUTS

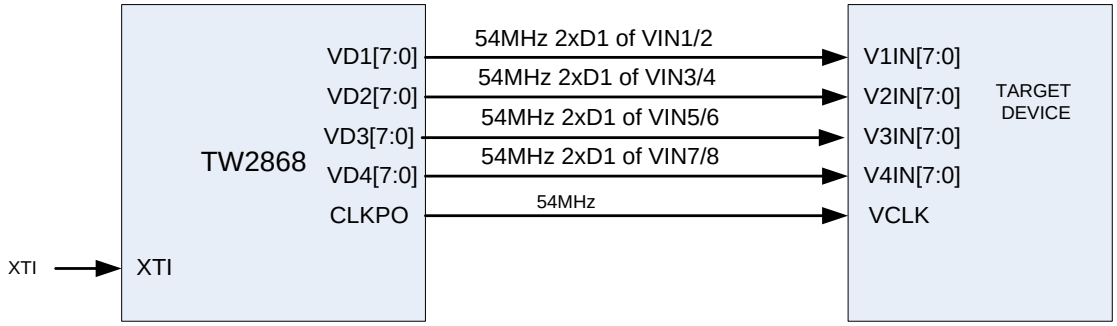


XTI (MHz)	SEL _X24	VD1MD	VD2MD	PLL_PD	DECOSC	XTIMD	CLKPO _MD	CLKPO _POL
27	1	2	2	0	1	3	2	0
54	0	2	2	0	1	3	2	0
108	X	2	2	1	0	2	2	0

VD1O1SEL	VD1O2SEL	VD1O3SEL	VD1O4SEL
0	1	2	3

VD2O1SEL	VD2O2SEL	VD2O3SEL	VD2O4SEL
4	5	6	7

FIGURE 18. 2X4D1 WITH 108MHZ CLOCK VIDEO OUTPUT INTERFACE WHEN TARGET HAS ONLY ONE CLOCK INPUT



XTI (MHz)	SEL _X24	VD1MD	VD2MD	VD3MD	VD4MD	PLL_PD	DECOSC	XTIMD	CLKPO _MD	CLKPO _POL	CLKPO _DS
27	1	1	1	1	1	0	1	3	1	0	0
54	X	1	1	1	1	1	0	1	1	0	0

VD1O1SEL	VD1O2SEL	VD1O3SEL	VD1O4SEL
0	1	X	X

VD2O1SEL	VD2O2SEL	VD2O3SEL	VD2O4SEL
2	3	X	X

VD3O1SEL	VD3O2SEL	VD3O3SEL	VD3O4SEL
4	5	X	X

VD4O1SEL	VD4O2SEL	VD4O3SEL	VD4O4SEL
6	7	X	X

FIGURE 19. 4X2D1 WITH 54MHZ CLOCK VIDEO OUTPUT INTERFACE WHEN TARGET HAS ONLY ONE CLOCK INPUT

Video Encoder

The TW2868 has built-in NTSC/PAL video encoder to support the analog video output. It converts the standard digital ITU-R BT.656 data stream into analog composite or Y/C video output through two 10 bit video DACs. The digital video data is first gain adjusted according the format selected. The luminance signal is band-limited to 6MHz before interpolated to 27MHz sampling rate. The chrominance is also band-limited to selected bandwidth before modulated with the internal generated sub-carrier and interpolated to 27MHz sampling rate. These signals are finally combined with sync information before sending out to DAC. The encoder can operate in either master or slave clock mode. In the master mode, the clock comes from the internal generated 27MHz clock. The NTSC output can be selected to include a 7.5 IRE pedestal. The luminance, chrominance, sync and burst amplitude can be adjusted independently. It also has built-in color bar pattern generator for video adjustment. The block diagram is shown in the following figure.

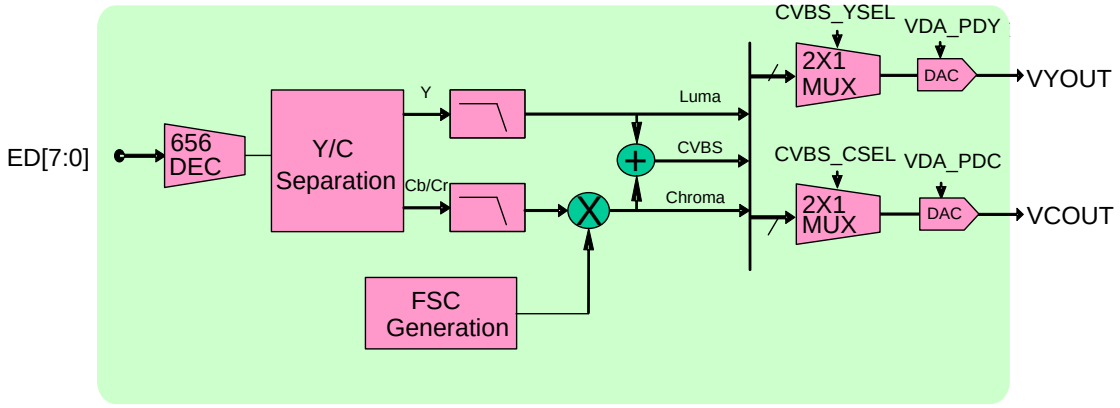


FIGURE 20. ENCODER BLOCK DIAGRAM

Output Standard Selection

The TW2868 supports various video standard outputs via the HZ50 and FSCSEL, PHALT, PED registers as described in Table 5.

TABLE 5. ANALOG OUTPUT VIDEO STANDARDS

FORMAT	SPECIFICATION			REGISTER			
	LINE/FV (HZ)	FH (KHZ)	FSC (MHZ)	HZ50	FSCSEL	PHALT	PED
NTSC-M	525/59.94	15.734	3.579545	0	0	0	1
NTSC-J							0
NTSC-4.43	525/59.94	15.734	4.43361875	0	1	0	1
NTSC-N	625/50	15.625	3.579545	1	0	0	0
PAL-BDGHI	625/50	15.625	4.43361875	1	1	1	0
PAL-N							1
PAL-M	525/59.94	15.734	3.57561149	0	2	1	0
PAL-NC	625/50	15.625	3.58205625	1	3	1	0
PAL-60	525/59.94	15.734	4.43361875	0	1	1	0

If the PHALT register is set to “1”, phase alternation can be reset every 8 field so that phase alternation keeps same phase every 8 field.

Chrominance Filter

The bandwidth of chrominance signal can be selected via the CBW register as shown in Figure 21.

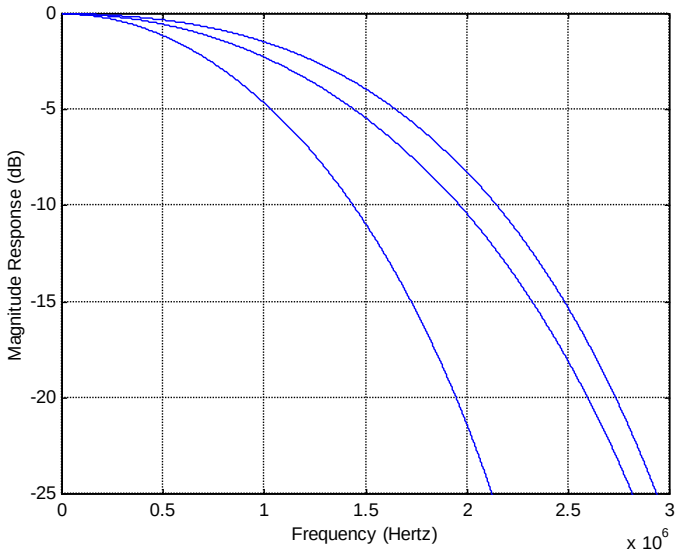


FIGURE 21. CHARACTERISTICS OF CHROMINANCE FILTER

Digital-to-Analog Converter

The digital video data from video encoder is converted to analog video signal by DAC (Digital to Analog Converter). The analog video signal format can be selected for each DAC independently via the CVBS_YSEL and CVBS_CSEL register. Each DAC can be disabled independently to save power by the VDA_PDY and VDA_PDC register. The full scale current can be controlled by the external RSET resistor.

A simple reconstruction filter is required externally to reject noise as shown in Figure 22.

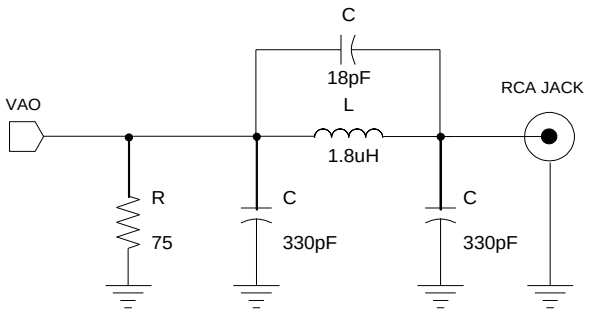


FIGURE 22. EXAMPLE OF RECONSTRUCTION FILTER

Audio Codec

The audio codec in the TW2868 is composed of ten audio Analog-to-Digital converter processes, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as the Fig23. The TW2868 can accept 10 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

The level of analog audio input signal AIN1/2/3/4/51/5/6/7/8/52 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1/2/3/4/51/5/6/7/8/52 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function. To record audio data, the TW2868 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pin.

The TW2868 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1/2/3/4/51/5/6/7/8/52/P registers. This mixing audio output can be provided through the analog and digital interfaces. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The embedded audio Digital-to-Analog converter supports the analog audio output.

The main purpose of AIN51/52 is to make the standard I2S/DSP digital audio output for AIN51/AIN52 data on ADATM pin for special application. Usually, 8 AIN1/AIN2/AIN3/AIN4/AIN5/AIN6/AIN7/AIN8 audio data are used on ADATR pin output.

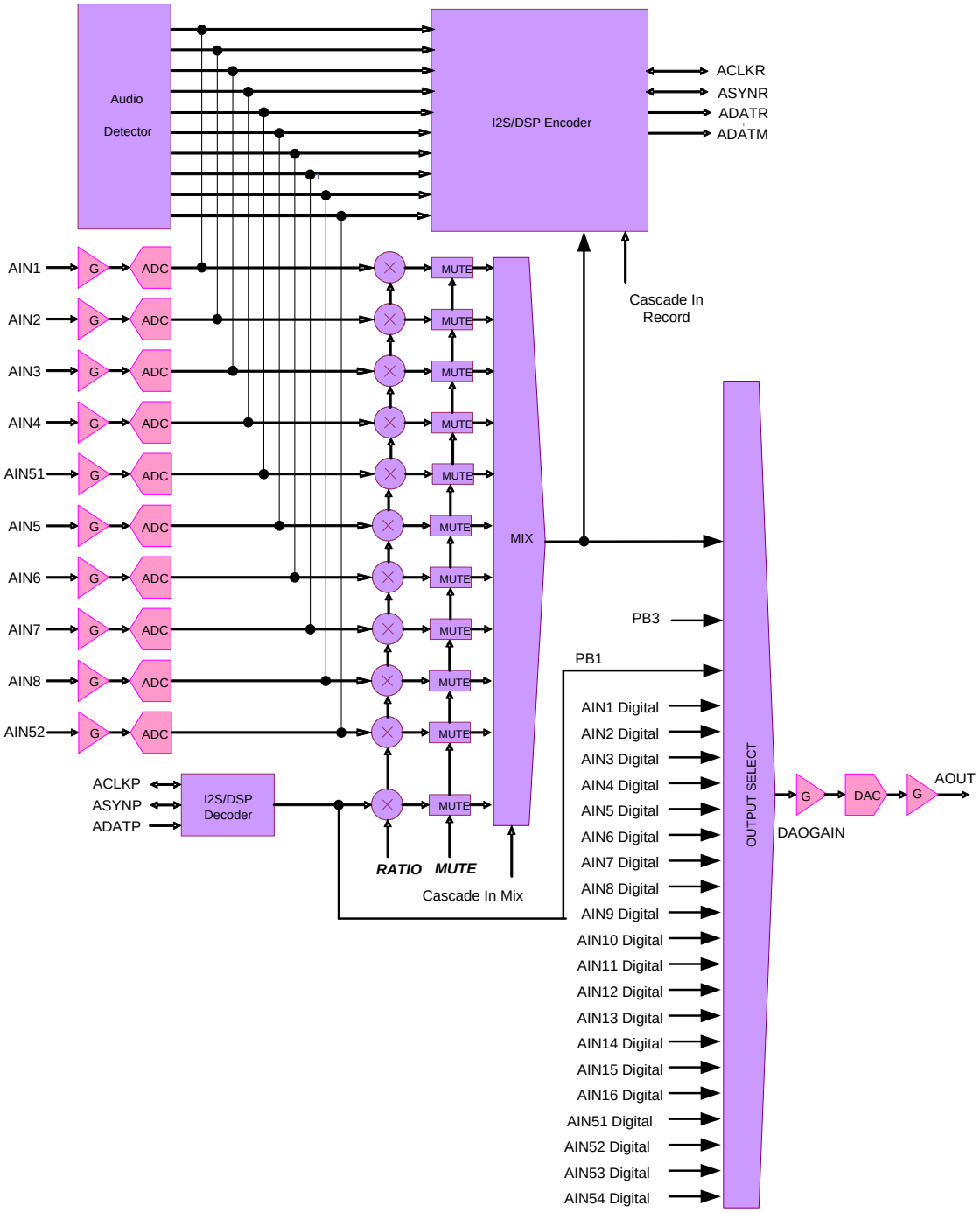


FIGURE 23. BLOCK DIAGRAM OF AUDIO CODEC

AUDIO CLOCK MASTER/SLAVE MODE

The TW2868 has two types of Audio Clock modes. If ACLKRMASTER register is set to 1, fs audio sample date is processed from audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0(output enable mode).If ACLKRMASTER register is set to 0, fs audio sample rate is processed from audio clock on ACLKR pin input.256xfs, 320xfs or 384xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode.AIN5MD and AFS384 register set up Audio fs mode by following Table 6. Audio Fs mode selection.

TABLE 6. AUDIO FS MODE SELECTION

REGISTER		FS MODE
AIN5MD	AFS384	
0	0	256xfs
1	0	320xfs
0	1	384xfs

AUDIO DETECTION

The TW2868 has an audio detector for individual 10 channels. Those are detection of differential amplitude from audio data. The accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1/2/3/4/51/5/6/7/8/52 registers. The status for audio detection are read by the AVDET1_STATE/AVDET2_STATE/A51DET_STATE/A52DET_STATE register and those also make the interrupt request through the IRQ pin with the combination of the status for video loss detection.

MULTI-CHIP OPERATION

TW2868 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 2 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode.

Each stage chip can accept 10 analog audio signals so that two cascaded chips will be 16-channel audio controller as default AIN5MD=0. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2868 can generate 16 channel data simultaneously using multi-channel method. The last stage chip can support 8 channel record outputs that are corresponding with analog audio inputs. The first stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog converter in the first stage chip. The first stage chip can output any audio channel data on AOUT pin. The first stage chip can also output 16 channel mixing audio data by the digital serial audio data for playback, analog audio signal on first stage chip and cascade input data.

Several Master/Slave mode configurations are available. Figure 24 is the most recommended and demanded system with Clock Master Mode (ACLKRMASTER=1). Figure 25 is the most recommended system with Clock Slave Sync Slave mode (ACLKRMASTER=0, ASYNROEN=1).

Another system combinations are also available if application needs different type specific system. Figure 24 and Figure 25 show the most typical system. In the following each figure, AIN1-16-51-54/Pb1-Pb3 means one selected Audio output in AIN1-16-51-54/Pb1-Pb3. If one TW2868 uses AIN5MD=1, all other cascaded TW2868 chips must set up AIN5MD=1 together.

In Multi-Chip Audio operation mode, one same Oscillator clock source (27MHz or 54MHz) need to be connected to all TW2868 XTI pin. If 108MHz clock needs to be connected to XTI pin, RSTB pin input control needs to be considered. Figure 26 shows RSTB timing on XTI 108MHz mode. Figure 27 shows one of RSTB control on XTI 108MHz mode.

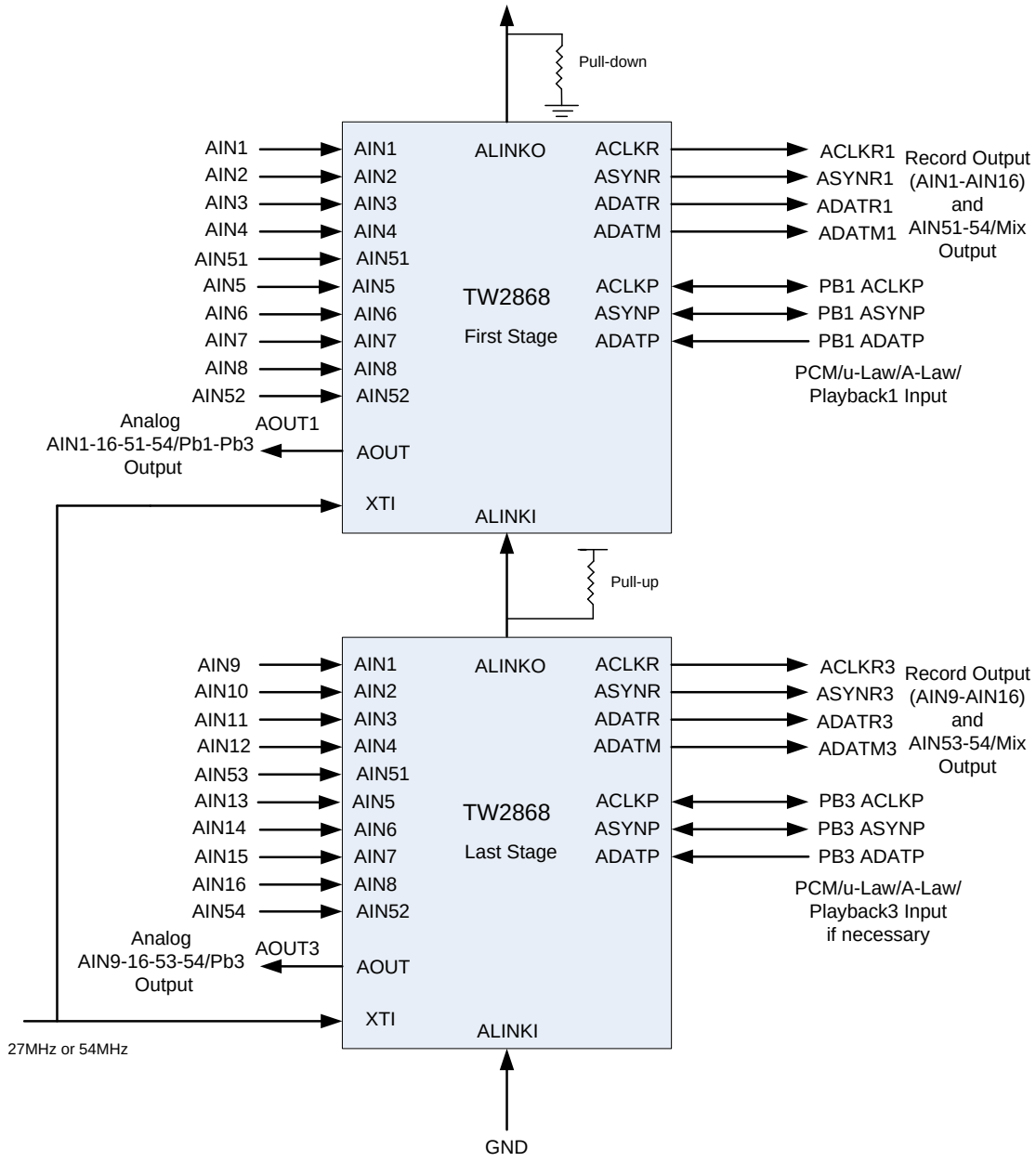


FIGURE 24. CLOCK MASTER CASCADE MODE SYSTEM

All chips have SMD=2; ACLKRMASTER=1; ASYNROEN=0

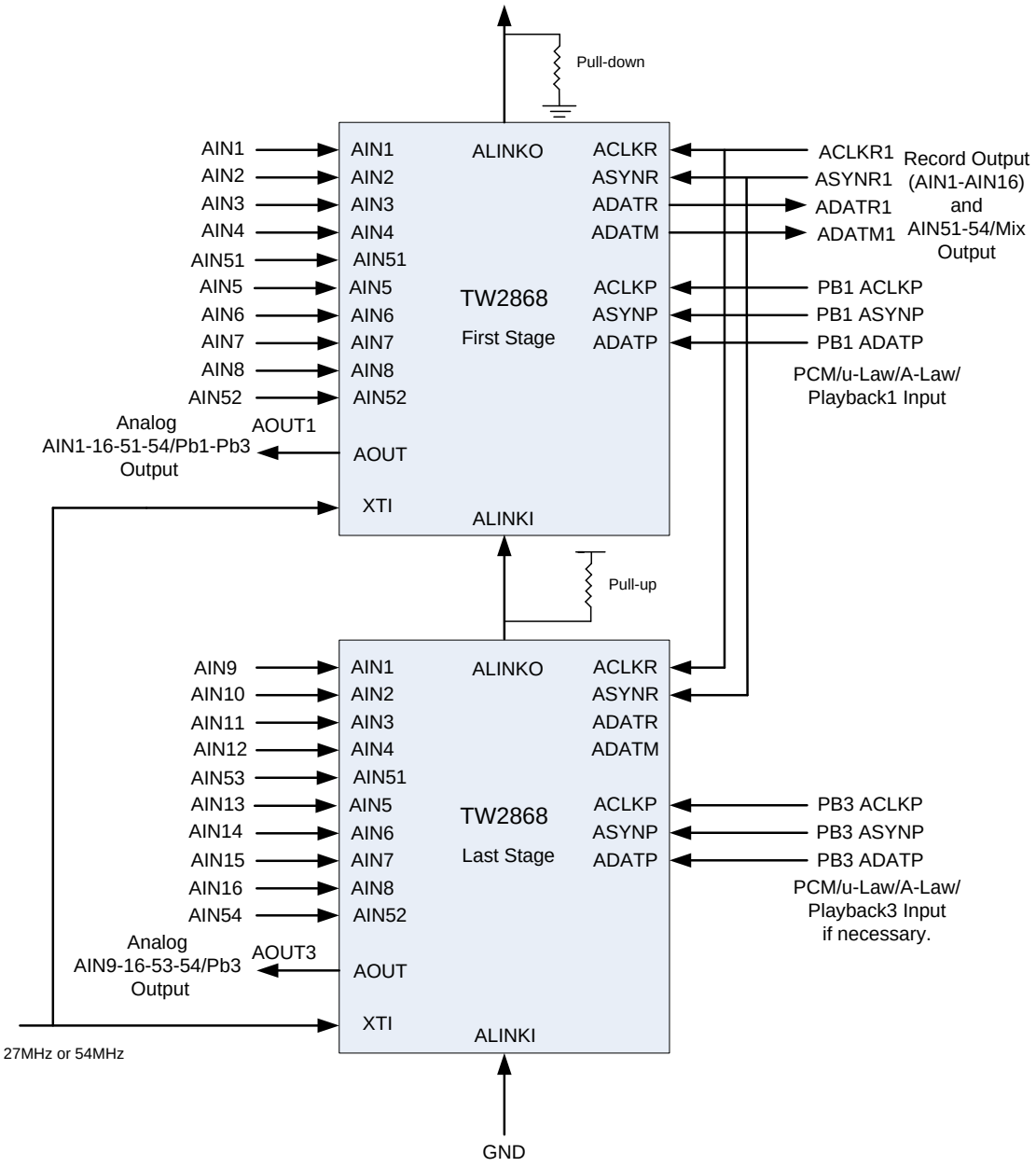


FIGURE 25. CLOCK SLAVE SYNC SLAVE CASCADE MODE SYSTEM

ALL CHIPS HAVE SMD=2; ACLKRMASTER=0; ASYNROEN=1; PB_MASTER=0

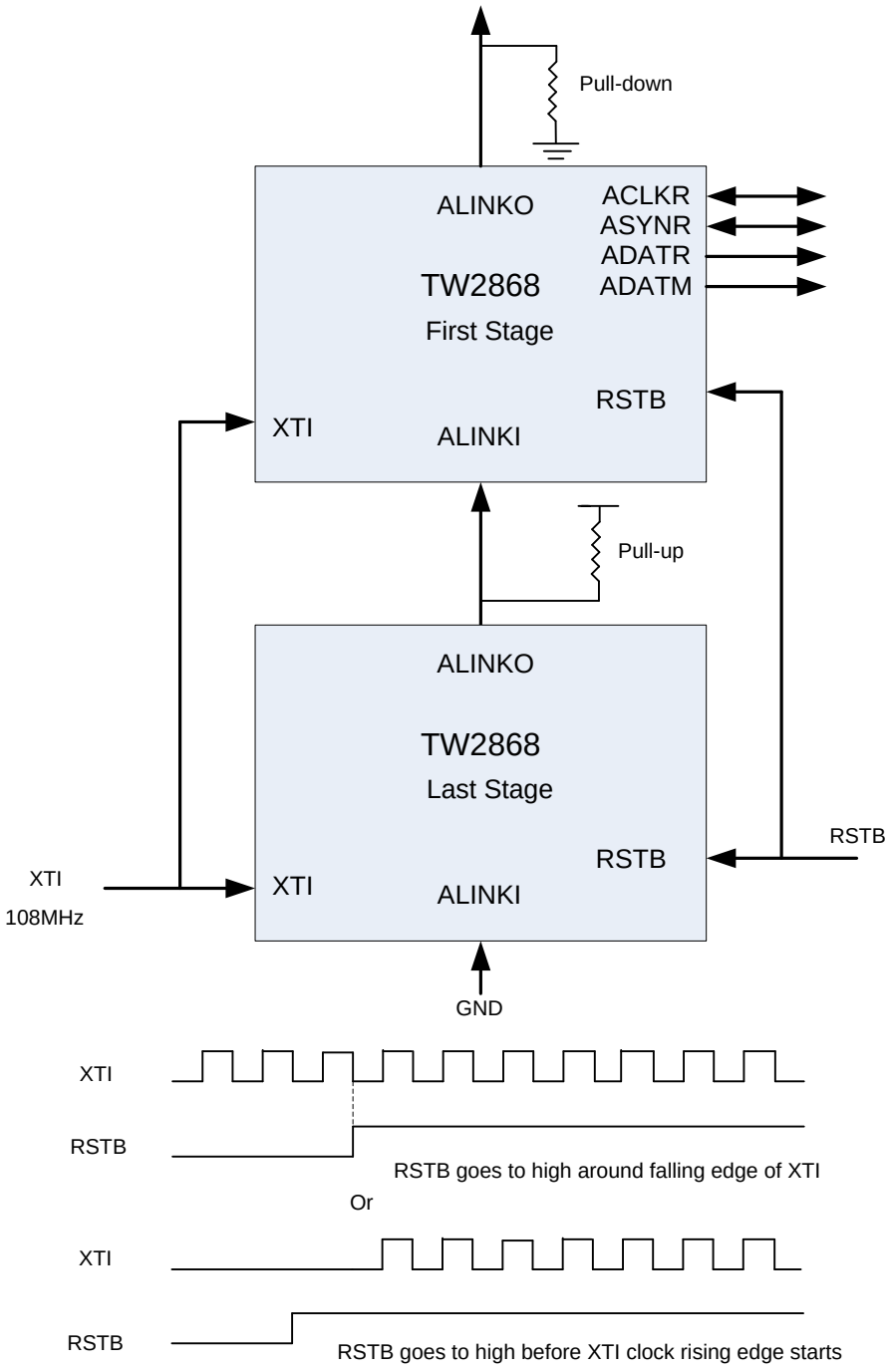
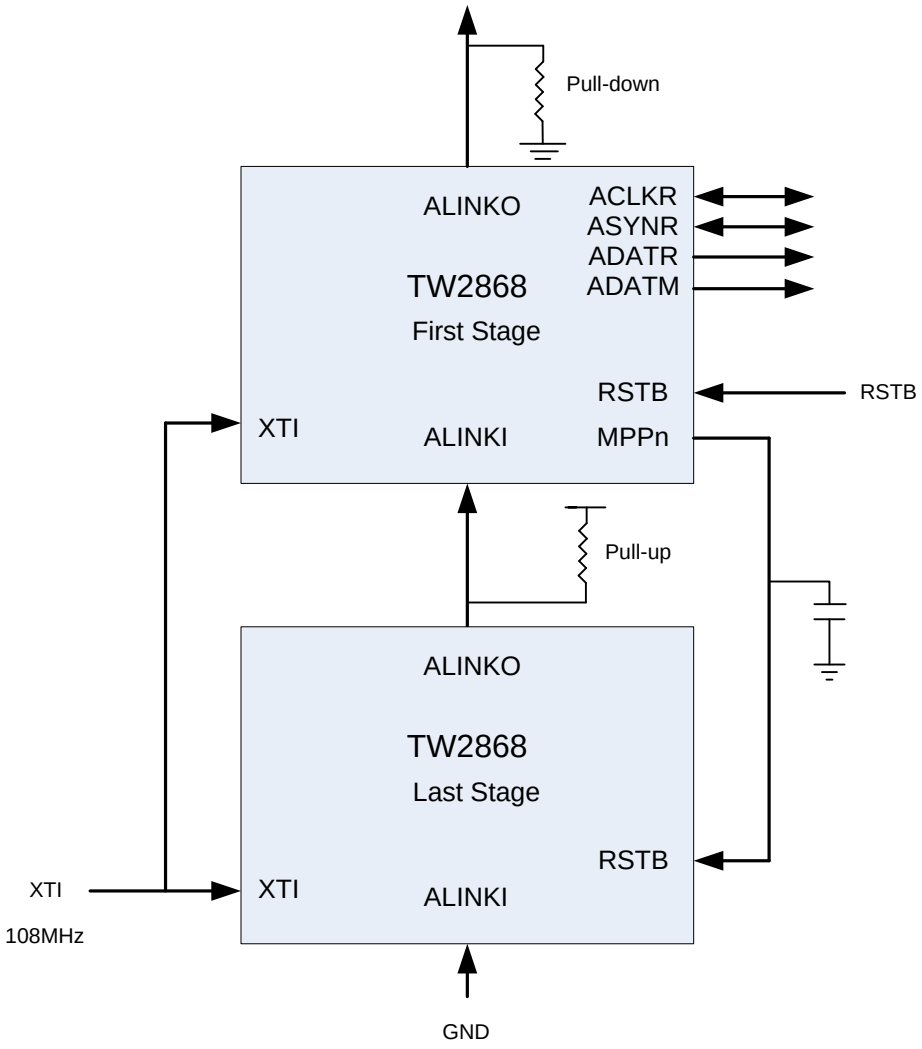


FIGURE 26. RSTB TIMING ON XTI 108MHZ MODE

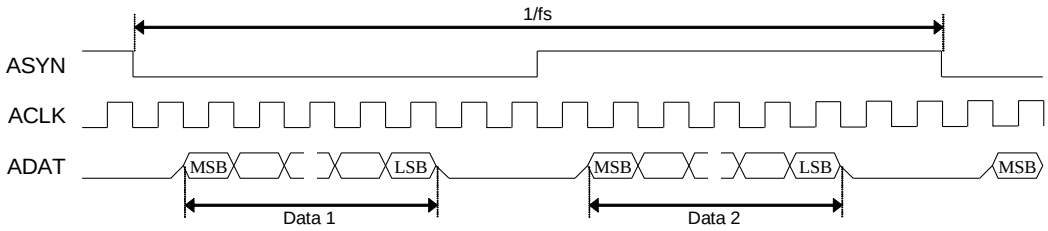


One of MPPn(n=1,2,3,,,8) controls previous chip's RSTB timing
by GPO output mode

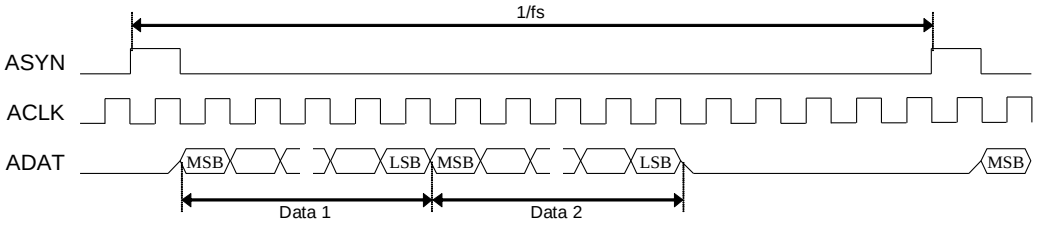
FIGURE 27. RSTB CONTROL BY MPPN GPO OUTPUT ON XTI 108MHZ MODE

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW2868, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in Figure 28.



(a) I2S Format



(b) DSP Format

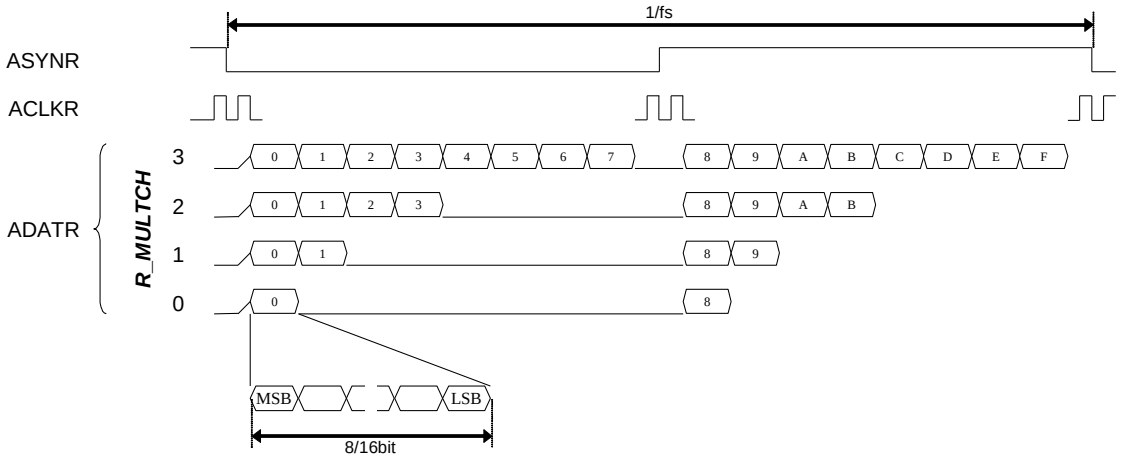
FIGURE 28. TIMING CHART OF SERIAL AUDIO INTERFACE

Playback Input

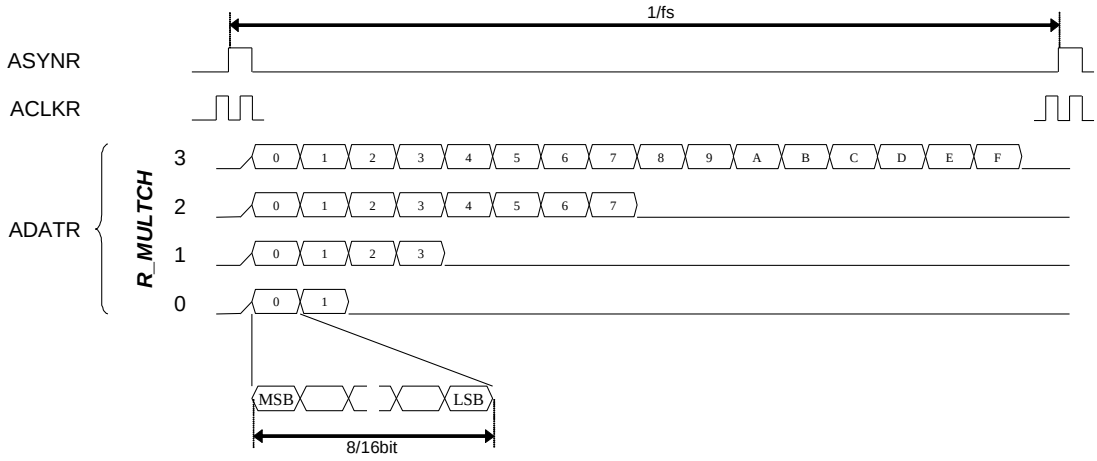
The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW2868 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs, 320xfs or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2868 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. The Fig29 shows the digital serial audio data organization for multi-channel audio.



(a) I2S Format



(b) DSP Format

FIGURE 29. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

Error! Reference source not found. 7 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F

register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is showed also in Table 7.

TABLE 7. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD

(a) I2S Format

R_MULTCH	Pin	Left Channel								Right Channel							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	Pin	Left/Right Channel															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data which are mixing audio and playback audio in this Mix output mode. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width per one digital audio data for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO CLOCK SLAVE MODE DATA OUTPUT TIMING

TW2868 always output ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing.

ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM outputs are always fixed to one ACLKR falling edge timing. But if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, TW2868 output ADATR/ADATM by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during ACLKR = 0.TW2868 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

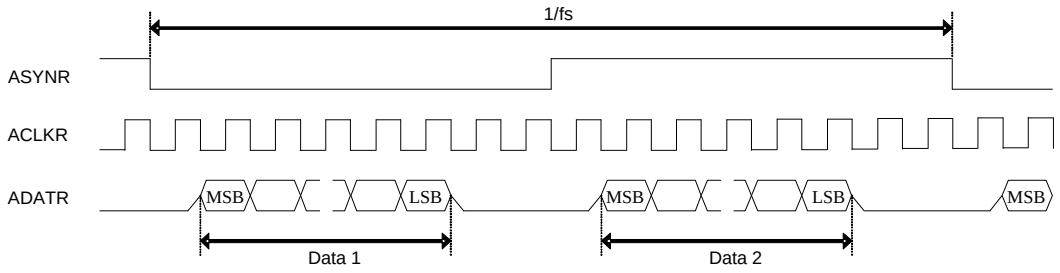


FIGURE 30. ACLKMASTER=0, RM_SYNC=0

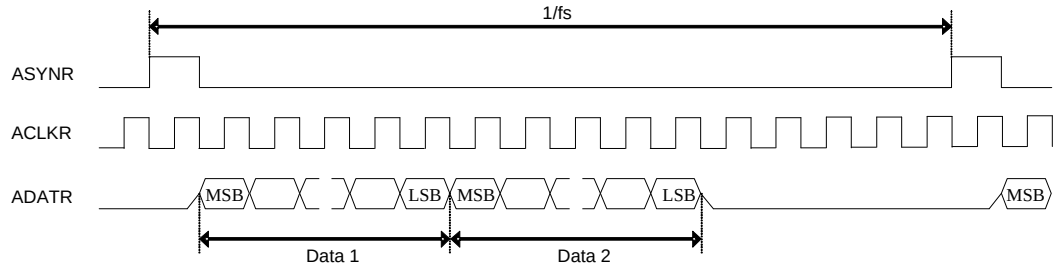


FIGURE 31. ACLKMASTER=0, RM_SYNC=1

ASYNR IS ACLKR RISING EDGE TRIGGERED INPUT

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2868 output ADATR/ADATM by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during ACLKR = 1.TW2868 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

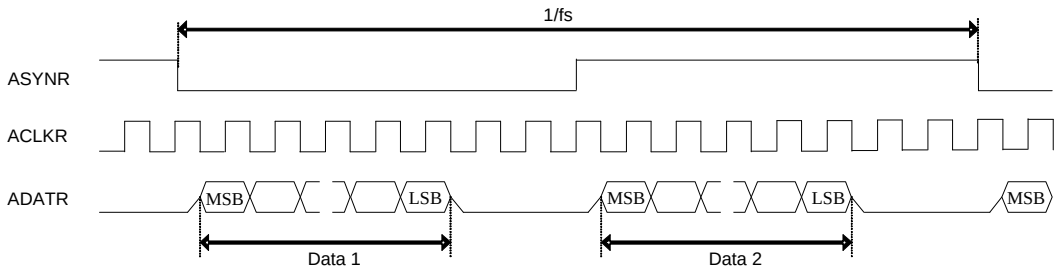


FIGURE 32. ACLKMASTER=0, RM_SYNC=0, ASYNROEN=1

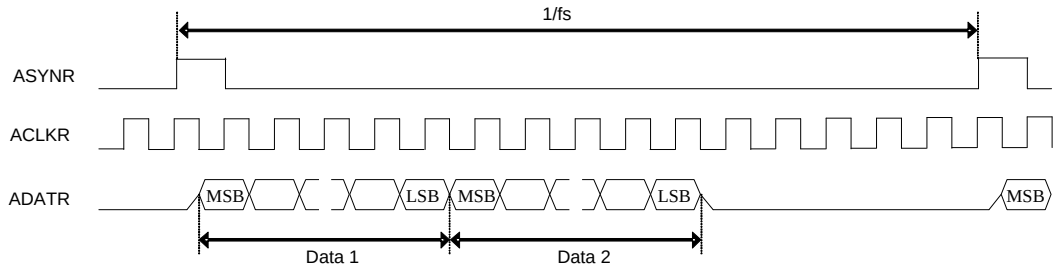


FIGURE 33. ACLKMASTER=0, RM_SYNC=1, ASYNROEN=1

ACLKP/ASYNP SLAVE MODE DATA INPUT TIMING

Following 8 data input timings are supported. ADATPDLY register need to be set up according to the difference of ADATP data input timings.Data1 is only used as default.MSB bit is the first input bit as default PBINSWAP=0.If PBINSWAP=1,LSB bit is the first input bit.

ASYNP is ACLKP falling edge triggered input

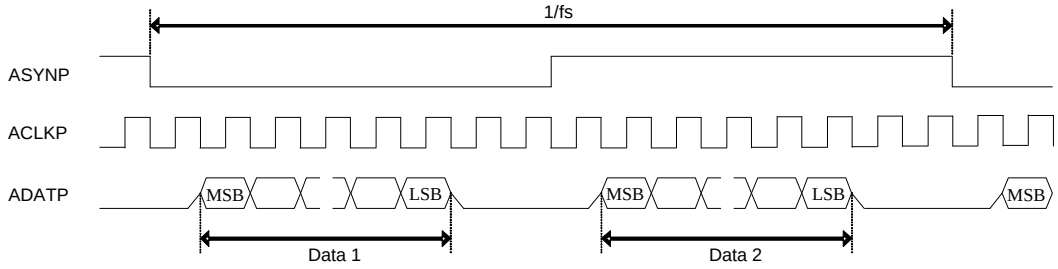


FIGURE 34. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

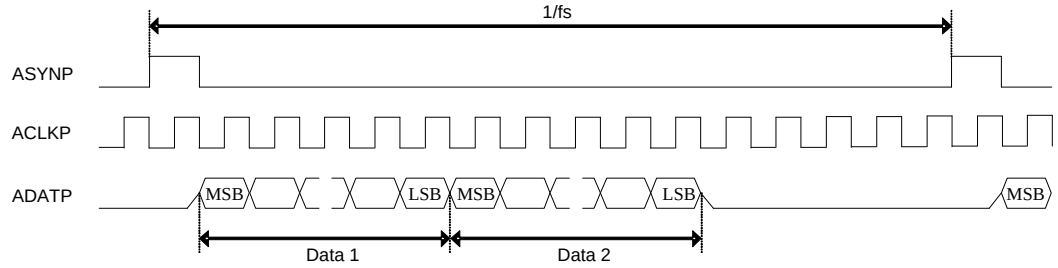


FIGURE 35. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

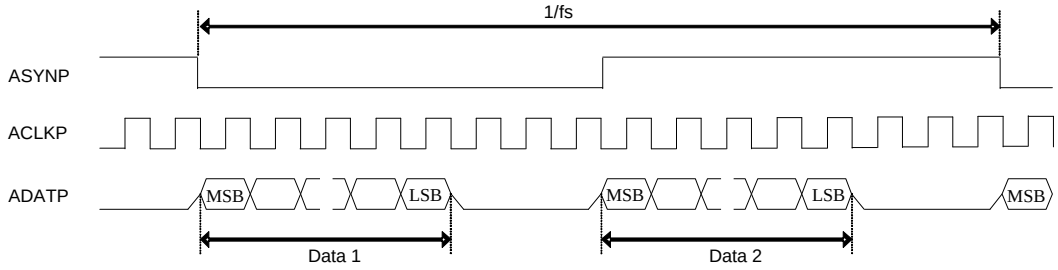


FIGURE 36. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

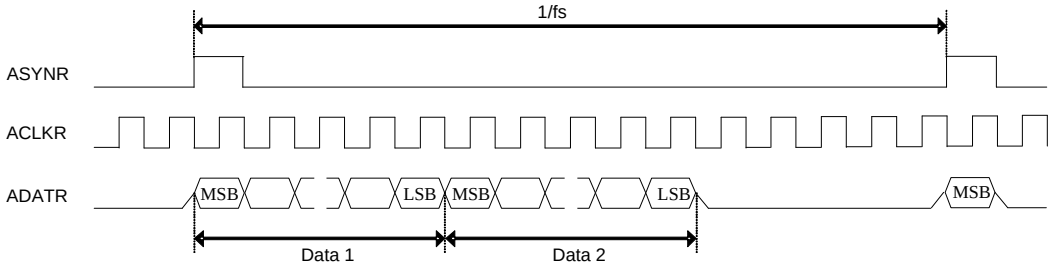


FIGURE 37. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

ASYNP is ACLKP rising edge triggered input.

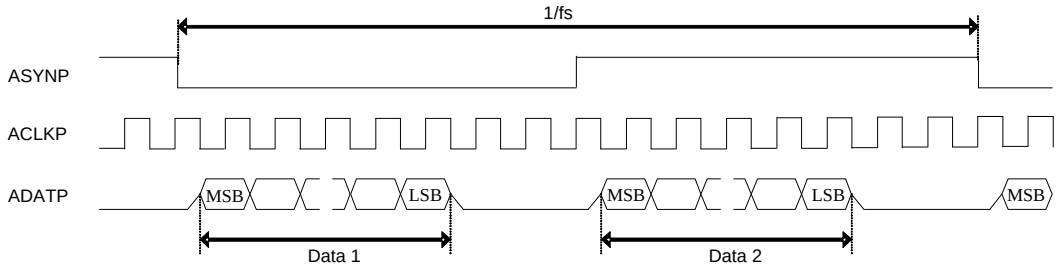


FIGURE 38. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

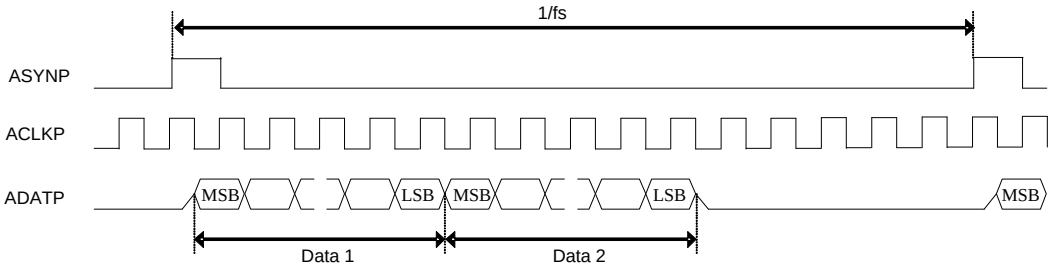


FIGURE 39. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

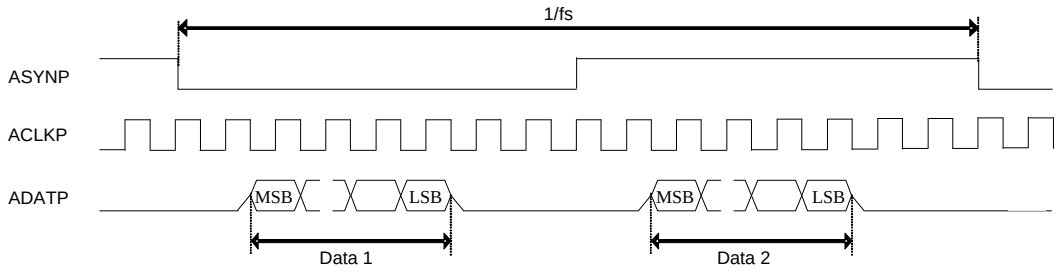


FIGURE 40. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

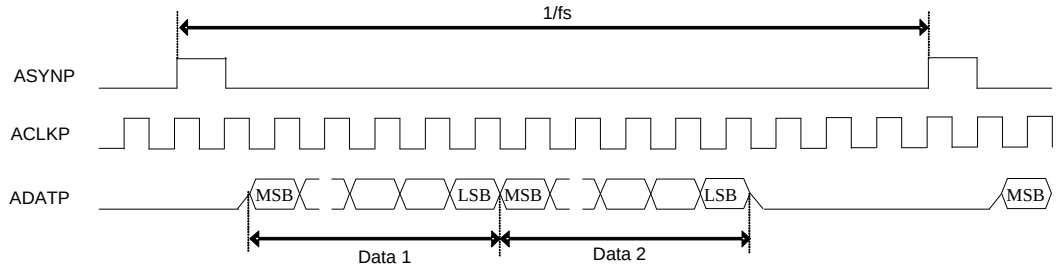


FIGURE 41. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

AUDIO CLOCK GENERATION

TW2868 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

ACKN = round (F AMCLK / F field), it gives the Audio master Clock per Field.
ACKI = round (F AMCLK / F 27MHz * 2^23), it gives the Audio master Clock Nominal increment.

Following table provides setting example of some common used audio frequency assuming Video Decoder system clock frequency of 27MHz.If ACLKRMASTER register bit is set to 1, following AMCLK is used as audio system clock inside TW2868.

If Slave Playback-in lock mode is required, ACKN=00100hex and PBREFEN=1 needs to be set up. The number of AMCLK clock per one ASYNP input cycle is locked (fixed) to 256 in this mode.

Frequency equation is “AMCLK (Freq) = 256 x ASYNP (Freq)”.

TABLE 8. 256XFS MODE: AIN5MD=0, AFS384=0.

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 16 KHz					
4.096	50	81920	1-40-00	1272583	13-6B-07
4.096	59.94	68335	1-0A-EF	1272583	13-6B-07
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

TABLE 9. 320XFS MODE: AIN5MD=1, AFS384=0. 44.1KHZ/48KHZ ARE NOT SUPPORTED

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
320 x 32 KHz					
10.24	50	204800	3-20-00	3181457	30-8B-91
10.24	59.94	170838	2-9B-56	3181457	30-8B-91
320 x 16 KHz					
5.12	50	102400	1-90-00	1590729	18-45-C9
5.12	59.94	85419	1-4D-AB	1590729	18-45-C9
320 x 8 KHz					
2.56	50	51200	C8-00	795364	C-22-E4
2.56	59.94	42709	A6-D5	795364	C-22-E4

TABLE 10. 384XFS MODE: AIN5MD=0, AFS384=1. 44.1KHZ/48KHZ ARE NOT SUPPORTED

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
384 x 32 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	381749	3A-41-15
384 x 16 KHz					
6.144	50	122880	1-E0-00	1908874	1D-20-8A
6.144	59.94	102503	1-90-67	1908874	1D-20-8A
384 x 8 KHz					
3.072	50	61440	F0-00	954437	E-90-45
3.072	59.94	51251	C8-33	954437	E-90-45

AUDIO CLOCK AUTO SETUP

If ACLKRMASTER=1 audio clock master mode is selected, and AFAUTO register is set to “1”,TW2868 set up ACKI register by AFMD register value automatically. ACKI control input in ACKG module block is automatically set up to the required value by the condition of AIN5MD and AFS384 register value.

TABLE 11. AFAUTO SETTING

AFAUTO	AFMD	ACKG MODULE ACKI CONTROL INPUT VALUE
1	0	8kHz mode value by each AIN5MD/AFS384 case.
1	1	16kHz mode value by each AIN5MD/AFS384 case.
1	2	32kHz mode value by each AIN5MD/AFS384 case.
1	3	44.1kHz mode value by each AIN5MD/AFS384 case.
1	4	48kHz mode value by each AIN5MD/AFS384 case.
0	X	ACKI register set up ACKI control input value.

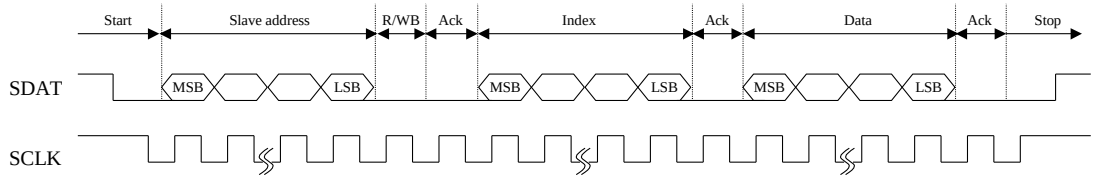
Host Interface

Serial Interface

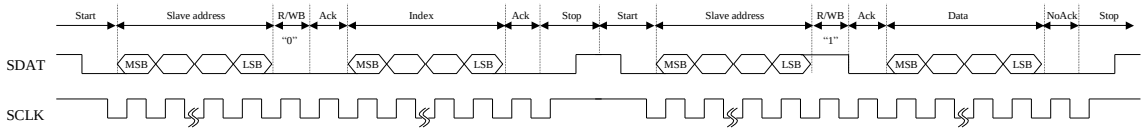
The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW2868 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDDO. Pull-up or Pull-down resistors on ALINKO pin while RSTB pin input is in low active state decides bit1 of Slave Address shows as SADD0 in following table.

SLAVE ADDRESS							R/W
0	1	0	1	0	0	1:Pull-up ALINKO 0:Pull-down ALINKO	1 = Read 0 = Write

The TW2868 supports auto index increments in write/read mode if the data are in sequential order. Data transfer rate on the bus is up to 400 Kbits/s.



(a) Write Mode



(b) Read Mode

FIGURE 42. TIMING CHART OF SERIAL INTERFACE

Interrupt Interface

The TW2868 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2868. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. Also, each channel of video and audio detection should be enabled by the AVDET1_ENA,A51DET_ENA,AVDET2_ENA,A52DET_ENA. Then,the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET1_STATE,A51DET_STATE,

AVDET2_STATE, A52DET_STATE. The Fig43 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading all enabled bits in AVDET1_STATE, A51DET_STATE, AVDET2_STATE,

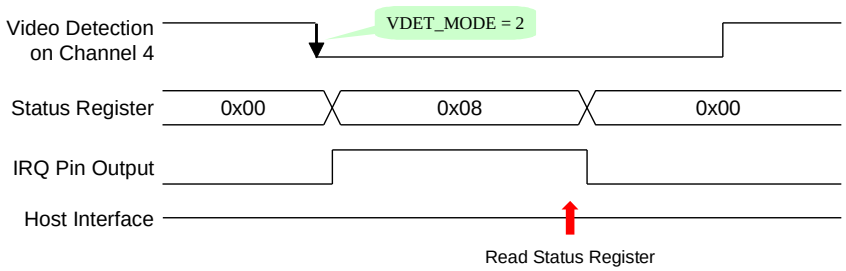
A52DET_STATE.If some bits are not enabled for interrupt requests in AVDET1_ENA,

A51DET_ENA, AVDET2_ENA, A52DET_ENA, those bits in AVDET1_STATE, A51DET_STATE,

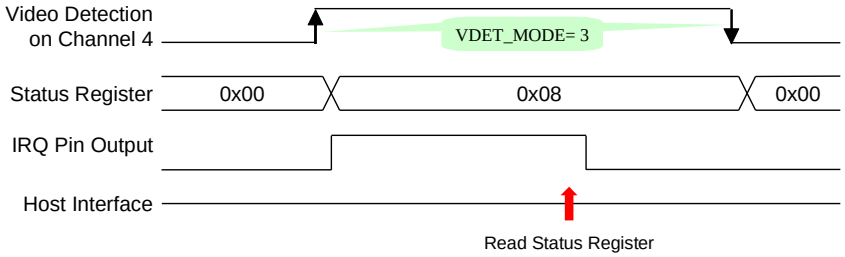
AVDET2_STATE, A52DET_STATE are not needed to be read to clear interrupt. When the VDET_MODE and/or ADET_MODE is 1 or 2, the status register AVDET1_STATE,

A51DET_STATE, AVDET2_STATE, A52DET_STATE will also be cleared automatically by reading AVDET_STATE, A51DET_STATE, AVDET2_STATE, A52DET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status registers AVDET1_STATE,

A51DET_STATE, AVDET2_STATE, A52DET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video and Audio Detection Flag Mode

FIGURE 43. TIMING DIAGRAM OF INTERRUPT INTERFACE

Squared Pixel mode operation

If FC27 register bit is set to 0,TW2868 works under Squared Pixel mode operation.XTI pin input on PAL-SQ mode should have either 59MHz(=29.5MHzx2) or 29.5MHz.Also,XTI pin input on NTSC-SQ mode should have either 49.086MHz(=24.543MHzx2) or 24.543MHz. HACTIVE register value should be 0x300(768dec) for PAL-SQ and 0x280(640dec) for NTSC-SQ. If Audio function is used with this Squared Pixel mode, ACKI register equations are as follows.

ACKI = round (F AMCLK / 29.5MHz * 2^{23}).....for PAL-SQ
ACKI = round (F AMCLK / 24.543MHz * 2^{23}).....for NTSC-SQ

Clock PLL

The TW2868 has built-in 2x/4x Clock PLL to generate 2xXTI clock or 4xXTI clock. If 54MHz is connected to XTI pin, SEL_X24 register need to be 0(2x, default).If 27MHz is connected to XTI pin, SEL_X24 register need to be 1(4x). If Clock PLL is not used, XTIMD register selects XTI input clock frequency mode by value=0/1/2 with Clock PLL power-down (PLL_PD=1). If Clock PLL is used (PLL_PD=0), XTIMD register needs to be set up to 3.

Control Register

PAGE MODE REGISTER MAP

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x40	PAGE	0	0	0	0	0	0	0	PAGE

PAGE0 REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN1	VIN2	VIN3	VIN4									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xE4	0xE7	0xEA	0xED	VSCALE_LO	VSCALE[7:0]							
0xE5	0xE8	0xEB	0xEE	SCALE_HI	VSCALE[11:8]				HSACLE[11:8]			
0xE6	0xE9	0xEC	0xEF	HSCALE_LO	HSCALE[7:0]							
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x41	ENCCTL	HZ50	INTERLACE	FSCSEL		COFF	PHALT	PDRST	PED
0x42	ENCTEST1	YBW		CBW		CBGEN	TCSEL		
0x43	ENCCLK	CKMST	ENCCKPOL	NONSTA	FRUN	YDEL			
0x44	ENCOUT	CVBS_YSEL	CVBS_CSEL	ENCTMODE					
0x45	SCH	SCH							
0x46	ENCYGAIN	ENCYGAIN							
0x47	ENCCGAIN	ENCCGAIN							
0x48	ENCSGAIN	ENCSGAIN							
0x49	ENCBGAIN	ENCBGAIN							
0x4A	ENCIREF	VDA_IREFC				VDA_IREFY			
0x4B	ENCTEST2	ENCVDOUT	TEST_DAC	VDA_PDC	VDA_PDY	VDAC_CKPOL	0	0	0
0x4C	EVDELAY	0	0	0	EVDELAY				
0x4D	EHDELAY	0	0	EHDELAY					
0x4E	ENC_LOOP	0	0	0	ENC_LOOP	0	LOOP_CH		
0x50	ADACCT1	ADACLK_INV	DAC_IB_DAC			0	DAC_IB_ADC		
0x51	DAC_LPFBIAS	DAC_LPFBIAS							
0x52	ADACLPF	0	LPF_SEL			BIAS_SEL	DAC_IB_OTA		
0x53	ANADACTEST	0	TAADCO			TVSENSE	ANADACTEST		
0x54	ASAVE1	0	0	DOUT_RST1	DIV_RST1	ACALEN1	ASAVE1		
0x58	VSENSE1*	VSENSE4B*	VSENSE3B*	VSENSE2B*	VSENSE1B*	VSENSE4A*	VSENSE3A*	VSENSE2A*	VSENSE1A*
0x59	PDBV1	PDBV4B	PDBV3B	PDBV2B	PDBV1B	PDBV4A	PDBV3A	PDBV2A	PDBV1A
0x5A	VSAVE	AVDSMD	VREF50M_AVDS	BIAS_AVDS		PD_BIAS	VSAVE		
0x5B	DS	VD4_DS	VD3_DS	VD2_DS	VD1_DS	0	0	CLKNO_DS	CLKPO_DS
0x5C	BGCTL1	0	0	BGCTL1	0	0	0	0	0
0x5D	CH2MISC2	NKILL_2	PKILL_2	SKILL_2	CBAL_2	FCS_2	LCS_2	CCS_2	BST_2
0x5E	CH3MISC2	NKILL_3	PKILL_3	SKILL_3	CBAL_3	FCS_3	LCS_3	CCS_3	BST_3
0x5F	CH4MISC2	NKILL_4	PKILL_4	SKILL_4	CBAL_4	FCS_4	LCS_4	ICCS_4	BST_4

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x60	PLL1	0	PLL_PD	PLLIREF	SEL_X24	LP_X4		CP_X4	
0x61	PLL2	0	0	0	DECOSC	CKOUTSEL		XTIMD	
0x65	VDOEB	0	0	0	0	VD4OEB	VD3OEB	VD2OEB	VD1OEB
0x66	CK13	VD4_27C	VD3_27C	VD2_27C	VD1_27C	0	0	CKNO_13	CKPO_13

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x70	ACLKPOL	0	S2I_8BIT	ACLKRPOL	ACLKPPOL	AFAUTO	AFMD		
0x71	AINCTL	I2S8MODE	MASCKMD	PBINSWAP	ASYNRDLY	ASYNPDLY	ADATPDLY	INLAWMD	
0x72	MRATIOMD	MRATIOMD	ADACTEST	AOFFCORE	DAORATIO	DAOGAIN			
0x73	A51DET_ENA	0	0	0	0	0	AIN5FORM	AINTPOFF	A51DET_ENA
0x74	A51DETST	0	0	0	0	0	0	0	A51DET_STATE*
0x75	AADC51OFS_H	0	0	0	0	0	0	AADC51OFS[9:8]	
0x76	AADC51OFS_L	AADC51OFS[7:0]							
0x77	AUD51ADC_H	0	0	0	0	0	0	AUD51ADC[9:8]	
0x78	AUD51ADC_L	AUD51ADC[7:0]							
0x79	ADJAADC51_H	0	0	0	0	0	0	ADJAADC51[9:8]	
0x7A	ADJAADC51_L	ADJAADC51[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x7B	I2SO_RSEL	0	0	0	I2SO_RSEL				
0x7C	I2SO_LSEL	0	0	0	I2SO_LSEL				
0x7D	RECSEL5	RECSEL54		RECSEL53		RECSEL52		RECSEL51	
0x7E	ADATMI2S	A5OUTOFF	ADATMI2SOEN	MUTEA5	ADET_TH51[4:0]				
0x7F	AIGAIN51	AIGAIN51				MIX_RATIO51			
0x80	SRST1	0	ENCRST	AUDIORST	VOUTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x81	ACNTL	0	IREF	VREF	0	CLKPDN	0	YFLEN	0
0x82	ACNTL2	CTEST	YCLEN	0	AFLTEN	GTEST	VLPF	CKLY	CKLC
0x83	CNTRL1	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY
0x84	CKHY	GMEN	CKHY		HSDLY				
0x85	SHCOR	SHCOR				0	0	0	0
0x86	CORING	CTCOR		CCOR		VCOR		CIF	
0x87	CLMPG	CLPEND				CLPST			
0x88	IAGC	NMGAIN				WPGAIN			0
0x89	AIN5MD	0	0	ACLKR128	ACLKR64	AFS384	AIN5MD	0	1
0x8A	PEAKWT	PEAKWT							
0x8B	CLMPL	CLMPLD	CLMPL						
0x8C	SYNCT	SYNCTD	SYNCT						
0x8D	MISSCNT	MISSCNT				HSWIN			
0x8E	PCLAMP	PCLAMP							
0x8F	VCNTL1	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT
0x90	VCNTL2	BSHT			VSHT				

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x91	CKILL	CKILMAX		CKILMIN					
0x92	COMB	COMBMD	HTL			VTL			
0x93	LDLY	CKLM	YDLY			HPF_RES			
0x94	MISC1	HPLC	ENCNT	PALC	SDET	TBCEN	BYPASS	SYOUT	0
0x95	LOOP	HPM		ACCT		SPM		CBW	
0x96	MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST
0x97	CLMD	FRM		YNR		CLMD		PSP	
0x98	HSLOWCTL	0	HSBEGIN[2:0]			0	HSEND[2:0]		
0x99	HSBEGIN	HSBEGIN[10:3]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x9A	HSEND	HSEND[10:3]							
0x9B	OVSDLY	OVSDLY							
0x9C	OVSEND	HASYNC	OFDLY			VSMODE	OVSEND		
0x9D	HBLEN	HBLEN							
0x9E	NOVID	0	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656
0x9F	CLK_DEL	CLKNO_DEL				CLKPO_DEL			
0xA8	HFLT21	HFLT2				HFLT1			
0xA9	HFLT43	HFLT4				HFLT3			
0xAA	AGCEN	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB	AGCGAIN1	AGCGAIN1[7:0]							
0xAC	AGCGAIN2	AGCGAIN2[7:0]							
0xAD	AGCGAIN3	AGCGAIN3[7:0]							
0xAE	AGCGAIN4	AGCGAIN4[7:0]							
0xAF	VSHP21	0	VSHP2			0	VSHP1		
0xB0	VSHP43	0	VSHP4			0	VSHP3		
0xB1	NOVIDMODE	CH8IDEN	0	NOVIDMODE		0	0	0	0
0xB2	VDLOSSOE	0	0	0	0	0	0	0	VDLOSSOE
0xB3	AADCOFS_H	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0xB4	AADC1OFS_L	AADC1OFS[7:0]							
0xB5	AADC2OFS_L	AADC2OFS[7:0]							
0xB6	AADC3OFS_L	AADC3OFS[7:0]							
0xB7	AADC4OFS_L	AADC4OFS[7:0]							
0xB8	AUDADC_H*	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9	AUD1ADC_L*	AUD1ADC[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xBA	AUD2ADC_L*	AUD2ADC[7:0]							
0xBB	AUD3ADC_L*	AUD3ADC[7:0]							
0xBC	AUD4ADC_L*	AUD4ADC[7:0]							
0xBD	ADJAADC_H*	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE	ADJAADC1_L*	ADJAADC1[7:0]							
0xBF	ADJAADC2_L*	ADJAADC2[7:0]							
0xC0	ADJAADC3_L*	ADJAADC3[7:0]							
0xC1	ADJAADC4_L*	ADJAADC4[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xC8	MPP_MODE21	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0xC9	MPP_MODE43	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		
0xCB	POLMPP1	POLMPP4	POLMPP3	POLMPP2	POLMPP1	0	0	0	0
0xCE	ANAPWDN1	AAUTOMUTE	0	A_DAC_PWDN	A_ADC_PWDN	V4_ADC_PWDN	V3_ADC_PWDN	V2_ADC_PWDN	V1_ADC_PWDN
0xCF	SMD	SMD		0	0	0	0	0	0
0xD0	AIGAIN21	AIGAIN2				AIGAIN1			
0xD1	AIGAIN43	AIGAIN4				AIGAIN3			
0xD2	R_MULTCH	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH	
0xD3	R_SEQ10	R_SEQ_1				R_SEQ_0			
0xD4	R_SEQ32	R_SEQ_3				R_SEQ_2			
0xD5	R_SEQ54	R_SEQ_5				R_SEQ_4			
0xD6	R_SEQ76	R_SEQ_7				R_SEQ_6			
0xD7	R_SEQ98	R_SEQ_9				R_SEQ_8			
0xD8	R_SEQBA	R_SEQ_B				R_SEQ_A			
0xD9	R_SEQDC	R_SEQ_D				R_SEQ_C			
0xDA	R_SEQFE	R_SEQ_F				R_SEQ_E			

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xDB	AMASTER	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER
0xDC	MIX_MUTE	LAWMD		MIX_DERATIO	MIX_MUTE				
0xDD	MIX_RATIO21	MIX_RATIO2				MIX_RATIO1			
0xDE	MIX_RATIO43	MIX_RATIO4				MIX_RATIO3			
0xDF	MIX_RATIOP	1	0	0	0	MIX_RATIOP			
0xE0	MIX_OUTSEL	VADCCKPOL	AADCCKPOL	ADACCKPOL	MIX_OUTSEL				

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xE1	ADET	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0xE2	ADET_TH21	ADET_TH2[3:0]				ADET_TH1[3:0]			
0xE3	ADET_TH43	ADET_TH4[3:0]				ADET_TH3[3:0]			
0xF0	ACKI_L	ACKI[7:0]							
0xF1	ACKI_M	ACKI[15:8]							
0xF2	ACKI_H	0	0	ACKI[21:16]					
0xF3	ACKN_L	ACKN[7:0]							
0xF4	ACKN_M	ACKN[15:8]							
0xF5	ACKN_H	0	0	0	0	0	0	ACKN[17:16]	
0xF6	SDIV	0	0	SDIV					
0xF7	LRDIV	0	0	LRDIV					
0xF8	ACCNTL	APZ	APG			0	ACPL	SRPH	LRPH
0xF9	VMISC	LIM16	PBREFEN	YCBCR422	HA656MD	VBI_FRAM	CNTL656	VSCL_SYNC	HA_EN
0xFA	CLKOCTL	VSCL_ENA	OE	CLKNO_OEB	CLKPO_OEB	CLKNO_MD		CLKPO_MD	
0xFB	AVDET_MODE	CLKNO_POL	CLKPO_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE	
0xFC	AVDET1_ENA	AVDET1_ENA							
0xFD	AVDET1_STATE*	AVDET1_STATE							
0xFE	TEST	DEV_ID[6:5]*		0	0	0	TEST		
0xFF	DEV_ID*	DEV_ID[4:0]*					REV_ID		

PAGE1 REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN5	VIN6	VIN7	VIN8									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xE4	0xE7	0xEA	0xED	VSCALE_LO	VSCALE[7:0]							
0xE5	0xE8	0xEB	0xEE	SCALE_HI	VSCALE[11:8]				HSACLE[11:8]			
0xE6	0xE9	0xEC	0xEF	HSCALE_LO	HSCALE[7:0]							
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x54	ASAVE2	0	0	DOUT_RST2	DIV_RST2	ACALEN2	ASAVE2		
0x58	VSENSE2*	VSENSE8B*	VSENSE7B*	VSENSE6B*	VSENSE5B*	VSENSE8A*	VSENSE7A*	VSENSE6A*	VSENSE5A*
0x59	PDBV2	PDBV8B	PDBV7B	PDBV6B	PDBV5B	PDBV8A	PDBV7A	PDBV6A	PDBV5A
0x5C	BGCTL2	0	0	BGCTL2	0	0	0	0	0
0x5D	CH6MISC2	NKILL_6	PKILL_6	SKILL_6	CBAL_6	FCS_6	LCS_6	CCS_6	BST_6
0x5E	CH7MISC2	NKILL_7	PKILL_7	SKILL_7	CBAL_7	FCS_7	LCS_7	CCS_7	BST_7
0x5F	CH8MISC2	NKILL_8	PKILL_8	SKILL_8	CBAL_8	FCS_8	LCS_8	ICCS_8	BST_8
0x60	VDMD	VD4MD		VD3MD		VD2MD		VD1MD	
0x61	VD1O12SEL	VD1O2SEL				VD1O1SEL			

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x62	VD1O34SEL	VD1O4SEL				VD1O3SEL			
0x63	VD2O12SEL	VD2O2SEL				VD2O1SEL			
0x64	VD2O34SEL	VD2O4SEL				VD2O3SEL			
0x65	VD3O12SEL	VD3O2SEL				VD3O1SEL			
0x66	VD3O34SEL	VD3O4SEL				VD3O3SEL			
0x67	VD4O12SEL	VD4O2SEL				VD4O1SEL			
0x68	VD4O34SEL	VD4O4SEL				VD4O3SEL			
0x73	A52DET_ENA	0	0	0	0	0	0	0	A52DET_ENA
0x74	A52DETST	0	0	0	0	0	0	0	A52DET_STATE*
0x75	AADC52OFS_H	0	0	0	0	0	0	AADC52OFS[9:8]	
0x76	AADC52OFS_L	AADC52OFS[7:0]							
0x77	AUD52ADC_H	0	0	0	0	0	0	AUD52ADC[9:8]	
0x78	AUD52ADC_L	AUD52ADC[7:0]							
0x79	ADJAADC52_H	0	0	0	0	0	0	ADJAADC52[9:8]	
0x7A	ADJAADC52_L	ADJAADC52[7:0]							
0x7E	ADET_52	0	0	MUTEA52	ADET_TH52[4:0]				
0x7F	AIGAIN52	AIGAIN52				MIX_RATIO52			
0x80	SRST2	0	0	0	0	VDEC8RST	VDEC7RST	VDEC6RST	VDEC5RST
0x96	MISC22	NKILL_5	PKILL_5	SKILL_5	CBAL_5	FCS_5	LCS_5	CCS_5	BST_5

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xA8	HFLT65	HFLT5				HFLT5			
0xA9	HFLT87	HFLT8				HFLT7			
0xAA	AGCEN2	AGCEN8	AGCEN7	AGCEN6	AGCEN5	AGCGAIN8[8]	AGCGAIN7[8]	AGCGAIN6[8]	AGCGAIN5[8]
0xAB	AGCGAIN5	AGCGAIN5[7:0]							
0xAC	AGCGAIN6	AGCGAIN6[7:0]							
0xAD	AGCGAIN7	AGCGAIN7[7:0]							
0xAE	AGCGAIN8	AGCGAIN8[7:0]							
0xAF	VSHP65	0	VSHP6			0	VSHP5		
0xB0	VSHP87	0	VSHP8			0	VSHP7		
0xB3	AADCOFS_H	AADC8OFS[9:8]		AADC7OFS[9:8]		AADC6OFS[9:8]		AADC5OFS[9:8]	
0xB4	AADC5OFS_L	AADC5OFS[7:0]							
0xB5	AADC6OFS_L	AADC6OFS[7:0]							
0xB6	AADC7OFS_L	AADC7OFS[7:0]							
0xB7	AADC8OFS_L	AADC8OFS[7:0]							

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xB8	AUDADC_H*	AUD8ADC[9:8]		AUD7ADC[9:8]		AUD6ADC[9:8]		AUD5ADC[9:8]	
0xB9	AUD5ADC_L*	AUD5ADC[7:0]							
0xBA	AUD6ADC_L*	AUD6ADC[7:0]							
0xBB	AUD7ADC_L*	AUD7ADC[7:0]							
0xBC	AUD8ADC_L*	AUD8ADC[7:0]							
0xBD	ADJAADC_H*	ADJAADC8[9:8]		ADJAADC7[9:8]		ADJAADC6[9:8]		ADJAADC5[9:8]	
0xBE	ADJAADC5_L*	ADJAADC5[7:0]							
0xBF	ADJAADC6_L*	ADJAADC6[7:0]							
0xC0	ADJAADC7_L*	ADJAADC7[7:0]							
0xC1	ADJAADC8_L*	ADJAADC8[7:0]							
0xC8	MPP_MODE65	GPP_VAL6	MPP_MODE6			GPP_VAL5	MPP_MODE5		
0xC9	MPP_MODE87	GPP_VAL8	MPP_MODE8			GPP_VAL7	MPP_MODE7		
0xCB	POLMPP	POLMPP8	POLMPP7	POLMPP6	POLMPP5	0	0	0	0

Address	Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0xCE	ANAPWDN2	0	0	0	0	V8_ADC_PWDN	V7_ADC_PWDN	V6_ADC_PWDN	V5_ADC_PWDN
0xD0	AIGAIN65	AIGAIN6				AIGAIN5			
0xD1	AIGAIN87	AIGAIN8				AIGAIN7			
0xDC	MIX_MUTE2	0	0	MIX_DERATIO2	MIX_MUTE2				
0xDD	MIX_RATIO65	MIX_RATIO6				MIX_RATIO5			
0xDE	MIX_RATIO87	MIX_RATIO8				MIX_RATIO7			
0xE1	ADET2	0	0	0	0	ADET_TH8[4]	ADET_TH7[4]	ADET_TH6[4]	ADET_TH5[4]
0xE2	ADET_TH65	ADET_TH6[3:0]				ADET_TH5[3:0]			
0xE3	ADET_TH87	ADET_TH8 [3:0]				ADET_TH7[3:0]			
0xFC	AVDET2_ENA	AVDET2_ENA							
0xFD	AVDET2_STATE*	AVDET2_STATE							
0xFF	DEV_ID*	DEV_ID[4:0]*				REV_ID			

NOTE: *** READ ONLY REGISTERS**

PAGE ACCESS

0X40 – PAGE MODE REGISTER

TW2868 has two page register mapping. Each page map has address range 0x00-0xFF.
0x40 address is accessible from both page0 state and page1 state. 0x40[0] bit shows current register map access mode.

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R		00
0	PAGE	R/W	0 = page0 access mode.page0 registers can be read/written. 1 = page1 access mode.page1 registers can be read/written.	0

PAGE0 REGISTER DESCRIPTION

Followings show page0 registers. These registers can be accessed when 0x40[0] is 0.

0X00(VIN1)/0X10(VIN2)/0X20(VIN3)/0X30(VIN4) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(VIN1)/0X11(VIN2)/0X21(VIN3)/0X31(VIN4) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(VIN1)/0X12(VIN2)/0X22(VIN3)/0X32(VIN4) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(VIN1)/0X13(VIN2)/0X23(VIN3)/0X33(VIN4) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with ‘0’ having no effect on the output image. 1 through 15 provides sharpness enhancement with ‘F’ being the strongest.	1

0X04(VIN1)/0X14(VIN2)/0X24(VIN3)/0X34(VIN4) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(VIN1)/0X15(VIN2)/0X25(VIN3)/0X35(VIN4) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(VIN1)/0X16(VIN2)/0X26(VIN3)/0X36(VIN4) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(VIN1)/0X17(VIN2)/0X27(VIN3)/0X37(VIN4) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(VIN1)/0X18(VIN2)/0X28(VIN3)/0X38(VIN4) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(VIN1)/0X19(VIN2)/0X29(VIN3)/0X39(VIN4) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(VIN1)/0X1A(VIN2)/0X2A(VIN3)/0X3A(VIN4) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0X0B(VIN1)/0X1B(VIN2)/0X2B(VIN3)/0X3B(VIN4) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C(VIN1)/0X1C(VIN2)/0X2C(VIN3)/0X3C(VIN4) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(VIN1)/0X1D(VIN2)/0X2D(VIN3)/0X3D(VIN4) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(VIN1)/0X1E(VIN2)/0X2E(VIN3)/0X3E(VIN4) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(VIN1)/0X1F(VIN2)/0X2F(VIN3)/0X3F(VIN4) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I).	1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
			0 = disable recognition.	
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0XE4(VIN1)/0XE7(VIN2)/0XEA(VIN3)/0XED(VIN4) – VERTICAL SCALING REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00

0XE5(VIN1)/0XE8(VIN2)/0XEB(VIN3)/0XEE(VIN4) – SCALING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0XE6(VIN1)/0XE9(VIN2)/0XEC(VIN3)/0XEF(VIN4) – HORIZONTAL SCALING REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00

0XA4(VIN1)/0XA5(VIN2)/0XA6(VIN3)/0XA7(VIN4) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 2A

0XC4(VIN1)/0XC5(VIN2)/0XC6(VIN3)/0XC7(VIN4) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator(Test purpose only)	X

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	00b
6	ENCRST	W	An 1 written to this bit resets the Digital Encoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
5	AUDIORST	W	A 1 written to this bit resets the Audio portion to its default state but all register content remains unchanged. This bit is self-resetting.	0
4	VOUTRST	W	A 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting.	0
3	VDEC4RST	W	A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC3RST	W	A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

BIT	FUNCTION	R/W	DESCRIPTION	RESET
1	VDEC2RST	W	A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC1RST	W	A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X81 – ANALOG CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference increase 30%.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	Reserved	R		0
3	CLKPDN	R/W	0 = Normal clock operation. 1 = All 8Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKPO and CLKNO) are still active.	0
2	Reserved	R		0
1	YFLEN	R/W	All VIN1/2/3/4/5/6/7/8 video anti-alias filter control 1 = enable 0 = disable	1
0	Reserved	R		0

0X82 – ANALOG CONTROL REISTER2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control for debugging use.(Test purpose only)	0
6	YCLEN	R/W	1 = Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
5	CKIPOL	R/W	27MHz clock output signal timing. This bit is effective when 54MHz rate output data is used and 27MHz clock is used in CLKPO or CLKNO pin. 0: change by 54MHz clock falling edge internally. 1: change by 54MHz clock rising edge internally.	0
4	Reserved	R		0
3	GTEST	R/W	1 = Test (Test purpose only) 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0	CKLC	R/W	Clamping current control 2.	0

0X83 – CONTROL REGISTER I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter for NTSC and PAL (recommended). Not for SECAM. 0 = Notch filter. For SECAM.	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GMEN	R/W	Reserved.	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	00b
4-0	HSDLY	RW	Reserved for test.	00h

0X85 – VERTICAL SHARPNESS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3-0	Reserved	R		0

0X86 – CORING CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X87 – CLAMPING GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0X88 – INDIVIDUAL AGC GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	Reserved	R	Reserved	0

0X8A – WHITE PEAK THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0X8B– CLAMP LEVEL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0X8C– SYNC AMPLITUDE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X8D – SYNC MISS COUNT REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR mode detection threshold.	4

0X8E – CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

0X8F – VERTICAL CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical countdown mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = short 0 = normal	0

0X90 – VERTICAL CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0X91 – COLOR KILLER LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0X92 – COMB FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HTL	R/W	0 = adaptive mode 1 = fixed comb	0
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X93 – LUMA DELAY AND H FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	Reserved	RW		0h

0X94 – MISCELLANEOUS CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	TBC_EN	R/W	1 = Internal TBC enable. Total pixel per line on Video active line is always 858x2 for NTSC/PAL-M (60Hz) and 864x2 for PAL/SECAM (50Hz). 0 = TBC off.	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	Reserved	R	Reserved	0

0X95 – LOOP CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X97 – CLAMP MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto, 2 = default to 60Hz, 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None, 1 = smallest, 2 = small, 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top, 1 = Auto, 2 = Pedestal, 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0X98 – HSLOWCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6-4	HSBEGIN[2:0]	R/W	HSYNC Start position Control Bit2-0.	00
3	Reserved	R/W		0
2-0	HSEND[2:0]	R/W	HSYNC End position Control Bit2-0.	00

0X99 – HSBEGIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSBEGIN[10:3]	R/W	HSYNC Start position Control Bit10-3.	28

0X9A – HSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSEND[10:3]	R/W	HSYNC End position Control Bit10-3.	44

0X9B – OVSDLY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	OVSDLY	R/W	VSYNC Start position. Control H position on VSYNC start.	44

0X9C – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC	R/W	1: the length of EAV to SAV is set up and fixed by HBLEN registers. 0: the length of SAV to EAV is set up and fixed by HACTIVE registers.	0
6-4	OFDLY	R/W	FIELD output delay. 0h:0H line delay FIELD output.(601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h: Reserved.	2
3	VSMODE	R/W	1: VSYNC output is HACTIVE-VSYNC mode. 0: VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0X9D – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLEN	R/W	These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720 If Reg0x0E[3](ATRIG for VIN1) is set to 0,this value changes into 8Ah or 90h at auto video format detection initial time automatically according to VIN1 video detection status.	90h

0X9E – NOVID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	0
6	FC27	R/W	1: normal ITU-R656 operation 0: Squared Pixel mode.	1
5-4	CHID_MD	R/W	Select the Channel ID format for time-multiplexed output 0 No channel ID (default) 1 CHID with the specific ITU-R BT.656 sync Code 2 CHID with the specific horizontal blanking code 3 CHID with the specific ITU-R BT.656 sync & horizontal blanking code	0
3	NOVID_656	R/W	0:Normal ITU-R BT.656 SA/EAV(default) 1:AN optional set of ITU-R BT.656 SAV/EAV code for No-video status	0
2	EAVSWAP	R/W	1: EAV-SAV code is swapped. 0:EAV-SAV code is not swapped(standard 656 output mode)	0
1	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code. 1: Standard ITU-R656 code format. (It's also VIP task-A code format.) 0: Old VIP task-B code format.	1
0	NTSC656	R/W	1: Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0

0X41 – VIDEO ENCODER STANDARD CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HZ50	R/W	1 = 50Hz field rate 0 = 60Hz field rate	0
6	INTERLACE	R/W	1 = Interlaced output 0 = Non-interlaced output	1
5-4	FSCSEL	R/W	FSCSEL frequency selection 00= NTSC-M, 01= PAL-B,10= PAL-M,11= PAL-N	0
3	COFF	R/W	1 = Turn off chroma output 0 = chroma output on	0
2	PHALT	R/W	1 = Alternating burst for PAL 0 = NTSC	0
1	PDRST	R/W	1 = PAL phase reset every 8 fields 0 = No phase reset	0
0	PED	R/W	1 = Pedestal enabled (NTSC-M) 0 = disabled	0

0X42 – VIDEO ENCODER TEST GENERATION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	YBW	R/W	Luminance bandwidth control. 2,3 = Normal BW 1,0 = not available	2
5-4	CBW	R/W	Chrominance bandwidth control. Refer to filter diagram.	1
3	CBGEN	R/W	1 = Enable internal test pattern generation 0 = Disabled	0
2-0	TCSEL	R/W	Test pattern selection. 0 = 75% color bar 1 = White 2 = Yellow 3 = Cyan 4 = Green 5 = Magenta 6 = Red 7 = Blue	0

0X43 – VIDEO ENCODER CLOCK AND DELAY CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKMST	R/W	1 = Use internal 27MHz clock as encoder clock. ENCLK Pin is clock output. 0 = Use input clock as encoder clock. ENCLK pin is clock input.	0
6	CKPOL	R/W	It controls the clock polarity for latching input data	0
5	NONSTA	R/W	1 = Non-standard 656 input (Internal use only) 0 = Normal 656 input	0
4	FRUN	R/W	0 = Encoder timing generation bases on input 1 = Internal generated timing for built-in test pattern	0
3-0	YDEL	R/W	Y delay adjustment relative to Cb/Cr. The center value is 8.8h should be set up normally.	8

0X44 – VIDEO ENCODER OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CVBS_YSEL	R/W	DAC1 output control 1 = Luma output 0 = CVBS output	0
6	CVBS_CSEL	R/W	DAC2 output control 1 = Chroma output 0 = CVBS output	0
5-0	TMODE	R/W	Encoder test mode. For internal use only.	0

0X45 – VIDEO ENCODER SCH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
6-0	SCH	R/W	Sub-carrier phase control. For internal use only.	38h

0X46 – VIDEO ENCODER YGAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	YGAIN	R/W	Luminance amplitude gain control. The 0dB gain is 0x80.	80h

0X47 – VIDEO ENCODER CGAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CGAIN	R/W	Chrominance amplitude gain control, The 0dB gain is 0x80.	80h

0X48 – VIDEO ENCODER SGAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SGAIN	R/W	Sync pulse amplitude gain control. The 0dB gain is 0x80	80h

0X49 – VIDEO ENCODER BGAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BGAIN	R/W	Burst amplitude gain control. The 0dB gain is 0x80	80h

0X4A – VIDEO DAC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VDAIREFC	R/W	C Video DAC IREF control	F
3-0	VDAIREFY	R/W	Y Video DAC IREF control	F

0X4B – VIDEO DAC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ENCVDOUT	R/W	Test purpose only.	0
6	TESTDAC	R/W	Test purpose only.	0
5	VDA_PDC	R/W	1:C Video DAC power down mode,0:normal mode	1
4	VDA_PDY	R/W	1: Y Video DAC power down mode, 0: normal mode.	1
3	VDACCKPOL	R/W	1:Analog Video DAC input clock polarity inverse: 0: not inverse.	0
2-0	Reserved	R		0

0X4C – VIDEO ENCODER VDELAY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0
4-0	EVDELAY	R/W	Video Encoder output Vertical position control.	0

0X4D – VIDEO ENCODER HDELAY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0
4-0	EHDELAY	R/W	Video Encoder output Horizontal position control.	0

0X4E – ENC_LOOP

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0
4	ENC_LOOP	R/W	Video Decoder to Video Encoder loop test mode. 1: Video Decoder output direct connects to Video Encoder input for Test purpose only. LOOP_CH register select Video Ch number to be connected to Video Encoder in this mode. This function is internal test use only. 0: Normal Video Decoder & Video Encoder operation. Video Decoder and Video Encoder are working independently.	0
3	Reserved	R		0
2-0	LOOP_CH	R/W	Select Video Ch number to be connected to Video Encoder directly when ENC_LOOP register is set to 1. 0: VIN1 Video Data. 1: VIN2 Video Data 2: VIN3 Video Data. 3. VIN4 Video Data. 4. VIN5 Video Data. 5. VIN6 Video Data. 6. VIN7 Video Data. 7. VIN8 Video Data.	0

0X9F – CLOCK OUTPUT DELAY CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLKNO_DEL	R/W	Control the clock delay of CLKNO pin. 0h/1h/3h/7h/Fh values are effective. 1h:about 2ns more delay, 3h: about 4ns more delay, 7h:about 6ns more delay, Fh: about 7ns more delay	0h
3-0	CLKPO_DEL	R/W	Control the clock delay of CLKPO pin. 0h/1h/3h/7h/Fh values are effective. 1h:about 2ns more delay, 3h: about 4ns more delay, 7h:about 6ns more delay, Fh: about 7ns more delay	0h

NOTE: * CLKNO_POL/CLKPO_POL CONTROLS HAVE MORE BETTER & EASY CLOCK MARGIN ADJUSTMENT.
USE CLKNO_POL/CLKPO_POL AT FIRST NORMALLY, ESPECIALLY FOR 27MHZ/54MHZ DATA OUTPUT APPLICATION.
CLKNO_DEL/CLKPO_DEL ARE SOMETIMES REQUIRED FOR 108MHZ DATA OUTPUT INTERFACE.
CLKNO_DEL/CLKPO_DEL ARE NOT REQUIRED FOR 27MHZ/54MHZ DATA OUTPUT IN MOST CASES.

0XA8 ~0XA9 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

0XA8 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT2	R/W	Pre-filter selection for Video VIN1/VIN2 horizontal scaler. If each HSCALE [11:8] =1, HFLT [3:0] controls the peaking function. If each HSCALE [11:8]>1, HFLT [2:0] function is bellow.	0h
3-0	HFLT1	R/W	1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image.	0h

0XA9 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HFLT4	R/W	Pre-filter selection for Video VIN3/VIN4 horizontal scaler. If each HSCALE [11:8] =1, HFLT [3:0] controls the peaking function. If each HSCALE [11:8]>1, HFLT [2:0] function is bellow.	0h
3-0	HFLT3	R/W	1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image.	0h

VIDEO AGC CONTROL

0XAA – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AGCEN4	R/W	Select Video AGC loop function on VIN4 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4	0
6	AGCEN3	R/W	Select Video AGC loop function on VIN3 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3	0
5	AGCEN2	R/W	Select Video AGC loop function on VIN2 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2	0
4	AGCEN1	R/W	Select Video AGC loop function on VIN1 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN1	0
3	AGCGAIN4[8]	R/W	AGCGAIN4 MSB bit	0
2	AGCGAIN3[8]	R/W	AGCGAIN3 MSB bit	0
1	AGCGAIN2[8]	R/W	AGCGAIN2 MSB bit	0
0	AGCGAIN1[8]	R/W	AGCGAIN1 MSB bit	0

0XAB – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN1[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN1 bit7-0.	F0h

0XAC – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN2[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN2 bit7-0.	F0h

0XAD – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN3[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN3 bit7-0.	F0h

0XAE – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN4[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGC GAIN4 bit7-0.	F0h

0XAF – VERTICAL PEAKING LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP2	R/W	Select VIN2 Video Vertical peaking level. (*) 0: none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP1	R/W	Select VIN1 Video Vertical peaking level. (*) 0: none. 7 : highest	0
*Note: VSHP must be set to '0' if page0 Reg0x83 COMB = 0.				

0XB0 – VERTICAL PEAKING LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP4	R/W	Select VIN4 Video Vertical peaking level. (*) 0: none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP3	R/W	Select VIN3 Video Vertical peaking level. (*) 0: none. 7 : highest	0
*Note: VSHP must be set to '0' if page0 Reg0x83 COMB = 0.				

0XB1 – NOVIDMODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		1
5-4	NOVIDMODE	R/W	Select NOVID_656 output mode status. When NOVID_656 is set to 1, NOVID_656 code is being output when following status is active in Video Decoding logic. 0: Video lost (vdloss). 1: No Video (novideo). 2 : Video lost or No video(vdloss or novideo) 3: NOVID_656 code is not being output at anytime.	0h
3-0	Reserved	R		Ah

AUDIO ADC DIGITAL INPUT OFFSET CONTROL

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AADC4OFS[9:8]	R/W	AIN4 Digital ADC input data offset control bit9-8.	0h
5-4	AADC3OFS[9:8]	R/W	AIN3 Digital ADC input data offset control bit9-8.	0h
3-2	AADC2OFS[9:8]	R/W	AIN2 Digital ADC input data offset control bit9-8.	0h
1-0	AADC1OFS[9:8]	R/W	AIN1 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by

ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC1OFS[7:0]	R/W	AIN1 Digital ADC input data offset control bit7-0.	0h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC2OFS[7:0]	R/W	AIN2 Digital ADC input data offset control bit7-0.	0h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC3OFS[7:0]	R/W	AIN3 Digital ADC input data offset control bit7-0.	0h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC4OFS[7:0]	R/W	AIN4 Digital ADC input data offset control bit7-0.	0h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-2	Reserved	R		0h
1-0	AADC51OFS[9:8]	R/W	AIN51 Digital ADC input data offset control bit9-8.	0h

NOTE:
DIGITAL ADC INPUT DATA OFFSET CONTROL. DIGITAL ADC INPUT DATA IS ADJUSTED BY:
ADJAADCN = AUDNADC + AADCNOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC51OFS[7:0]	R/W	AIN51 Digital ADC input data offset control bit7-0.	0h

ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-6	AUD4ADC[9:8]	R	Bit9-8 of AIN4 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD3ADC[9:8]	R	Bit9-8 of AIN3 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD2ADC[9:8]	R	Bit9-8 of AIN2 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD1ADC[9:8]	R	Bit9-8 of AIN1 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD1ADC[7:0]	R	Bit7-0 of AIN1 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD2ADC[7:0]	R	Bit7-0 of AIN2 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD3ADC[7:0]	R	Bit7-0 of AIN3 Analog Audio ADC Digital Output Value by 2's format..	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD4ADC[7:0]	R	Bit7-0 of AIN4 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-2	Reserved		Reserved	00h
1-0	AUD51ADC[9:8]	R	Bit9-8 of AIN51 Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD51ADC[7:0]	R	Bit7-0 of AIN51 Analog Audio ADC Digital Output Value by 2's format.	X

ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

0XBD – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-6	ADJAADC4[9:8]	R	Bit9-8 of AIN4 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC3[9:8]	R	Bit9-8 of AIN3 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC2[9:8]	R	Bit9-8 of AIN2 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC1[9:8]	R	Bit9-8 of AIN1 adjusted Audio ADC Digital Input Data Value by 2's format.	X
The value shows the first input data in front of Digital Audio Decimation Filtering process.				

0XBE – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC1[7:0]	R	Bit7-0 of AIN1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBF – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC2[7:0]	R	Bit7-0 of AIN2 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC3[7:0]	R	Bit7-0 of AIN3 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC4[7:0]	R	Bit7-0 of AIN4 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-2			Reserved	00h
1-0	ADJAADC51[9:8]	R	Bit9-8 of AIN51 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC51[7:0]	R	Bit7-0 of AIN51 adjusted Audio ADC Digital Input Data Value by 2's format.	X

MPP PIN OUTPUT MODE CONTROL

0XC8 – MPP PIN OUTPUT MODE CONTROL

Bit	Function	R/W	Description	Reset
7	GPP_VAL2	R/W	Select the general purpose value through the MPP2 pin. 0 : “0” value, 1: “1” value	0h
6-4	MPP_MODE2	R/W	Select the output mode for MPP2 pin. Followings show the status when POLMPP2 register is set to 0. If POLMPP2 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1 (Odd), High is field2 (Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL2 register value. If VDLOSSOE register is set to “1”, vdloss2 signal is output to MPP2 pin and these MPP_MODE2 function is not effective.	0h
3	GPP_VAL1	R/W	Select the general purpose value through the MPP1 pin. 0 : “0” value, 1: “1” value	0h
2-0	MPP_MODE1	R/W	Select the output mode for MPP1 pin. Followings show the status when POLMPP1 register is set to 0. If each POLMPP1 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1 (Odd), High is field2 (Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL1 registers value. If VDLOSSOE register is set to “1”, vdloss1 signal is output to MPP1 pin and these MPP_MODE1 function is not effective.	0h

0XC9 – MPP PIN OUTPUT MODE CONTROL

Bit	Function	R/W	Description	Reset
7	GPP_VAL4	R/W	Select the general purpose value through the MPP4 pin. 0 : “0” value, 1: “1” value	0h
6-4	MPP_MODE4	R/W	Select the output mode for MPP4 pin. Followings show the status when POLMPP4 register is set to 0. If POLMPP4 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1 (Odd), High is field2 (Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL4 register value. If VDLOSSOE register is set to “1”, vdloss4 signal is output to MPP4 pin and these MPP_MODE4 function is not effective.	0h
3	GPP_VAL3	R/W	Select the general purpose value through the MPP3 pin. 0 : “0” value, 1: “1” value	0h
2-0	MPP_MODE3	R/W	Select the output mode for MPP3 pin. Followings show the status when POLMPP3 register is set to 0. If each POLMPP3 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1 (Odd), High is field2 (Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL3 register value. If VDLOSSOE register is set to “1”, vdloss3 signal is output to MPP3 pin and these MPP_MODE3 function is not effective.	0h

0XCB – POLMPP1/2/3/4

Bit	Function	R/W	Description	Reset
7	POLMPP4	R/W	Select MPP4 pin output polarity. 0: normal, 1: inverse polarity.	0
6	POLMPP3	R/W	Select MPP3 pin output polarity. 0: normal, 1: inverse polarity.	0
5	POLMPP2	R/W	Select MPP2 pin output polarity. 0: normal, 1: inverse polarity.	0
4	POLMPP1	R/W	Select MPP1 pin output polarity. 0: normal, 1: inverse polarity.	0
3-0	Reserved	R		0

0XCE – ANALOG POWER DOWN CONTROL

Bit	Function	R/W	Description	Reset
7	AAUTOMUTE	R/W	1: When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200. 0: No effect	0
6	Reserved	R	Reserved	0
5	A_DAC_PWDN	R/W	Power down the audio DAC. 0: Normal operation 1: Power down	0
4	A_ADC_PWDN	R/W	Power down the audio ADC. 0: Normal operation 1: Power down	0

3-0	V_ADC_PWDN [4:1]	R/W	Power down the video ADC. V_ADC_PWDN[4:1] stands for VIN4 to VIN1. 0: Normal operation 1: Power down	0h

0XCF – SERIAL MODE CONTROL

Bit	Function	R/W	Description	Reset
7-6	SMD	R/W	Set up cascade Audio Serial mode. When SMD=2hex or 3hex, ALINKO pin output cascaded audio serial data. When SMD=0hex, ALINKO pin output is tri-state. 00: No Serial mode. ALINKO pin is tri-state output. 10: ALINKO pin is Serial out pin. ALINKI pin is Serial input pin.	0h
5-0	Reserved	R		0

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

Index	Bit	Function	R/W	Description	Reset
0xD0	7-4	AIGAIN2	R/W	Select the amplifier's gain for each analog audio input AIN1/2/3/4/51. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75	8h
0xD1		AIGAIN4	R/W		

Index	Bit	Function	R/W	Description	Reset
0x7F		AIGAIN51	R/W	7 0.88 8 1.00 (default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	
0xD0	3-0	AIGAIN1	R/W		8h
0xD1		AIGAIN3	R/W		
0x7F		MIXRATIO51	R/W	Audio input AIN51 ratio value for audio mixing	0h

0XD2 – NUMBER OF AUDIO TO BE RECORDED

Bit	Function	R/W	Description	Reset
7	M_RLSWAP	R/W	Define the sequence of mixing and playback audio data on the ADATM pin. If RM_SYNC=0 : I2S format, 0:Mixing audio on position 0 and playback audio on position 8 1:Playback audio on position 0 and mixing audio on position 8 If RM_SYNC=1 : DSP format, 0:Mixing audio on position 0 and playback audio on position 1 1:Playback audio on position 0 and mixing audio on position 1	0
6	RM_SYNC	R/W	Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin. 0 : I2S format 1 : DSP format	0
5-4	RM_PBSEL	R/W	Select the output PlayBackIn data for the ADATM pin. 0 : First Stage PlayBackIn audio PB1 1 : Reserved 2 : Last Stage PlayBackIn audio PB3 3 : Reserved	0h
3-2	R_ADATM	R/W	Select the output mode for the ADATM pin. 0:Digital serial data of mixing audio 1:Digital serial data of ADATR format record audio 2:Digital serial data of ADATM format record audio	0h
1-0	R_MULTCH	R/W	Define the number of audio for record on the ADATR pin. 0 : 2 audios 1 : 4 audios 2 : 8 audios 3 : 16 audios Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. Also, each output position data are selected by R_SEQ_0/R_SEQ_1/…/R_SEQ_F registers.	0h

0XD3, 0XD4, 0XD5, 0XD6, 0XD7, 0XD8, 0XD9, 0XDA – SEQUENCE OF AUDIO TO BE RECORDED

Index	Bit	Function	R/W	Description	Reset
0xD3	7-4	R_SEQ1	R/W	Define the sequence of record audio on the ADATR pin. Refer to the Fig29 and Table7 for the detail of the R_SEQ_0 ~ R_SEQ_F. The default value of R_SEQ_0 is “0”, R_SEQ_1 is “1”, and R_SEQ_F is “F”. 0 AIN1 1 AIN2 2 AIN3 : : : : 14 AIN15 15 AIN16	1h
	3-0	R_SEQ0	R/W		0h
0xD4	7-4	R_SEQ3	R/W		3h
	3-0	R_SEQ2	R/W		2h
0xD5	7-4	R_SEQ5	R/W		5h
	3-0	R_SEQ4	R/W		4h
0xD6	7-4	R_SEQ7	R/W		7h
	3-0	R_SEQ6	R/W		6h
0xD7	7-4	R_SEQ9	R/W		9h
	3-0	R_SEQ8	R/W		8h
0xD8	7-4	R_SEQB	R/W		Bh
	3-0	R_SEQA	R/W		Ah
0xD9	7-4	R_SEQD	R/W		Dh
	3-0	R_SEQC	R/W		Ch
0xDA	7-4	R_SEQF	R/W		Fh
	3-0	R_SEQE	R/W		Eh

0XDB –MASTER CONTROL

Bit	Function	R/W	Description	Reset
7	ADACEN	R/W	Audio DAC Function mode 0:Audio DAC function disable(test purpose only) 1:Audio DAC function enable	1
6	AADCEN	R/W	Audio ADC Function mode 0:Audio ADC function disable(test purpose only) 1:Audio ADC function enable	1
5	PB_MASTER	R/W	Define the operation mode of the ACLKP and ASYNP pin for playback. 0:All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1:TW2868 type I2S/DSP Master mode (ACLKP and ASYNP is output)	0
4	PB_LRSEL	R/W	Select audio data to be used for playback input. If PB_SYNC=0 I2S format, 0: 1st Left channel audio data(default), 1: 1st Right channel audio data. If PB_SYNC=1 DSP format, 0: 1st input audio data. 1: 2nd input audio data	0
3	PB_SYNC	R/W	Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin. 0:I2S format 1:DSP format	0
2	RM_8BIT	R/W	Define output data format per one word unit on ADATR pin. 0:16bit one word unit output 1:8bit one word unit packed output	0
1	ASYNROEN	R/W	Define input/output mode on the ASYNR pin. 1:ASYNR pin is input 0:ASYNR pin is output	1

0	ACLKRMASTER	R/W	Define input/output mode on the ACLKR pin and set up audio system processing. 0: ACLKR pin is input. External 256xfs or 320fs or 384xfs clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1: ACLKR pin is output. Internal ACKG generates audio system clock.	0

U-LAW/A-LAW OUTPUT AND MIX MUTE CONTROL

0XDC –U-LAW/A-LAW OUTPUT AND MIX MUTE CONTROL

Bit	Function	R/W	Description	Reset
7-6	LAWMD	R/W	Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin. 0:PCM output 1:SB(Signed MSB bit in PCM data is inverted) output 2:u-Law output 3:A-Law output	0
5	MIX_DERATIO	R/W	Disable the mixing ratio value for all audio. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly	0
4-0	MIX_MUTE	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0]: Audio input AIN1. MIX_MUTE[1]: Audio input AIN2. MIX_MUTE[2]: Audio input AIN3. MIX_MUTE[3]: Audio input AIN4. MIX_MUTE[4]: Playback audio input. 0: Normal 1: Muted.	00h

0X7E – MIX_MUTE_A51

Bit	Function	R/W	Description	Reset
7	AIN51OUTOFF	R/W	AIN51/52/53/54 data output control on ADATR record signal. 0: output AIN51/AIN52/AIN53/AIN54 record data on ADATR. 1: not output AIN51/AIN52/AIN53/AIN54 record data on ADATR.	1
6	ADATM_I2SOEN	R/W	Define ADATM pin output 2 word data to make standard I2S output. 0:Mixing Data or Playback Input data are only output on ADATM pin by M_RLSWAP register.(default) 1:L/R data on ADATM pin is selected by I2SO_RSEL / I2SO_LSEL registers.	0
5	MIX_MUTE_A51	R/W	MIX_MUTE_A51: Audio input AIN51 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH51[4:0]	R/W	AIN51 threshold value for audio detection	03h

0X72 – MIX RATIO VALUE

Bit	Function	R/W	Description	Reset
7	MRATIOMD	R/W	Audio Mixing ratio value divider control 0: MIX_RATIOn 0 0.25 (default) 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: MIX_RATIO / 64	0
6	ADACTEST	R/W	0: must be set up 0 in normal mode. 1: test purpose only	0
5	AOFFCORE	R/W	0: Audio No-input Noise reduction on (default) 1: Audio No-input Noise reduction off **This bit must be set to a 1 ("No-input Noise reduction off") when the TW2868 is initialized. If this bit stays at its default setting (0), the TW2868 may generate unwanted noise.**	0
4	DAORATIO	R/W	Digital Audio Output Gain is controlled by following. 0: DAOGAIN 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00(default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: DAOGAIN / 64	0

3-0	DAOGAIN	R/W	Digital Audio Output Gain. Gain is controlled with DAORATIO mode.	8h

0XDD – MIX RATIO VALUE

Bit	Function	R/W	Description	Reset
7-4	MIX_RATIO2	R/W	Audio input AIN2 ratio value for audio mixing	0
3-0	MIX_RATIO1	R/W	Audio input AIN1 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

Bit	Function	R/W	Description	Reset
7-4	MIX_RATIO4	R/W	Audio input AIN4 ratio value for audio mixing	0
3-0	MIX_RATIO3	R/W	Audio input AIN3 ratio value for audio mixing	0

0XDF – ANALOG AUDIO OUTPUT GAIN

Bit	Function	R/W	Description	Reset
7-4	AOGAIN	R/W	Define the amplifier gain for analog audio output. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 (default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	8h
3-0	MIX_RATIOP	R/W	Playback audio input ratio value for audio mixing.	0

0XE0 – MIX OUTPUT SELECTION

Bit	Function	R/W	Description	Reset
7	VADCCKPOL	R/W	Test purpose only.	0
6	AADCCKPOL	R/W	1: Analog Audio ADC input clock polarity inverse 0: not inverse.	0
5	ADACCKPOL	R/W	Test purpose only.	0
4-0	MIX_OUTSEL	R/W	Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10(Ah) Select record audio of channel 11 11(Bh) Select record audio of channel 12 12(Ch) Select record audio of channel 13 13(Dh) Select record audio of channel 14 14(Eh) Select record audio of channel 15 15(Fh) Select record audio of channel 16 16(10h) Select playback audio of the first stage chip PB1 17(11h) Reserved 18(12h) Select playback audio of the last stage chip PB3 19(13h) Reserved 20(14h) Select mixed audio 21(15h) Select record audio of channel AIN51 22(16h) Select record audio of channel AIN52 23(17h) Select record audio of channel AIN53 24(18h) Select record audio of channel AIN54 Others no sound.	1Fh

AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

0XE1 – AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7	AAMPMD	R/W	Define the audio detection method. 0: Detect audio if absolute amplitude is greater than threshold(Test purpose only) 1: Detect audio if differential amplitude is greater than threshold(recommended)	1
6-4	ADET_FILT	R/W	Select the filter for audio detection 0: Wide LPF . . . . 7: Narrow LPF	7
3	ADET_TH4[4]*	R/W	MSB bit of AIN4 threshold value for audio detection.	0
2	ADET_TH3[4]*	R/W	MSB bit of AIN3 threshold value for audio detection.	0
1	ADET_TH2[4]*	R/W	MSB bit of AIN2 threshold value for audio detection.	0
0	ADET_TH1[4]*	R/W	MSB bit of AIN1 threshold value for audio detection.	0

NOTE: *

ADET_TH :Define the threshold value for audio detection.

ADET_TH1: Audio input AIN1.

ADET_TH2: Audio input AIN2.

ADET_TH3: Audio input AIN3.

ADET_TH4: Audio input AIN4.
ADET_TH51: Audio input AIN51.

0:Low value (default)

. .

. .

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7-4	ADET_TH2[3:0]	R/W	Bit3-0 of AIN2 threshold value for audio detection.	3h
3-0	ADET_TH1[3:0]	R/W	Bit3-0 of AIN1 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7-4	ADET_TH4[3:0]	R/W	Bit3-0 of AIN4 threshold value for audio detection.	3h
3-0	ADET_TH3[3:0]	R/W	Bit3-0 of AIN3 threshold value for audio detection.	3h

AUDIO CLOCK INCREMENT

0XF0 – AUDIO CLOCK INCREMENT

Bit	Function	R/W	Description	Reset
7-0	ACKI[7:0]	R/W	ACKI[7:0], these bits control ACKI Clock Increment in ACKG block. ACKI[21:0]: 09B583h for fs = 8kHz is default.	83h

0XF1 – AUDIO CLOCK INCREMENT

Bit	Function	R/W	Description	Reset
7-0	ACKI[15:8]	R/W	ACKI[15:8], these bits control ACKI Clock Increment in ACKG block.	B5h

0XF2 – AUDIO CLOCK INCREMENT

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0h
5-0	ACKI[21:16]	R/W	ACKI[21:16], these bits control ACKI Clock Increment in ACKG block.	09h

AUDIO CLOCK NUMBER

0XF3 – AUDIO CLOCK NUMBER

Bit	Function	R/W	Description	Reset
7-0	ACKN[7:0]	R/W	ACKN[7:0], these bits control ACKN Clock Number in ACKG block. ACKN[17:0]: 000100h for Playback Slave-in lock is default.	00h

0XF4 – AUDIO CLOCK NUMBER

Bit	Function	R/W	Description	Reset
7-0	ACKN[15:8]	R/W	ACKN[15:8], these bits control ACKN Clock Number in ACKG block.	01h

0XF5 – AUDIO CLOCK NUMBER

Bit	Function	R/W	Description	Reset
7-2	Reserved	R		00h
1-0	ACKN[17:16]	R/W	ACKN[17:16], these bits control ACKN Clock Number in ACKG block.	0h

0XF6 – SERIAL CLOCK DIVIDER

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5-0	SDIV	R/W	These bits control SDIV Serial Clock Divider in ACKG block.	00h

0XF7 – LEFT/RIGHT CLOCK DIVIDER

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5-0	LRDIV	R/W	Reserved.	20h

0XF8 – AUDIO CLOCK CONTROL

Bit	Function	R/W	Description	Reset
7	APZ	R/W	These bits control Loop in ACKG block.	1
6-4	APG	R/W	These bits control Loop in ACKG block.	4h
3	Reserved	R		0
2	ACPL	R/W	These bits control Loop closed/open in ACKG block. 0: Loop closed(Test purpose only) 1 :Loop open(for normal mode)	1
1	SRPH	R/W	Reserved.This function is not used in TW2868 chip.	0
0	LRPH	R/W	Reserved. This function is not used in T2868 chip.	0

0XF9 – VIDEO MISCELLANEOUS FUNCTION CONTROL

Bit	Function	R/W	Description	Reset
7	LIM16	R/W	0: Output ranges are limited to 2~254 1: Output ranges are limited to 16~235 for Y and 16~239 for CbCr	0
6	PBREFEN	R/W	Audio ACKG Reference(refin) input select 0: ACKG has video VRST refin input selected by VRSTSEL register 1: ACKG has audio ASYNP refin input	1
5	YCBCR422	R/W	Control YCbCr 4:2:2 output mode 0: Normal 4:2:2 output mode 1: Averaging 4:2:2 output mode	0
4	HA656MD	R/W	Control HACTIVE signal output on H-Down Scaling output mode. 0: HACTIVE signal is always HACTIVE register's length. 1: HACTIVE signal is same as DVALID signal in H-Down Scaled video output.	1
3	VBI_FRAM	R/W	Test purpose only.	0
2	CNTL656	R/W	Select invalid data value. 0: 0x80 and 0x10 code will be output as invalid data during active video line. 1: 0x00 code will be output as invalid data during active video line.	0
1	VSCL_SYNC	R/W	Enable the optional ITU-R.656 sync code format. 0: Skip ITU-R BT.656 sync code for non-valid vertical line. 1: Standard ITU-R BT.656 sync code on any vertical line.	0
0	HA_EN	R/W	Control HACTIVE output during vertical blanking period. 0: HACTIVE output is disabled during vertical blanking	1

Bit	Function	R/W	Description	Reset
			period. 1: HACTIVE output is enabled during vertical blanking period.	

0XFA – OUTPUT ENABLE CONTROL AND CLOCK OUTPUT CONTROL

Bit	Function	R/W	Description	Reset
7	VSCL_ENA	R/W	Enable the vertical scaler for 4x CIF time-multiplexed format with 54MHz. 0: Full size for vertical direction 1: Half size for vertical direction	0
6	OE	R/W	Control the tri-state of output pin 0: Outputs are Tri-state except clock output (CLKPO, CLKNO) pin 1: Outputs are enabled	0
5	CLKNO_OEB	R/W	Control the tri-state of CLKNO pin 0: Output is enabled (default) 1: Output is Tri-state	0
4	CLKPO_OEB	R/W	Control the tri-state of CLKPO pin 0: Output is enabled 1: Output is Tri-state	0
3-2	CLKNO_MD	R/W	Control the clock frequency of CLKNO pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value	0h
1-0	CLKPO_MD	R/W	Control the clock frequency of CLKPO pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value	0h

0XFB – CLOCK POLARITY CONTROL

Bit	Function	R/W	Description	Reset
7	CLKNO_POL	R/W	Polarity inverse control on output CLKNO signal just before CLKNO pin. 0: Not inversed. 1: Polarity inverse.	0
6	CLKPO_POL	R/W	Polarity inverse control on output CLKPO signal just before CLKPO pin. 0: Not inversed. 1: Polarity inverse.	0
5	IRQENA	R/W	Enable/Disable the interrupt request through the IRQ pin. 0: Disable 1: Enable	0
4	IRQPOL	R/W	Select the polarity of interrupt request through the IRQ pin. 0: Falling edge requests the interrupt and keeps its state until cleared 1: Rising edge requests the interrupt and keeps its state until cleared	0
3-2	ADET_MODE	R/W	Define the polarity of state register and interrupt request for audio detection. 0: No interrupt request by the audio detection 1: Make the interrupt request rising only when the audio signal comes in 2: Make the interrupt request falling only when the audio signal goes out 3: Make the interrupt request rising and falling when the audio comes in and goes out	3
1-0	VDET_MODE	R/W	Define the polarity of state register and interrupt request for video detection. 0: No interrupt request by the video detection 1: Make the interrupt request rising only when the video signal comes in 2: Make the interrupt request falling only when the video signal goes out 3: Make the interrupt request rising and falling when the video comes in and goes out	3

ENABLE VIDEO AND AUDIO DETECTION

0XFC – ENABLE VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-0	AVDET1_ENA	R/W	Enable state register updating and interrupt request of video and audio detection for each input. [0]: Video input VIN1. [1]: Video input VIN2. [2]: Video input VIN3. [3]: Video input VIN4. [4]: Audio input AIN1. [5]: Audio input AIN2. [6]: Audio input AIN3. [7]: Audio input AIN4. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	FFh

0X73 – ENABLE VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-3	Reserved	R	Reserved	00h
2	AIN51FORM	R/W	AIN51/52/53/54 record output format selection. This bit is only effective when A51OUTOFF register is set to 0. When AIN1/2/3/4/51 and AIN6/7/8/9/52 are required to be continuous order in record output, 1 is necessary. 0: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat4><dat5> <dat6><dat7><dat51>< dat52> R dat : <dat8><dat9><datA><datB><datC><datD> <datE><datF><dat53><dat54> If DSP mode(RM_SYNC=1) all data are continuous. <dat0><dat1><dat2><dat3><dat4><dat5><dat6> <dat7><dat8><dat9><datA><datB><datC><datD> <datE><datF><dat51><dat52><dat53><dat54> 1: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat51><dat4> <dat5><dat6><dat7><dat52> R dat : <dat8><dat9><datA><datB><dat53><datC> <datD>< datE>< datF><dat54> If DSP mode(RM_SYNC=1) all data continuous. <dat0><dat1><dat2><dat3>< dat51><dat4><dat5> <dat6><dat7><dat52><dat8><dat9><datA><datB> <dat53><datC><datD><datE><datF><dat54>	0
1	AINTPOFF	R/W	0:must be set up 1:test purpose only	0
0	A51DET_ENA	R/W	Enable state register updating and interrupt request of audio AIN51 detection for each input. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	1

STATUS OF VIDEO AND AUDIO DETECTION

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-0	AVDET1_STATE	R/W	State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE. [0]: Video input VIN1. [1]: Video input VIN2. [2]: Video input VIN3. [3]: Video input VIN4. [4]: Audio input AIN1. [5]: Audio input AIN2. [6]: Audio input AIN3. [7]: Audio input AIN4. 0 Inactivated 1 Activated	00h

0X74 – STATUS OF VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-1	Reserved	R		00h
0	A51DET_STATE	R/W	State of Audio AIN51 detection. This bit is activated according ADET_MODE. 0 Inactivated 1 Activated	0

DEVICE ID AND REVISION ID FLAG

0XFE – DEVICE ID AND REVISION ID FLAG

Bit	Function	R/W	Description	Reset
7-6	DEV_ID[6:5]	R	Bit6-5 of Device ID. Together with 0xFF[7:3] indicate TW2868 product ID code. DEV_ID=7'h1B	0
5-3	Reserved	R		0
2-0	TEST	R/W	Test purpose only. This must be 0 in normal mode.	0

0XFF – DEVICE ID AND REVISION ID FLAG

Bit	Function	R/W	Description	Reset
7-3	DEV_ID[4:0]	R	Bit4-0 of Device ID.	1Bh
2:0	REV_ID	R	The revision number. REV_ID=3'h0 1st TW2868 chip.	0h

0X60 – CLOCK PLL CONTROL

Bit	Function	R/W	Description	Reset
7	PLLCKOUT	R/W	0: must be set up in normal mode. 1: MPP1 pin output 108MHz Clock - in phase in Clock PLL MPP2 pin output 108MHz Clock - 90 degree phase shift in Clock PLL MPP3 pin output 108MHz Clock - 180 degree phase shift in Clock PLL MPP4 pin output 108MHz Clock – 270 degree phase shift in Clock PLL	0
6	PLL_PD	R/W	Clock PLL Power down control. 0: Clock PLL normal mode. 1: Clock PLL power down mode. (Recommended when 108MHz CLKPO/CLKNO output is not used with XTI=54MHz input, or when XTI=108MHz input is used.)	0
5	PLL_IREF	R/W	Clock PLL Current bias reference. 0: reference 0. 1: reference 1.	0
4	SEL_X24	R/W	Clock PLL output mode 0: 2x XTI input frequency.54MHz clock input mode. 1: 4x XTI input frequency.27MHz clock input mode.	0
3-2	LP_X4	R/W	Loop resistor for PLL. 0: 80.5kOhm. 1: 35.5kOhm. 2: 25.5kOhm. 3: 20.5kOhm.	1h
1-0	CP_X4	R/W	Charge-pump current for PLL. 0: 1uA. 1: 5uA. 2: 10uA. 3: 15uA.	1h

0X61 – 108MHZ CLOCK SELECT

Bit	Function	R/W	Description	Reset
7-5	Reserved	R	Reserved	0h
4	DECOSC	R/W	Video Decoder/Digital Audio system clock select. This bit is effective when Clock PLL is enable (PLL_PD=0). 0: Clock PLL output 108MHz/4 clock is selected when PLL_PD=0. If PLL_PD=1, this bit should be 0 for default function. 1: system clock generated by XTI input crystal clock when Clock PLL is enable (PLL_PD=0). If 108MHz is connected, system clock is XTI / 4 If 54MHz is connected, system clock is XTI / 2. If 27MHz is connected, system clock is XTI.	1
3-2	CKOUTSEL	R/W	Clock PLL output 108MHz select. 0: 108MHz Clock output - in phase. 1: 108MHz Clock output - 90 degree phase shift. 2: 108MHz Clock output - 180 degree phase shift. 3: 108MHz Clock output – 270 degree phase shift.	0h
1-0	XTIMD	R/W	XTI pin input clock process control. If XTIMD=0/1/2, Clock PLL Output clock is not used for internal logic process. 0: 27MHz XTI input clock is used for all clock sources. (test purpose only) 1: 54MHz XTI input clock is used for all clock sources. 2: 108MHz XTI input clock is used for all clock sources. 3: Clock PLL 108MHz output is used for all system clock source.	3h

0X65 – VIDEO BUS TRI-STATE CONTROL

Bit	Function	R/W	Description	Reset
7-4	Reserved	R		0h
3	VD4OEB	R/W	VD4[7:0] output tri-state control. 1: tri-state output VD4[7:0]. 0: normal output VD4[7:0].	0
2	VD3OEB	R/W	VD3[7:0] output tri-state control. 1: tri-state output VD3[7:0]. 0: normal output VD3[7:0].	0
1	VD2OEB	R/W	VD2[7:0] output tri-state control. 1: tri-state output VD2[7:0]. 0: normal output VD2[7:0].	0
0	VD1OEB	R/W	VD1[7:0] output tri-state control. 1: tri-state output VD1[7:0]. 0: normal output VD1[7:0].	0

0X66 – OPTIONAL CLOCK OUTPUT

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5	VDN_27C	R/W	0: normal 27MHz output if CLKNO_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKNO pin.	0
4	VDP_27C	R/W	0: normal 27MHz output if CLKPO_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKPO pin.	0
3-2	Reserved	R		0
1	CKN_13	R/W	0: normal clock output on CLKNO pin by CLKNO_MD. 1: Optional 13.5MHz clock output on CLKNO pin.	0

Bit	Function	R/W	Description	Reset
0	CKP_13	R/W	0: normal clock output on CLKPO pin by CLKPO_MD. 1: Optional 13.5MHz clock output on CLKPO pin.	0

0X70 – AUDIO CLOCK CONTROL

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6	S2I_8BIT	R/W	0: ACLKP/ASYNP/ADATP pin input is 16bit control. 1: ACLKP/ASYNP/ADATP pin input is 8bit control.	0
5	ACLKRPOL	R/W	ACLKR input signal polarity inverse. 0: not inverse. 1: inverse.	0
4	ACLKPPOL	R/W	ACLKP input signal polarity inverse. 0: not inverse. 1: inverse.	0
3	AFAUTO	R/W	ACKI[21:0] control automatic set up with AFMD registers. This mode is only effective when ACLKRMASTER=1. 0: ACKI[21:0] registers set up ACKI control. 1: ACKI control is automatically set up by AFMD register values.	1
2-0	AFMD	R/W	AFAUTO control mode. 0: 8kHz setting (default). 1: 16kHz setting. 2: 32kHz setting. 3: 44.1kHz setting. 4: 48kHz setting.	0h

0X71 – DIGITAL AUDIO INPUT CONTROL

Bit	Function	R/W	Description	Reset
7	I2S8MODE	R/W	8bit I2S Record output mode. 0: L/R half length separated output. 1: One continuous packed output equal to DSP output format.	0
6	MASCKMD	R/W	Audio Clock Master ACLKR output wave format. 0: High period is one 27MHz clock period. 1: Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up ACKI registers. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1. SDIV=00h is used with this function normally.	1
5	PBINSWAP	R/W	Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping. 0: Not swapping. 1: Swapping.	0
4	ASYNRDLY	R/W	ASYNR input signal delay. 0: No delay. 1: Add one 27MHz period delay in ASYNR signal input.	0
3	ASYNPDLY	R/W	ASYNP input signal delay. 0: No delay. 1: Add one 27MHz period delay in ASYNP signal input.	0
2	ADATPDLY	R/W	ADATP input data delay by one ACLKP clock. 0: No delay. This is for I2S type 1T delay input interface. 1: Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.	0
1-0	INLAWMD	R/W	Select u-Law/A-Law/PCM/SB data input format on ADATP pin. 0:PCM input 1:SB(Signed MSB bit in PCM data is inverted) input 2:u-Law input	0h

Bit	Function	R/W	Description	Reset
			3:A-Law input	

ADATM I2S OUTPUT SELECT

0X7B – ADATM I2S OUTPUT SELECT

Bit	Function	R/W	Description	Reset
7-5	Reserved	R		0h
4-0	I2SO_RSEL	R/W	Select R-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

*Note :
Both I2SO_RSEL and I2SO_LSEL select output data by following order.

0	Select record audio of channel 1(AIN1)
1	Select record audio of channel 2(AIN2)
2	Select record audio of channel 3(AIN3)
3	Select record audio of channel 4(AIN4)
4	Select record audio of channel 5(AIN5)
5	Select record audio of channel 6(AIN6)
6	Select record audio of channel 7(AIN7)
7	Select record audio of channel 8(AIN8)
8	Select record audio of channel 9(AIN9)
9	Select record audio of channel 10(AIN10)
10(Ah)	Select record audio of channel 11(AIN11)
11(Bh)	Select record audio of channel 12(AIN12)
12(Ch)	Select record audio of channel 13(AIN13)
13(Dh)	Select record audio of channel 14(AIN14)
14(Eh)	Select record audio of channel 15(AIN15)
15(Fh)	Select record audio of channel 16(AIN16)
16(10h)	Select playback audio of the first stage chip(PB1)
17(11h)	Reserved
18(12h)	Select playback audio of the last stage chip(PB3)
19(13h)	Reserved
20(14h)	Select mixed audio.
21(15h)	Select record audio of channel 51(AIN51)(default)
22(16h)	Select record audio of channel 52(AIN52)
23(17h)	Select record audio of channel 53(AIN53)
24(18h)	Select record audio of channel 54(AIN54)
Others	no audio output.

0X7C – ADATM I2S OUTPUT SELECT

Bit	Function	R/W	Description	Reset
7-5	Reserved	R		0h
4-0	I2SO_LSEL	R/W	Select L-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h
* Note: Please read 0x7B Note for detail description.				

AIN51/52/53/54 RECORD OUTPUT

0X7D – AIN51/52/53/54 RECORD OUTPUT

Bit	Function	R/W	Description	Reset
7-6	I2SRECSEL54	R/W	Select output data in bellow dat54 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	3h
5-4	I2SRECSEL53	R/W	Select output data in bellow dat53 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	2h
3-2	I2SRECSEL52	R/W	Select output data in bellow dat52 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	1h
1-0	I2SRECSEL51	R/W	Select output data in bellow dat51 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	0

These registers are only effective when A51OUTOFF=0.These registers function change under AIN51FORM control at that time as follows.

When AIN51FORM=0:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat51><dat52>

R data : <dat8><dat9><datA><datB><datC><datD><datE><datF><dat53><dat54>

If DSP mode(RM_SYNC=1),all data are continuous.

<dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat8><dat9><datA><datB><datC>

<datD><datE><datF><dat51><dat52><dat53><dat54>

When AIN51FORM=1:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52>

R data : <dat8><dat9><datA><datB><dat53><datC><datD><datE><datF><dat54>

Bit	Function	R/W	Description	Reset
			If DSP mode(RM_SYNC=1),all data are continuous. <dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52><dat8><dat9> <datA><datB><dat53><datC><datD><datE><datF><dat54> All other datN(N=0,1,2,,,,F) are selected by R_SEQ_N registers	

0X89 – AUDIO FS MODE CONTROL

Bit	Function	R/W	Description	Reset
7	ATHROUGH	R/W	0: must be set up in normal mode. 1: test purpose only.	0
6	ASYNSERIAL	R/W	0: must be set up in normal mode. 1: test purpose only.	0
5	ACLKR128	R/W	ACLKR clock output mode for special 16x8bit(total 128bit) data interface. 0: ACLKR output is normal. 1: the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8bit mode (special purpose).	0
4	ACLKR64	R/W	ACLKR clock output mode for special 4 word output interface. ACLKRMASTER=1 mode only. 0: ACLKR output is normal 1: the number of ACLKR clock per fs is 64.	0
3	AFS384	R/W	Special Audio fs Sampling mode. 0: Audio fs Sampling mode is normal 256xfs if AIN51MD=0. 1: Audio fs Sampling mode is 384xfs mode.	0
2	AIN5MD	R/W	Audio Input process mode. 0: AIN1/AIN2/AIN3/AIN4/AIN5/AIN6/AIN7/AIN8 8 Audio input only process. This mode is 256xfs if AFS384=0.In this mode, AIN51/AIN52 input is not processed. 1: AIN1/AIN2/AIN3/AIN4/AIN51/AIN5/AIN6/AIN7/AIN8/ AIN52 10 Audio input process. This mode is 320xfs mode if AFS384=0.	0
1-0	Reserved	R		1h

0XB2 – VDLOSS OUTPUT

Bit	Function	R/W	Description	Reset
7-1	Reserved	R		00h
0	VDLOSSOE	R/W	**Video Decoder VDLOSS1/VDLOSS2/VDLOSS3/VDLOSS4/VDLOSS5/VDLOSS6/ VDLOSS7/VDLOSS8 signals output MPP1/ MPP2/ MMP3/ MPP4/MPP5/MPP6/MPP7/MPP8 pins.** 0: not output VDLOSS1/VDLOSS2/VDLOSS3/VDLOSS4/ VDLOSS5/VDLOSS6/VDLOSS7/VDLOSS8 on MPP1/ MPP2/MPP3/MPP4/MPP5/MPP6/MPP7/MPP8pins. 1: VIN1 Video Decoder VDLOSS1 output on MPP1 pin. VIN2 Video Decoder VDLOSS2 output on MPP2 pin. VIN3 Video Decoder VDLOSS3 output on MPP3 pin. VIN4 Video Decoder VDLOSS4 output on MPP4 pin. VIN5 Video Decoder VDLOSS5 output on MPP5 pin. VIN6 Video Decoder VDLOSS6 output on MPP6 pin. VIN7 Video Decoder VDLOSS7 output on MPP7 pin. VIN8 Video Decoder VDLOSS8 output on MPP8 pin.	0

0X50 – AUDIO DAC GAIN CONTROL

Bit	Function	R/W	Description	Reset
7	ADACCLK_INV	R/W	Clock inversion control in Audio DAC module. 0: not inversed. 1: inversed.	0
6-4	DAC_IB_DAC	R/W	Audio DAC bias fine control 000->10uA 001->12uA 010->6uA 011->8uA 100->18uA 101->20uA 110->14uA 111->16uA Note: Idac=10uA + Idac_ib_dac + i_dac_ib_adc Default: Idac=60uA. 80uA to get full scale	0
3	Reserved	R		0
2-0	DAC_IB_ADC	R/W	Audio DAC bias coarse control 000->40uA 001->48uA 010->24uA 011->32uA 100->72uA 101->80uA 110->56uA 111->64uA Note: Idac=10uA + Idac_ib_dac + i_dac_ib_adc Default: Idac=60uA. 80uA to get full scale	0

0X51 – AUDIO DAC LOW PASS BIAS CONTROL

Bit	Function	R/W	Description	Reset
7-0	DAC_LPFBIAS	R/W	Audio DAC Reference LPF control DAC_LPFBIAS<7:5>=000 -> 2uA DAC_LPFBIAS<7:5>=001 -> 4uA DAC_LPFBIAS<7:5>=010 -> 6uA DAC_LPFBIAS<7:5>=011 -> 8uA DAC_LPFBIAS<7:5>=100 -> 10uA DAC_LPFBIAS<7:5>=101 -> 12uA DAC_LPFBIAS<7:5>=110 -> 14uA DAC_LPFBIAS<7:5>=111 -> 16uA DAC_LPFBIAS<4>=0 -> disable the on-chip reference bias DAC_LPFBIAS<4>=1 -> enable the on-chip reference bias DAC_LPFBIAS<3:0>=0000 -> 31.25nA DAC_LPFBIAS<3:0>=0001 -> 62.5nA … … DAC_LPFBIAS<3:0>=1000 -> 125nA (default) … … **DAC_LPFBIAS<3:0>=1111 -> 343.75nA**	00

0X52 – AUDIO DAC LPF AND BIAS CONTROL

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-4	LPFSEL	R/W	Audio DAC LPF corner frequency selection 000->15.6kHz 001->7.8kHz 010->Don't use 011->3.9kHz 100->Don't use 101->Don't use 110->Don't use 111->2.6Khz	0
3	BIAS_SEL	RW	Audio DAC Bias selection. 0-> AVDD33 as the reference voltage. **1-> select bandgap voltage as the reference**	0
2-0	DAC_IB_OTA	R/W	Audio DAC OTA bias control. 000->10uA 001->12uA 010->6uA 011->8uA 100->18uA 101->20uA 110->14uA **111->16uA**	0

0X53 – AUDIO DAC TEST CONTROL

Bit	Function	R/W	Description	Reset
7-4	Reserved	R	TBD	0h
3	TVSENSE	RW	AVDS Test purpose only. 0 must be set up in normal mode. 0:MPP1/2/3/4/5/6/7/8 pin are normal function output. 1:MPP1/2/3/4/5/6/7/8 pin output have followings. MPP8 : VSENSE8A MPP7 : VSENSE7A MPP6 : VSENSE6A MPP5 : VSENSE5A MPP4 : VSENSE4A MPP3 : VSENSE3A MPP2 : VSENSE2A MPP1 : VSENSE1A	0
2-0	ADACTEST	R/W	Audio DAC test control 000->normal operation 001->ibias places to the dac_out (Don't use) 010->din_0 is places to the dac_out (Don't use) 011->both ibias and din_o are placed at the dac_out (Don't use) 100->disable output driver. Dac_out floating 101-> disable output driver, ibias places to dac_out 110-> disable output driver, din_0 places to dac_out 111->don't use	0

0X54 – AIN1/2/3/4/51 AUDIO ADC CONTROL

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5	DOUT_RST1	R/W	AIN1/2/3/4/51 Audio ADC digital output reset for all channel. This bit must be set up to 0 again after 1 value is set up.	0
4	DIV_RST1	R/W	AIN1/2/3/4/51 Audio ADC divider reset. This bit must be set up to 0 again after 1 value is set up.	0
3	ACALEN1	RW	AIN1/2/3/4/51 Audio ADC Calibration control. This bit must be set up to 0 again after 1 value is set up.	0
2-0	ASAVE1	R/W	AIN1/2/3/4/51 Audio ADC power save	7

0X58 – AVDS STATUS (TEST PURPOSE ONLY)

Bit	Function	R/W	Description	Reset
7	VSENSE4B	R	VIN4B AVDS VSENSE signal.	X
6	VSENSE3B	R	VIN3B AVDS VSENSE signal.	X
5	VSENSE2B	R	VIN2B AVDS VSENSE signal.	X
4	VSENSE1B	R	VIN1B AVDS VSENSE signal.	X
3	VSENSE4A	R	VIN4A AVDS VSENSE signal.	X
2	VSENSE3A	R	VIN3A AVDS VSENSE signal.	X
1	VSENSE2A	R	VIN2A AVDS VSENSE signal.	X
0	VSENSE1A	R	VIN1A AVDS VSENSE signal.	X

0X59 – AVDS POWER CONTROL (TEST PURPOSE ONLY)

Bit	Function	R/W	Description	Reset
7	PDBV4B	R/W	0: VIN4B AVDS power down. 1: VIN4B AVDS normal operation.	0
6	PDBV3B	R/W	0: VIN3B AVDS power down. 1: VIN3B AVDS normal operation.	0
5	PDBV2B	R/W	0: VIN2B AVDS power down. 1: VIN2B AVDS normal operation.	0
4	PDBV1B	R/W	0: VIN1B AVDS power down. 1: VIN1B AVDS normal operation.	0
3	PDBV4A	R/W	0: VIN4A AVDS power down. 1: VIN4A AVDS normal operation.	0
2	PDBV3A	R/W	0: VIN3A AVDS power down. 1: VIN3A AVDS normal operation.	0
1	PDBV2A	R/W	0: VIN2A AVDS power down. 1: VIN2A AVDS normal operation.	0
0	PDBV1A	R/W	0: VIN1A AVDS power down. 1: VIN1A AVDS normal operation.	0

0X5A – VSAVE

Bit	Function	R/W	Description	Reset
7	AVDSMD	R/W	AVDS module PDB input select. (Test purpose only). 0: PDBV4B input = PDBV4B register. PDBV3B input = PDBV3B register. PDBV2B input = PDBV2B register. PDBV1B input = PDBV1B register. PDBV4A input = PDBV4A register. PDBV3A input = PDBV3A register. PDBV2A input = PDBV2A register. PDBV1A input = PDBV1A register. 1: PDBV4B input = inversed VIN4 register. PDBV3B input = inversed VIN3 register. PDBV2B input = inversed VIN2 register. PDBV1B input = inversed VIN1 register. PDBV4A input = VIN4 register. PDBV3A input = VIN3 register. PDBV2A input = VIN2 register. PDBV1A input = VIN1 register.	0
6	VREF50M_AVDS	R/W	AVDS Vref selection(Test purpose only). 0->100mV, 1->50mV	0
5-4	BIAS_AVDS	R/W	AVDS BIAS selection(Test purpose only). 00->1.0uA 01->2.0uA 10->8.0uA 11->8.0uA	0
3	PD_BIAS	R/W	Video ADC PD_BIAS.	0
2-0	VSAVE	R/W	Video ADC power save.	7

0X5B– VIDEO OUTPUT PIN DRIVE

Bit	Function	R/W	Description	Reset
7	VD4_DS	R/W	VD4[7:0] pin drive. 0: Low-drive, 1: High-drive	0
6	VD3_DS	R/W	VD3[7:0] pin drive. 0: Low-drive, 1: High-drive	0
5	VD2_DS	R/W	VD2[7:0] pin drive. 0: Low-drive, 1: High-drive	0
4	VD1_DS	R/W	VD1[7:0] pin drive. 0: Low-drive, 1: High-drive	0
3-2	Reserved	R		0
1	CLKNO_DS	R/W	CLKNO pin drive. 0: Low-drive, 1: High-drive	0
0	CLKPO_DS	R/W	CLKPO pin drive. 0: Low-drive, 1: High-drive	0

0X5C– BGCTL1

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
5	BGCTL1	R/W	0: page0 Reg96[7:0] control all VIN1/2/3/4 video. 1: page0 Reg96[7:0] control only VIN1 video. page0 Reg5D[7:0] control only VIN2 video. page0 Reg5E[7:0] control only VIN3 video. page0 Reg5F[7:0] control only VIN4 video.	0
4-0	Reserved	R		1

0X96 – MISCELLANEOUS CONTROL II (VIN1 OR ALL VIN1/2/3/4)

Bit	Function	R/W	Description	Reset
7	NKILL_1	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_1	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_1	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_1	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_1	R/W	1 = Force decoder output value determined by CCS_1. 0 = Disabled.	0
2	LCS_1	R/W	1 = Enable pre-determined output value indicated by CCS_1 when video loss is detected. 0 = Disabled.	0
1	CCS_1	R/W	When FCS_1 is set high or video loss condition is detected when LCS_1 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_1	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5D – VIN2 MISCELLANEOUS CONTROL II ON BGCTL1=1

Bit	Function	R/W	Description	Reset
7	NKILL_2	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_2	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_2	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_2	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_2	R/W	1 = Force decoder output value determined by CCS_2. 0 = Disabled.	0
2	LCS_2	R/W	1 = Enable pre-determined output value indicated by CCS_2 when video loss is detected. 0 = Disabled.	0
1	CCS_2	R/W	When FCS_2 is set high or video loss condition is detected when LCS_2 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_2	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5E – VIN3 MISCELLANEOUS CONTROL II ON BGCTL1=1

Bit	Function	R/W	Description	Reset
7	NKILL_3	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_3	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_3	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_3	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_3	R/W	1 = Force decoder output value determined by CCS_3. 0 = Disabled.	0
2	LCS_3	R/W	1 = Enable pre-determined output value indicated by CCS_3 when video loss is detected. 0 = Disabled.	0
1	CCS_3	R/W	When FCS_3 is set high or video loss condition is detected when LCS_3 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_3	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5F – VIN4 MISCELLANEOUS CONTROL II ON BGCTL1=1

Bit	Function	R/W	Description	Reset
7	NKILL_4	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_4	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_4	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_4	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_4	R/W	1 = Force decoder output value determined by CCS_4. 0 = Disabled.	0
2	LCS_4	R/W	1 = Enable pre-determined output value indicated by CCS_4 when video loss is detected. 0 = Disabled.	0
1	CCS_4	R/W	When FCS_4 is set high or video loss condition is detected when LCS_4 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_4	R/W	1 = Enable blue stretch. 0 = Disabled.	0

PAGE1 REGISTER DESCRIPTION

The following shows page1 registers. These registers can be accessed when 0x40[0] is 1.

0X00(VIN5)/0X10(VIN6)/0X20(VIN7)/0X30(VIN8) – VIDEO STATUS REGISTER

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(VIN5)/0X11(VIN6)/0X21(VIN7)/0X31(VIN8) – BRIGHTNESS CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(VIN5)/0X12(VIN6)/0X22(VIN7)/0X32(VIN8) – CONTRAST CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(VIN5)/0X13(VIN6)/0X23(VIN7)/0X33(VIN8) – SHARPNESS CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X04(VIN5)/0X14(VIN6)/0X24(VIN7)/0X34(VIN8) – CHROMA (U) GAIN REGISTER

Bit	Function	R/W	Description	Reset

7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(VIN5)/0X15(VIN6)/0X25(VIN7)/0X35(VIN8) – CHROMA (V) GAIN REGISTER

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(VIN5)/0X16(VIN6)/0X26(VIN7)/0X36(VIN8) – HUE CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(VIN5)/0X17(VIN6)/0X27(VIN7)/0X37(VIN8) – CROPPING REGISTER, HIGH

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(VIN5)/0X18(VIN6)/0X28(VIN7)/0X38(VIN8) – VERTICAL DELAY REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(VIN5)/0X19(VIN6)/0X29(VIN7)/0X39(VIN8) – VERTICAL ACTIVE REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(VIN5)/0X1A(VIN6)/0X2A(VIN7)/0X3A(VIN8) – HORIZONTAL DELAY REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0X0B(VIN5)/0X1B(VIN6)/0X2B(VIN7)/0X3B(VIN8) – HORIZONTAL ACTIVE REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C(VIN5)/0X1C(VIN6)/0X2C(VIN7)/0X3C(VIN8) – MACROVISION DETECTION

Bit	Function	R/W	Description	Reset
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(VIN5)/0X1D(VIN6)/0X2D(VIN7)/0X3D(VIN8) – CHIP STATUS II

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0

Bit	Function	R/W	Description	Reset
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(VIN5)/0X1E(VIN6)/0X2E(VIN7)/0X3E(VIN8) – STANDARD SELECTION

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(VIN5)/0X1F(VIN6)/0X2F(VIN7)/0X3F(VIN8) – STANDARD RECOGNITION

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B, D, G, H, I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0XE4(VIN1)/0XE7(VIN2)/0XEA(VIN3)/0XED(VIN4) – VERTICAL SCALING REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00

0XE5(VIN5)/0XE8(VIN6)/0XEB(VIN7)/0XEE(VIN8) – SCALING REGISTER, HIGH

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0XE6(VIN5)/0XE9(VIN6)/0XEC(VIN7)/0XEF(VIN8) – HORIZONTAL SCALING REGISTER, LOW

Bit	Function	R/W	Description	Reset
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00

0XA4(VIN5)/0XA5(VIN6)/0XA6(VIN7)/0XA7(VIN8) – ID DETECTION CONTROL

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 2A

0XC4(VIN5)/0XC5(VIN6)/0XC6(VIN7)/0XC7(VIN8) – H MONITOR

Bit	Function	R/W	Description	Reset
7-0	HFREF	R	Horizontal line frequency indicator(Test purpose only)	X

0X80 – SOFTWARE RESET CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-4	Reserved	R	Reserved	00b
3	VDEC8RST	W	A 1 written to this bit resets the Video8 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC7RST	W	A 1 written to this bit resets the Video7 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC6RST	W	A 1 written to this bit resets the Video6 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC5RST	W	A 1 written to this bit resets the Video5 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0XA8 ~0XA9 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

0XA8 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-4	HFLT6	R/W	Pre-filter selection for Video VIN5/VIN6 horizontal scaler. If each HSCALE[11:8]=1,HFLT [3:0] controls the peaking function. If each HSCALE[11:8]>1,HFLT [2:0] function is bellow.	0h
3-0	HFLT5	R/W	1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image.	0h

0XA9 – HORIZONTAL SCALER PRE-FILTER CONTROL REGISTER

Bit	Function	R/W	Description	Reset
7-4	HFLT8	R/W	Pre-filter selection for Video VIN7/VIN8 horizontal scaler. If each HSCALE[11:8]=1,HFLT [3:0] controls the peaking function. If each HSCALE[11:8]>1,HFLT [2:0] function is bellow.	0h
3-0	HFLT7	R/W	1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image.	0h

VIDEO AGC CONTROL

0XAA – VIDEO AGC CONTROL

Bit	Function	R/W	Description	Reset
7	AGCEN8	R/W	Select Video AGC loop function on VIN8 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN8	0
6	AGCEN7	R/W	Select Video AGC loop function on VIN7 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN7	0
5	AGCEN6	R/W	Select Video AGC loop function on VIN6 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN6	0
4	AGCEN5	R/W	Select Video AGC loop function on VIN5 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN5	0
3	AGCGAIN8[8]	R/W	AGCGAIN8 MSB bit	0
2	AGCGAIN7[8]	R/W	AGCGAIN7 MSB bit	0
1	AGCGAIN6[8]	R/W	AGCGAIN6 MSB bit	0
0	AGCGAIN5[8]	R/W	AGCGAIN5 MSB bit	0

0XAB – VIDEO AGC CONTROL

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN5[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN5 bit7-0.	F0h

0XAC – VIDEO AGC CONTROL

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN6[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN6 bit7-0.	F0h

0XAD – VIDEO AGC CONTROL

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN7[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN7 bit7-0.	F0h

0XAE – VIDEO AGC CONTROL

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN8[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGC GAIN8 bit7-0.	F0h

0XAF – VERTICAL PEAKING LEVEL CONTROL

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-4	VSHP6	R/W	Select VIN6 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP5	R/W	Select VIN5 Video Vertical peaking level. (*) 0: none. 7 : highest	0
*Note: VSHP must be set to '0' if page0 Reg0x83 COMB = 0.				

0XB0 – VERTICAL PEAKING LEVEL CONTROL

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-4	VSHP8	R/W	Select VIN8 Video Vertical peaking level. (*) 0: none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP7	R/W	Select VIN7 Video Vertical peaking level. (*) 0: none. 7 : highest	0

*Note: VSHP must be set to '0' if page0 Reg0x83 COMB = 0.

AUDIO ADC DIGITAL INPUT OFFSET CONTROL

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-6	AADC8OFS[9:8]	R/W	AIN8 Digital ADC input data offset control bit9-8.	0h
5-4	AADC7OFS[9:8]	R/W	AIN7 Digital ADC input data offset control bit9-8.	0h
3-2	AADC6OFS[9:8]	R/W	AIN6 Digital ADC input data offset control bit9-8.	0h
1-0	AADC5OFS[9:8]	R/W	AIN5 Digital ADC input data offset control bit9-8.	0h
Digital ADC input data offset control. Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.				

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC5OFS[7:0]	R/W	AIN5 Digital ADC input data offset control bit7-0.	0h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC6OFS[7:0]	R/W	AIN6 Digital ADC input data offset control bit7-0.	0h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC7OFS[7:0]	R/W	AIN7 Digital ADC input data offset control bit7-0.	0h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC8OFS[7:0]	R/W	AIN8 Digital ADC input data offset control bit7-0.	0h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-2	Reserved	R		0h
1-0	AADC52OFS[9:8]	R/W	AIN52 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by

ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

Bit	Function	R/W	Description	Reset
7-0	AADC52OFS[7:0]	R/W	AIN52 Digital ADC input data offset control bit7-0.	0h

ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-6	AUD8ADC[9:8]	R	Bit9-8 of AIN8 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD7ADC[9:8]	R	Bit9-8 of AIN7 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD6ADC[9:8]	R	Bit9-8 of AIN6 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD5ADC[9:8]	R	Bit9-8 of AIN5 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD8ADC[7:0]	R	Bit7-0 of AIN8 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD7ADC[7:0]	R	Bit7-0 of AIN7 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD6ADC[7:0]	R	Bit7-0 of AIN6 Analog Audio ADC Digital Output Value by 2's format.	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD5ADC[7:0]	R	Bit7-0 of AIN5 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-2	Reserved		Reserved	00h
1-0	AUD52ADC[9:8]	R	Bit9-8 of AIN52 Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	AUD52ADC[7:0]	R	Bit7-0 of AIN52 Analog Audio ADC Digital Output Value by 2's format.	X

ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

0XBD – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-6	ADJAADC8[9:8]	R	Bit9-8 of AIN8 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC7[9:8]	R	Bit9-8 of AIN7 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC6[9:8]	R	Bit9-8 of AIN6 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC5[9:8]	R	Bit9-8 of AIN5 adjusted Audio ADC Digital Input Data Value by 2's format.	X
The value shows the first input data in front of Digital Audio Decimation Filtering process.				

0XBE – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC5[7:0]	R	Bit7-0 of AIN5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBF – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC6[7:0]	R	Bit7-0 of AIN6 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC7[7:0]	R	Bit7-0 of AIN7 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC8[7:0]	R	Bit7-0 of AIN8 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-2			Reserved	00h
1-0	ADJAADC52[9:8]	R	Bit9-8 of AIN52 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

Bit	Function	R/W	Description	Reset
7-0	ADJAADC52[7:0]	R	Bit7-0 of AIN52 adjusted Audio ADC Digital Input Data Value by 2's format.	X

MPP PIN OUTPUT MODE CONTROL

0XC8 – MPP PIN OUTPUT MODE CONTROL

Bit	Function	R/W	Description	Reset
7	GPP_VAL6	R/W	Select the general purpose value through the MPP6 pin. 0 : "0" value, 1: "1" value	0h
6-4	MPP_MODE6	R/W	Select the output mode for MPP6 pin. Followings show the status when POLMPP6 register is set to 0. If POLMPP6 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1(Odd), High is field2(Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL6 register value. If VDLOSSOE register is set to "1", vdloss6 signal is output to MPP6 pin and these MPP_MODE6 function is not effective.	0h
3	GPP_VAL5	R/W	Select the general purpose value through the MPP5 pin. 0 : "0" value, 1: "1" value	0h
2-0	MPP_MODE5	R/W	Select the output mode for MPP5 pin. Followings show the status when POLMPP5 register is set to 0. If each POLMPP5 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1(Odd),High is field2(Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL5 register value. If VDLOSSOE register is set to "1", vdloss5 signal is output to MPP5 pin and these MPP_MODE5 function is not effective.	0h

0XC9 – MPP PIN OUTPUT MODE CONTROL

Bit	Function	R/W	Description	Reset
7	GPP_VAL8	R/W	Select the general purpose value through the MPP8 pin. 0 : “0” value, 1: “1” value	0h
6-4	MPP_MODE8	R/W	Select the output mode for MPP8 pin. Followings show the status when POLMPP8 register is set to 0. If POLMPP8 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1(Odd),High is field2(Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL8 registers value. If VDLOSSOE register is set to “1”, vdloss8 signal is output to MPP8 pin and these MPP_MODE8 function is not effective.	0h
3	GPP_VAL7	R/W	Select the general purpose value through the MPP7 pin. 0 : “0” value, 1: “1” value	0h
2-0	MPP_MODE7	R/W	Select the output mode for MPP7 pin. Followings show the status when POLMPP7 register is set to 0. If each POLMPP7 register is set to 1, following values have inversed status. 0: Horizontal sync output. Low is H-sync active. 1: Vertical sync output. Low is V-sync active. 2: Field flag output. Low is field1(Odd),High is field2(Even). 3: Horizontal active signal output. High is H-active. 4: Vertical active & horizontal active signal output. High is VH-active. 5: No video flag. High is No-video, Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL7 register value. If VDLOSSOE register is set to “1”, vdloss7 signal is output to MPP7 pin and these MPP_MODE7 function is not effective.	0h

0XCB – POLMPP5/6/7/8

Bit	Function	R/W	Description	Reset
7	POLMPP8	R/W	Select MPP8 pin output polarity. 0: normal, 1: inverse polarity.	0
6	POLMPP7	R/W	Select MPP7 pin output polarity. 0: normal, 1: inverse polarity.	0
5	POLMPP6	R/W	Select MPP6 pin output polarity. 0: normal, 1: inverse polarity.	0
4	POLMPP5	R/W	Select MPP5 pin output polarity. 0: normal, 1: inverse polarity.	0
3-0	Reserved	R		0

0XCE – ANALOG POWER DOWN CONTROL

Bit	Function	R/W	Description	Reset
7-4	Reserved	R		0
3-0	V_ADC_PWDN [8:5]	R/W	Power down the video ADC. V_ADC_PWDN[8:5] stands for VIN8 to VIN5. 0: Normal operation 1: Power down	0h

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

Index	Bit	Function	R/W	Description	Reset
0xD0	7-4	AIGAIN6	R/W	Select the amplifier's gain for each analog audio input AIN5/6/7/8/52. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 (default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	8h
0xD1		AIGAIN8	R/W		
0x7F		AIGAIN52	R/W		
0xD0	3-0	AIGAIN5	R/W		8h
0xD1		AIGAIN7	R/W		
0x7F		MIX_RATIO52	R/W	Audio input AIN52 ratio value for audio mixing	0h

0XDC – MIX_MUTE2

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5	MIX_DERATIO2	R/W	Disable the mixing ratio value for all audio5/6/7/8/52. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly	0
4-0	MIX_MUTE2	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0]: Audio input AIN5. MIX_MUTE[1]: Audio input AIN6. MIX_MUTE[2]: Audio input AIN7. MIX_MUTE[3]: Audio input AIN8. MIX_MUTE[4]: Reserved (no effect). 0:Normal 1:Muted.	00h

0X7E – MIX_MUTE_A52

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		1
5	MIX_MUTE_A52	R/W	MIX_MUTE_A52: Audio input AIN52 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH52[4:0]	R/W	AIN52 threshold value for audio detection	03h

0XDD – MIX RATIO VALUE

Bit	Function	R/W	Description	Reset
7-4	MIX_RATIO6	R/W	Audio input AIN6 ratio value for audio mixing	0
3-0	MIX_RATIO5	R/W	Audio input AIN5 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

Bit	Function	R/W	Description	Reset
7-4	MIX_RATIO8	R/W	Audio input AIN8 ratio value for audio mixing	0
3-0	MIX_RATIO7	R/W	Audio input AIN7 ratio value for audio mixing	0

AUDIO DETECTION THRESHOLD

0XE1 – AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7-4	Reserved	R		0
3	ADET_TH8[4]*	R/W	MSB bit of AIN8 threshold value for audio detection.	0
2	ADET_TH7[4]*	R/W	MSB bit of AIN7 threshold value for audio detection.	0
1	ADET_TH6[4]*	R/W	MSB bit of AIN6 threshold value for audio detection.	0
0	ADET_TH5[4]*	R/W	MSB bit of AIN5 threshold value for audio detection.	0

* Note :

ADET_TH :Define the threshold value for audio detection.

ADET_TH5: Audio input AIN5.

ADET_TH6: Audio input AIN6.

ADET_TH7: Audio input AIN7.

ADET_TH8: Audio input AIN8.
ADET_TH52: Audio input AIN52.

0:Low value (default)

.

.

.

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7-4	ADET_TH6[3:0]	R/W	Bit3-0 of AIN6 threshold value for audio detection.	3h
3-0	ADET_TH5[3:0]	R/W	Bit3-0 of AIN5 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

Bit	Function	R/W	Description	Reset
7-4	ADET_TH8[3:0]	R/W	Bit3-0 of AIN8 threshold value for audio detection.	3h
3-0	ADET_TH7[3:0]	R/W	Bit3-0 of AIN7 threshold value for audio detection.	3h

ENABLE VIDEO AND AUDIO DETECTION

0XFC – ENABLE VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-0	AVDET2_ENA	R/W	Enable state register updating and interrupt request of video and audio detection for each input. [0]: Video input VIN5. [1]: Video input VIN6. [2]: Video input VIN7. [3]: Video input VIN8. [4]: Audio input AIN5. [5]: Audio input AIN6. [6]: Audio input AIN7. [7]: Audio input AIN8. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	FFh

0X73 – ENABLE VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-1	Reserved	R	Reserved	00h
0	A52DET_ENA	R/W	Enable state register updating and interrupt request of audio AIN52 detection for each input. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	1

STATUS OF VIDEO AND AUDIO DETECTION

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-0	AVDET2_STATE	R/W	State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE. [0]: Video input VIN5. [1]: Video input VIN6. [2]: Video input VIN7. [3]: Video input VIN8. [4]: Audio input AIN5. [5]: Audio input AIN6. [6]: Audio input AIN7. [7]: Audio input AIN8. 0 Inactivated 1 Activated	00h

0X74 – STATUS OF VIDEO AND AUDIO DETECTION

Bit	Function	R/W	Description	Reset
7-1	Reserved	R		00h
0	A52DET_STATE	R/W	State of Audio AIN52 detection. This bit is activated according ADET_MODE. 0 Inactivated 1 Activated	0

0X54 – AIN5/6/7/8/52 AUDIO ADC CONTROL

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		0
5	DOUT_RST2	R/W	AIN5/6/7/8/52 Audio ADC digital output reset for all channel. This bit must be set up to 0 again after 1 value is set up.	0
4	DIV_RST2	R/W	AIN5/6/7/8/52 Audio ADC divider reset. This bit must be set up to 0 again after 1 value is set up.	0
3	ACALEN2	RW	AIN5/6/7/8/52 Audio ADC Calibration control. This bit must be set up to 0 again after 1 value is set up.	0
2-0	ASAVE2	R/W	AIN5/6/7/8/52 Audio ADC power save	7

0X58 – AVDS STATUS(TEST PURPOSE ONLY)

Bit	Function	R/W	Description	Reset
7	VSENSE8B	R	VIN8B AVDS VSENSE signal.	X
6	VSENSE7B	R	VIN7B AVDS VSENSE signal.	X
5	VSENSE6B	R	VIN6B AVDS VSENSE signal.	X
4	VSENSE5B	R	VIN5B AVDS VSENSE signal.	X
3	VSENSE8A	R	VIN8A AVDS VSENSE signal.	X
2	VSENSE7A	R	VIN7A AVDS VSENSE signal.	X
1	VSENSE6A	R	VIN6A AVDS VSENSE signal.	X
0	VSENSE5A	R	VIN5A AVDS VSENSE signal.	X

0X59 – AVDS POWER CONTROL (TEST PURPOSE ONLY)

Bit	Function	R/W	Description	Reset
7	PDBV8B	R/W	0: VIN8B AVDS power down. 1: VIN8B AVDS normal operation.	0
6	PDBV7B	R/W	0: VIN7B AVDS power down. 1: VIN7B AVDS normal operation.	0
5	PDBV6B	R/W	0: VIN6B AVDS power down. 1: VIN6B AVDS normal operation.	0
4	PDBV5B	R/W	0: VIN5B AVDS power down. 1: VIN5B AVDS normal operation.	0
3	PDBV8A	R/W	0: VIN8A AVDS power down. 1: VIN8A AVDS normal operation.	0
2	PDBV7A	R/W	0: VIN7A AVDS power down. 1: VIN7A AVDS normal operation.	0
1	PDBV6A	R/W	0: VIN6A AVDS power down. 1: VIN6A AVDS normal operation.	0
0	PDBV5A	R/W	0: VIN5A AVDS power down. 1: VIN5A AVDS normal operation.	0

0X5C– BGCTL2

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
5	BGCTL2	R/W	0: page1 Reg96[7:0] control all VIN5/6/7/8 video. 1: page1 Reg96[7:0] control only VIN5 video. page1 Reg5D[7:0] control only VIN6 video. page1 Reg5E[7:0] control only VIN7 video. page1 Reg5F[7:0] control only VIN8 video.	0
4-0	Reserved	R		1

0X96 – MISCELLANEOUS CONTROL II2(VIN5 ONLY OR VIN5/6/7/8)

Bit	Function	R/W	Description	Reset
7	NKILL_5	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_5	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_5	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_5	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_5	R/W	1 = Force decoder output value determined by CCS_5. 0 = Disabled.	0
2	LCS_5	R/W	1 = Enable pre-determined output value indicated by CCS_5 when video loss is detected. 0 = Disabled.	0
1	CCS_5	R/W	When FCS_5 is set high or video loss condition is detected when LCS_5 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_5	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5D – VIN6 MISCELLANEOUS CONTROL II ON BGCTL2=1

Bit	Function	R/W	Description	Reset
7	NKILL_6	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_6	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_6	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_6	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_6	R/W	1 = Force decoder output value determined by CCS_6. 0 = Disabled.	0
2	LCS_6	R/W	1 = Enable pre-determined output value indicated by CCS_6 when video loss is detected. 0 = Disabled.	0
1	CCS_6	R/W	When FCS_6 is set high or video loss condition is detected when LCS_6 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_6	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5E – VIN7 MISCELLANEOUS CONTROL II ON BGCTL2=1

Bit	Function	R/W	Description	Reset
7	NKILL_7	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_7	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_7	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_7	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_7	R/W	1 = Force decoder output value determined by CCS_7. 0 = Disabled.	0
2	LCS_7	R/W	1 = Enable pre-determined output value indicated by CCS_7 when video loss is detected. 0 = Disabled.	0
1	CCS_7	R/W	When FCS_7 is set high or video loss condition is detected when LCS_7 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_7	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5F – VIN8 MISCELLANEOUS CONTROL II ON BGCTL2=1

Bit	Function	R/W	Description	Reset
7	NKILL_8	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_8	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_8	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_8	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_8	R/W	1 = Force decoder output value determined by CCS_8. 0 = Disabled.	0
2	LCS_8	R/W	1 = Enable pre-determined output value indicated by CCS_8 when video loss is detected. 0 = Disabled.	0
1	CCS_8	R/W	When FCS_8 is set high or video loss condition is detected when LCS_8 is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_8	R/W	1 = Enable blue stretch. 0 = Disabled.	0

VIDEO OUTPUT MODE SELECTION

0X60 – VIDEO OUTPUT MODE

Bit	Function	R/W	Description	Reset
7-6	VD4MD	R/W	VD4[7:0] pin output mode selection 0: single D1 output 1: 2xD1 dual channel video output with 54MHz rate 2: 4xD1 quad channel video output with 108MHz rate 3: 4xCIF quad channel video output with 54MHz rate	1
5-4	VD3MD	R/W	VD3[7:0] pin output mode selection 0: single D1 output 1: 2xD1 dual channel video output with 54MHz rate 2: 4xD1 quad channel video output with 108MHz rate 3: 4xCIF quad channel video output with 54MHz rate	1
3-2	VD2MD	R/W	VD2[7:0] pin output mode selection 0: single D1 output 1: 2xD1 dual channel video output with 54MHz rate 2: 4xD1 quad channel video output with 108MHz rate 3: 4xCIF quad channel video output with 54MHz rate	1
1-0	VD1MD	R/W	VD1[7:0] pin output mode selection 0: single D1 output 1: 2xD1 dual channel video output with 54MHz rate 2: 4xD1 quad channel video output with 108MHz rate 3: 4xCIF quad channel video output with 54MHz rate	1

0X61 – VD1 OUTPUT CH12 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD1O2SEL	R/W	CH2 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	1h
3-0	VD1O1SEL	R/W	CH1 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	0h

0X62 – VD1 OUTPUT CH34 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD1O4SEL	R/W	CH4 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	3h
3-0	VD1O3SEL	R/W	CH3 data selection in VD1[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	2h

0X63 – VD2 OUTPUT CH12 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD2O2SEL	R/W	CH2 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	3h
3-0	VD2O1SEL	R/W	CH1 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	2h

0X64 – VD2 OUTPUT CH34 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD2O4SEL	R/W	CH4 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	5h
3-0	VD2O3SEL	R/W	CH3 data selection in VD2[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	4h

0X65 – VD3 OUTPUT CH12 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD3O2SEL	R/W	CH2 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	5h
3-0	VD3O1SEL	R/W	CH1 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	4h

0X65 – VD3 OUTPUT CH34 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD3O4SEL	R/W	CH4 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	7h
3-0	VD3O3SEL	R/W	CH3 data selection in VD3[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	6h

0X67 – VD4 OUTPUT CH12 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD4O2SEL	R/W	CH2 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	7h
3-0	VD4O1SEL	R/W	CH1 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	6h

0X68 – VD4 OUTPUT CH34 SELECT

Bit	Function	R/W	Description	Reset
7-4	VD4O4SEL	R/W	CH4 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	1h
3-0	VD4O3SEL	R/W	CH3 data selection in VD4[7:0] pin output. 0: VIN1 Video Decoder data 1: VIN2 Video Decoder data 2: VIN3 Video Decoder data 3: VIN4 Video Decoder data 4: VIN5 Video Decoder data 5: VIN6 Video Decoder data 6: VIN7 Video Decoder data 7: VIN8 Video Decoder data	0h

Electrical Information

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDD_{VM}	-0.5		4.5	V
VDDVDA (Measured to VSSVDA)	VDD_{VDAM}	-0.5		4.5	V
VDDAPLL(Measured to VSSAPLL)	VDD_{APLLM}	-0.5		4.5	V
VDDA (Measured to VSSA)	VDD_{AM}	-0.5		4.5	V
VDDI (Measured to VSS)	VDD_{IM}	-0.5		2.3	V
VDDO (Measured to VSS)	VDD_{OM}	-0.5		4.5	V
Digital Input/Output Voltage	-	–0.5		4.5	V
Analog Input Voltage	-	–0.5		3.3	V
Storage Temperature	T_S	–65		150	°C
Junction Temperature	T_J	-40		125	°C
Reflow Soldering (10-30 Seconds)	T_{PEAK}			255-260	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDD_V	3.0	3.3	3.6	V
VDDVDA (Measured to VSSVDA)	VDD_{VDA}	3.0	3.3	3.6	V
VDDAPLL (Measured to VSSAPLL)	VDD_{APLL}	3.0	3.3	3.6	V
VDDA (Measured to VSSA)	VDD_A	3.0	3.3	3.6	V
VDDI (Measured to VSS)	VDD_I	1.08	1.2	1.32	V
VDDO (Measured to VSS)	VDD_O	3.0	3.3	3.6	V
Analog Input Vpp (AC Coupling Required)	V_{AIN}	0	1.0	2.0	V
Ambient Operating Temperature	T_A	-40		85	°C

DC Electrical Parameters

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
DIGITAL INPUTS					
Input High Voltage	V_{IH}	2.0		3.6	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=3.3V or 0V)	I_L			±10	uA
Input Capacitance	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	9.3	18.2	29.5	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	7.4	11.8	16.5	mA
Tri-state Output Leakage Current (@V_O=3.3V or 0V)	I_{OZ}			±10	uA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
SUPPLY CURRENT					
Analog Video ADC Supply Current (VDDV, 3.3V)	I_{DDV}		115		mA
Analog Video DAC Supply Current (VDDVDA,3.3V)	I_{DDVDA}		71		mA
Analog Audio Supply Current (VDDA, 3.3V)	I_{DDA}		38		mA
Clock PLL Supply Current (VDDAPLL,3.3V)	I_{DDAPLL}		2.2		mA
Digital Internal Supply Current (VDDI, 1.2V)	I_{DDI}		32		mA
Digital I/O Supply Current (VDDO, 3.3V)	I_{DDO}		25		mA
Total Power Dissipation with Video Encoder	P		867.36		mW
Total Power Dissipation without Video Encoder	P		633.06		mW

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

CLKPO and Video Data Timing

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Setup from CLKPO(54MHz) to Video Data(54MHz)	1a	8.0		9.5	Ns
Hold from CLKPO(54MHz) to Video Data (54MHz)	1b	8.5		9.6	Ns
Setup from CLKPO(27MHz) to Video Data(54MHz)	2a	8		10	Ns
Hold from CLKPO(27MHz) to Video Data(54MHz)	2b	8		9	Ns
Setup from CLKPO(108MHz) to Video Data(108MHz)	3a	3.7		4.8	Ns
Hold from CLKPO(108MHz) to Video Data (108MHz)	3b	4.1		4.9	Ns

NOTE:

1. CLKPO timing is related with CLKPO_DEL register value. The following timing diagram is illustrated in the case that the CLKPO_DEL is set to 0hex and CLKPO_POL is set to 0.CLKNO timing is inversed CLKPO timing as default setting.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2.

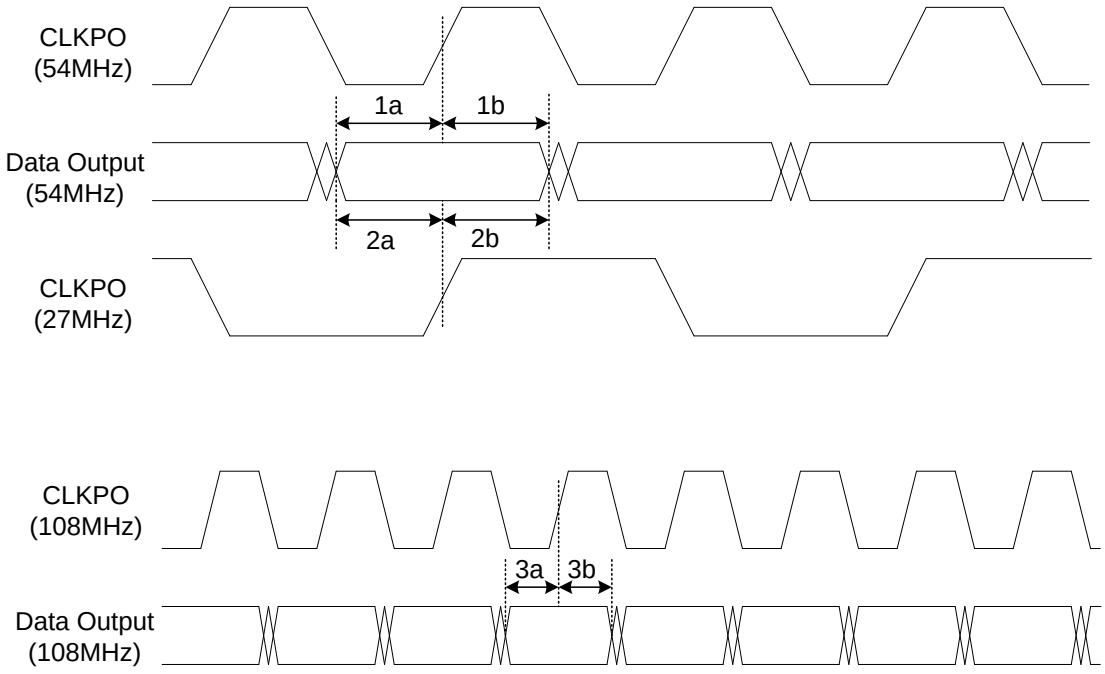


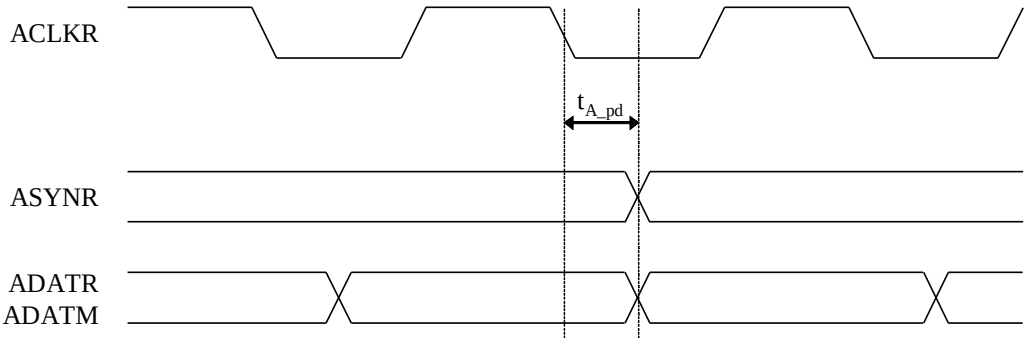
FIGURE 44. CLKPO AND VIDEO DATA TIMING DIAGRAM

Digital Serial Audio Interface Timing

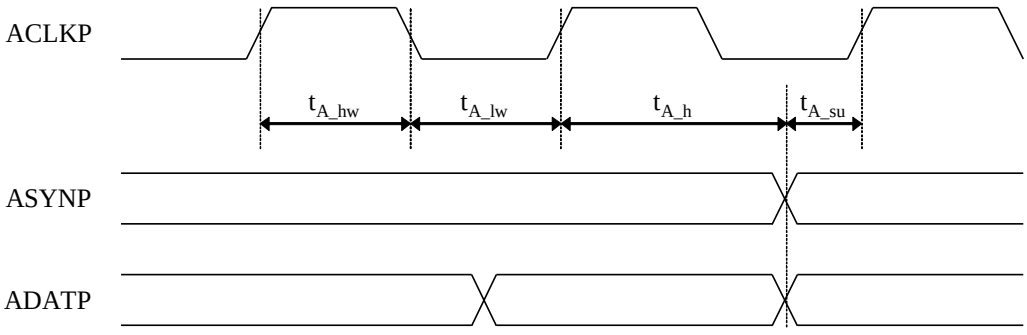
PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
ASYNR,ADATR,ADATM Propagation Delay	T_{A_pd}	1.0		4	ns
ACLKP High Pulse Duration	T_{A_hw}	37			ns
ACLKP Low Pulse Duration	T_{A_lw}	74			ns
ASYNP, ADATP Setup Time	T_{A_su}	36			ns
ASYNP, ADATP Hold Time	T_{A_h}	35			ns

NOTE:

1. T_{A_lw} Min value and T_{A_su} Min value are Fs=48KHz mode only. If Fs < 48KHz, these Min values are more bigger. High period of ACLKR/ACLKP is 27MHz one clock period.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



(a) Record and Mix Audio (Master mode)



(b) Playback Audio (Master mode)

FIGURE 45. TIMING DIAGRAM OF DIGITAL SERIAL AUDIO INTERFACE

Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Bus Free Time Between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	100			Ns
SDAT Hold Time(XTI 108MHz)	t_{hSDAT}	50			Ns
SDAT Hold Time (XTI 54MHz)		100			Ns
SDAT Hold Time (XTI 27MHz)		150			Ns
Setup Time for START Condition	t_{sSTA}	370			Ns
Setup Time for STOP Condition	t_{sSTOP}	370			Ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
LOW Period of SCLK	t_{LOW}	0.5			us
HIGH Period of SCLK	t_{HIGH}	0.5			us
SCLK Clock Frequency (XTI 108MHz)	f_{SCLK}			400	KHz
SCLK Clock Frequency (XTI 54MHz)				350	KHz
SCLK Clock Frequency (XTI 27MHz)				300	KHz

NOTE:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

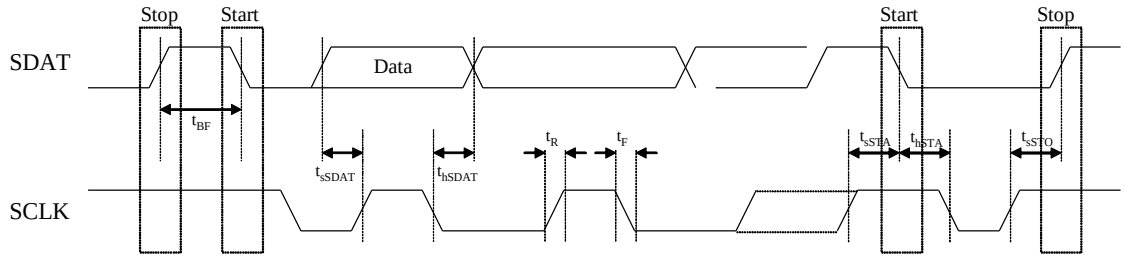


FIGURE 46. SERIAL HOST INTERFACE TIMING

Video Decoder Parameter 1

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
ADCS					
ADC Resolution	ADCR	-	10	-	Bits
ADC Integral Non-linearity	AINL	-	±1	-	LSB
ADC Differential Non-linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	fADC	24	27	30	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	fLN	-	15.625	-	KHz
Line Frequency (60Hz)	fLN	-	15.734	-	KHz
Static Deviation	ΔfH	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	fSC	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	fSC	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	fSC	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	fSC	-	3582056	-	Hz
Lock In Range	ΔfH	±450	-	-	Hz
OSCILLATOR INPUT					
Nominal Frequency		-	27	-	MHz
Deviation		-	-	±50	ppm
Duty Cycle		-	-	55	%

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Video Decoder Parameter 2

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
LOCK SPECIFICATION					
Sync Amplitude Range		1		200	%
Color Burst Range		5		200	%
Horizontal Lock Range		-5		5	%
Vertical Lock Range		45		65	Hz
Fsc Lock Range			±450		Hz
Color Burst Position Range			±2.2		μs
Color Burst Width Range					cycle
VIDEO BANDWIDTH					
B/W			6		MHz
NOISE SPECIFICATION					
SNR (Luma Flat Field)			57		dB
NONLINEAR SPECIFICATION					
Y Nonlinearity			0.5	0.7	%
Differential Phase	DP		0.4	0.6	Degree
Differential Gain	DG		0.6	0.8	%
CHROMA SPECIFICATION					
Hue Accuracy			1		Degree
Chroma ACC Range				400	%
Chroma Amplitude Error			1		%
Chroma Phase Error			0.3		%
Chroma Luma Intermodulation			0.2		%
K-FACTOR					
K_{2T}			0.5		%
$K_{pulse/bar}$			0.5		%

NOTE:

1. COMPLIANCE TO DATASHEET LIMITS IS ASSURED BY ONE OR MORE METHODS: PRODUCTION TEST, CHARACTERIZATION AND/OR DESIGN.

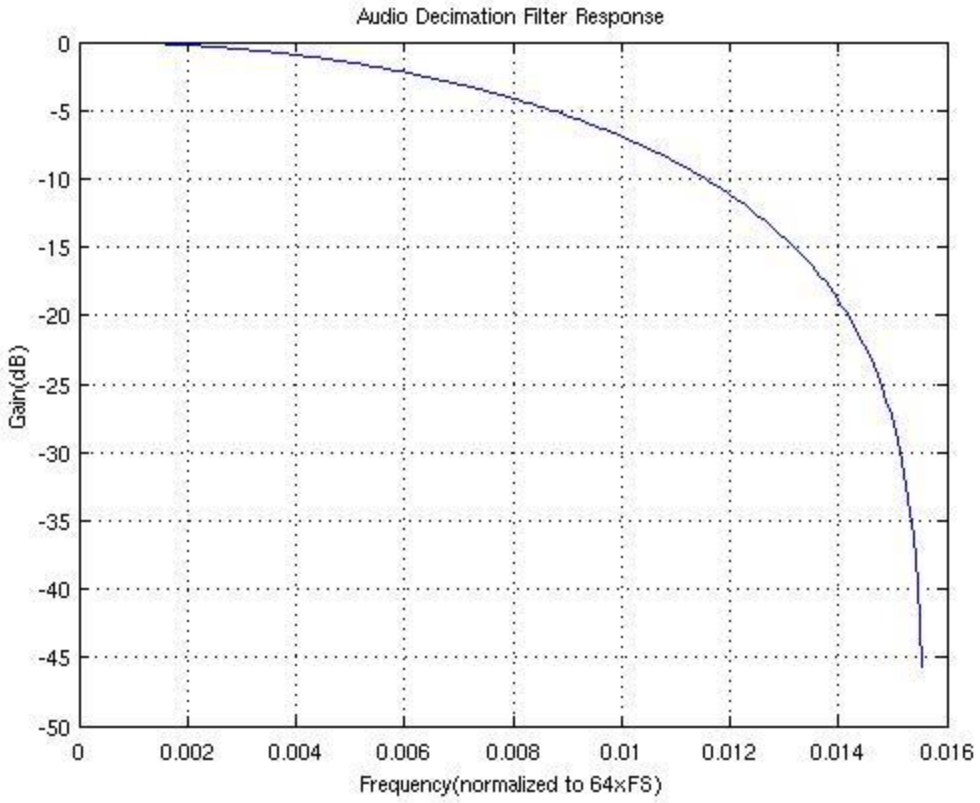
Analog Audio Parameters

PARAMETER	SYMBOL	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG AUDIO INPUT CHARACTERISTICS					
AIN1/2/3/4/51/5/6/7/8/52 Input Impedance	RINX	10			Kohm
Interchannel Gain Mismatch			0.2		dB
Input Voltage Range				2	Vpp
Full Scale Input Voltage (Note Note:)	ViFULL		1		Vpp
Interchannel Isolation (Note 2)			90		dB
ANALOG AUDIO OUTPUT CHARACTERISTICS					
AOUT Output Load Resistance	RLAO	2K	10K		ohm
AOUT Load Capacitance	CLAO		20	1000	pF
AOUT Offset Voltage	VOSAO			100	mV
Full Scale Output Voltage (Note 3)	Vo_{FULL}		2.0	2.5	Vpp

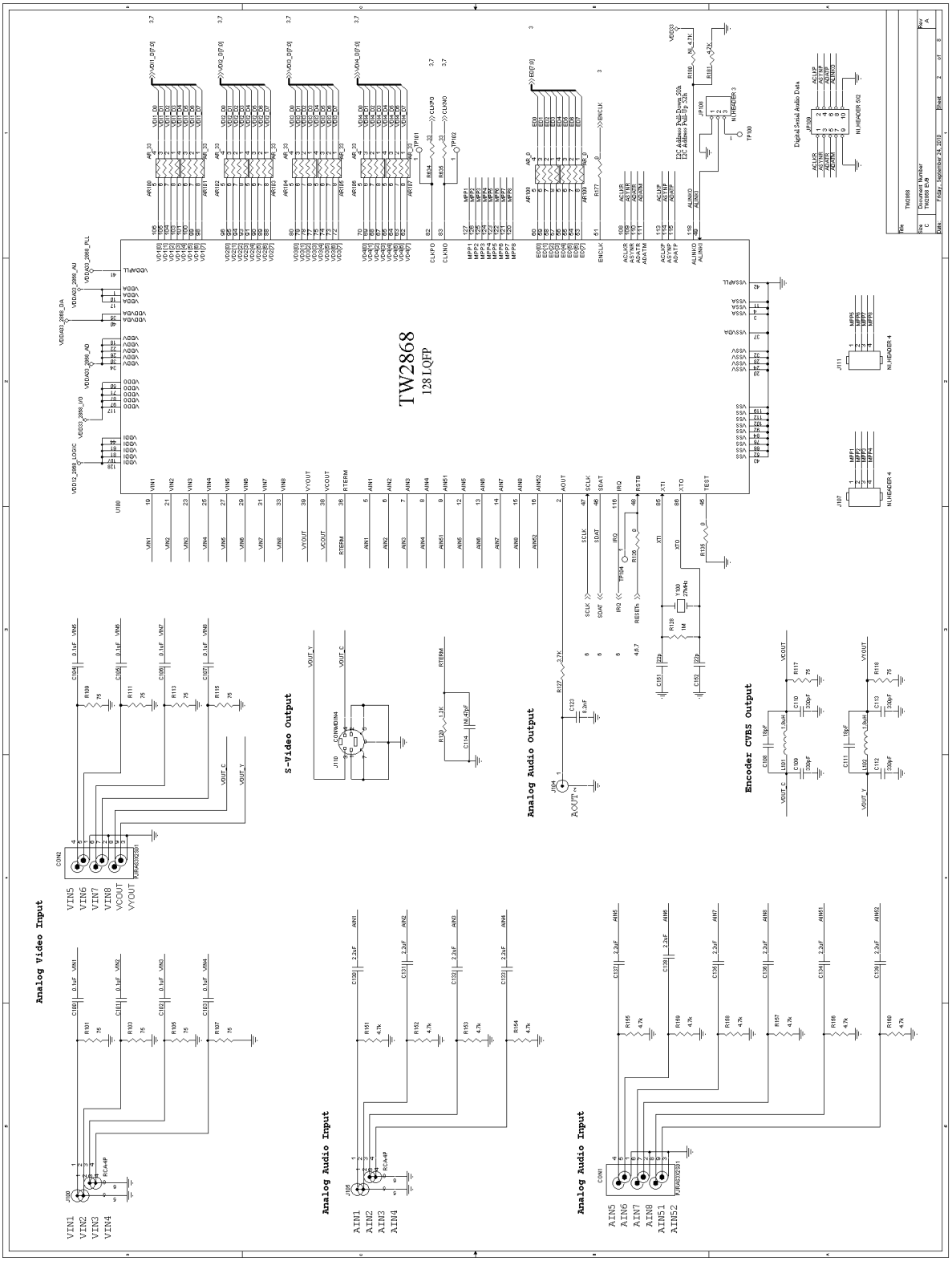
NOTE:

1. Tested at input gain of 0 dB, Fin = 1KHz.
2. Tested at input gain of 0 dB, Fs=8 KHz and 16KHz.
3. Tested at output gain of 0 dB, Fout = 1KHz.
4. COMPLIANCE TO DATASHEET LIMITS IS ASSURED BY ONE OR MORE METHODS: PRODUCTION TEST, CHARACTERIZATION AND/OR DESIGN.
4.

Audio Decimation Filter Response

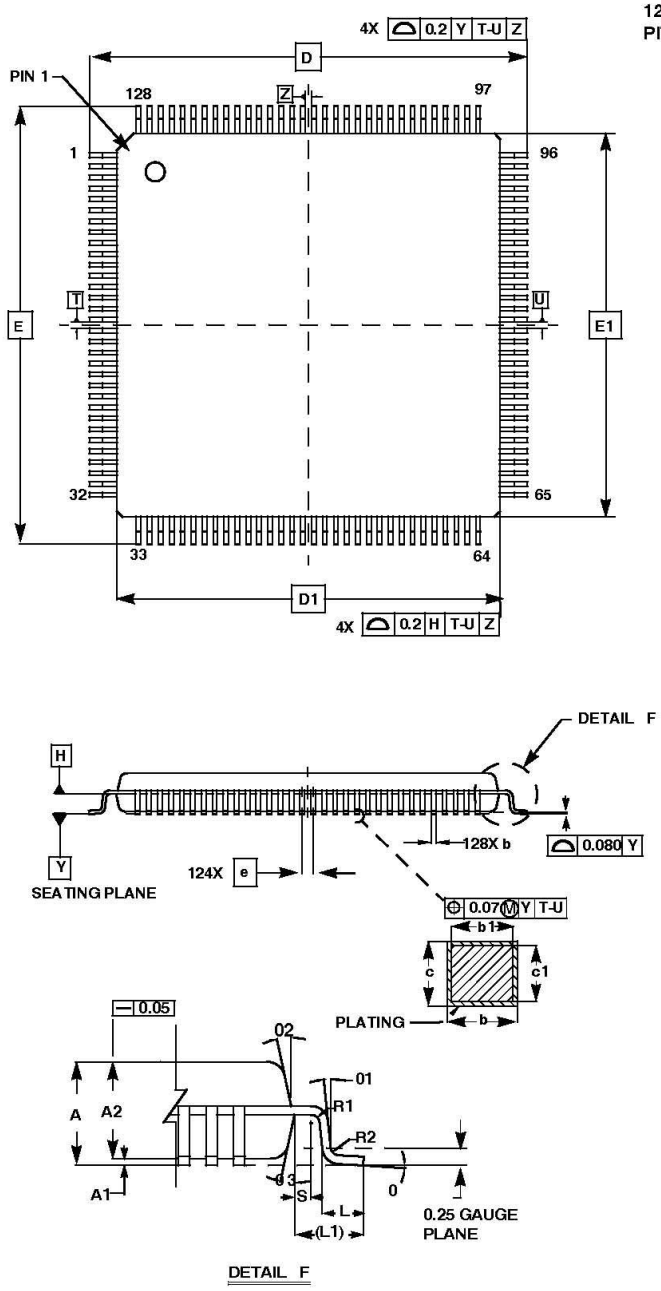


Application Schematic



Package Dimension

Low Plastic Quad Flatpack Packages (LQFP)



Q128.14x14

128 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH

SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D	16 BSC			-
D1	14 BSC			3
E	16 BSC			-
E1	14 BSC			3
L	0.45	0.60	0.75	-
L1	1.00 REF			-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N	128			-
e	0.40 BSC			-

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NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

Revision History

REVISION	DATE	DESCRIPTION
FN7796.3	May 7, 2013	Changed the text for the AOFFCORE description on page 108 and added sentence. From: 0: Audio No-input Noise reduction on 1: Audio No-input Noise reduction off To: 0: Audio No-input Noise reduction on (default) 1: Audio No-input Noise reduction off This bit must be set to a 1 ("No-input Noise reduction off") when the TW2868 is initialized. If this bit stays at its default setting (0), the TW2868 may generate unwanted noise.
FN7796.2	November 5, 2012	In “Absolute Maximum Ratings” on page 188, corrected T_J MIN from “0°C” to “-40°C”.
FN7796.1	January 4, 2012	Change part number in “Ordering Information” on page 10 from TW2868-LA1-CR to TW2868-LA2-CR.
FN7796.0	August 9, 2011	Initial release