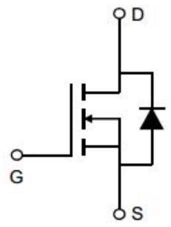
迈诺斯科技

MP70N10

100V N-Channel MOSFET



Schematic diagram

TO-220

Description

MP70N10, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

FEATURES

① V_{DS}=100V,I_D=70A $R_{DS(ON)}$<21mΩ@VGS=10V
② Fast switching
③ 100% avalanche tested
④ Improved dv/dt capability

APPLICATIONS

① Switch Mode Power Supply(SMPS)
② Uninterruptible Power Supply(UPS)
③ Power Factor Correction(PFC)

Package Marking And Ordering Information：

Ordering Codes	Package	Product Code	Packing
MP70N10	TO-220	MP70N10	Tube

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
		TO-220	
Drain-Source Voltage (VGS = 0V)	V_{DSS}	100	V
Continuous Drain Current	I_D	70	A
Pulsed Drain Current (note1)	I_{DM}	Figure 6	A
Gate-Source Voltage	V_{GSS}	±20	V
Single Pulse Avalanche Energy (note2)	E_{AS}	1943	mJ
Avalanche Current (note1)	I_{AR}	32	A
Repetitive Avalanche Energy (note1)	E_{AR}	36	mJ
Power Dissipation (TC = 25ºC)	P_D	200	W
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to175	℃

Thermal Resistance

Parameter	Symbol	Value	Unit
		TO-220	
Thermal Resistance, Junction-to-Case	R_{thJC}	0.75	℃/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62	

Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Valu			Uni t
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V, T_J = 25ºC	-	--	1	μA
		V_{DS} = 80V, V_{GS} = 0V, T_J = 125ºC	-	--	100	
Gate-Source Leakage	I_{GSS}	V_{GS} = +20V,V_{DS}=0V	-	--	100	nA
		V_{GS}=-20V, V_{DS}=0V	-	--	-100	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 28A	-	17	21	mΩ
Forward Transconductance	gfs	V_{DS} = 10V, I_D = 28A		85		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	2700	--	pF
Output Capacitance	C_{oss}		-	610	--	
Reverse Transfer Capacitance	C_{rss}		--	260	--	
Total Gate Charge	Q_g	V_{DD} =50V, I_D = 28A, V_{GS} = 0 to 10V	-	60	--	nC
Gate-Source Charge	Q_{gs}		-	15	--	
Gate-Drain Charge	Q_{gd}		--	45	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D =28A, V_{GS}= 10V, R_G = 2.5 Ω	-	20	--	ns
Turn-on Rise Time	t_r		-	28	--	
Turn-off Delay Time	$t_{d(off)}$		-	65	--	
Turn-off Fall Time	t_f		-	15	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25 ºC	--	--	70	A
Pulsed Diode Forward Current	I_{SM}		-	--	230	
Body Diode Voltage	V_{SD}	T_J = 25℃, I_{SD} = 28A, V_{GS} = 0V	-	--	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0V,I_S = 28A, dI_F/dt =100A /μs	--	195	--	ns
Reverse Recovery Charge	Q_{rr}		--	107	--	μC

Notes

1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.I_{AS}= 30A, V_{DD}= 50V, R_G= 25 Ω, Starting T_J= 25ºC

3.Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤1%

Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

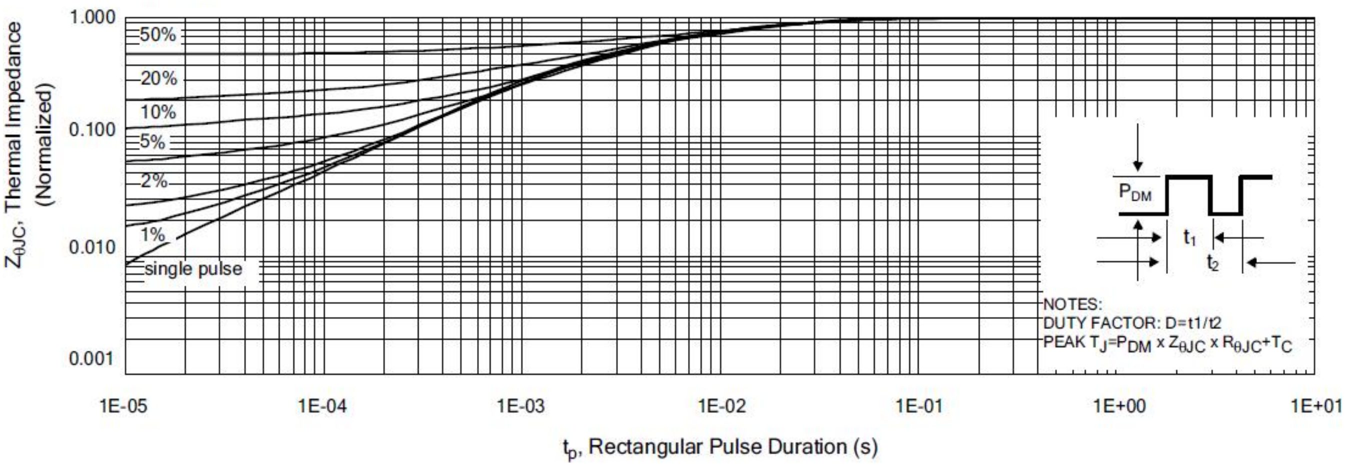


Figure 2. Maximum Power Dissipation vs Case Temperature

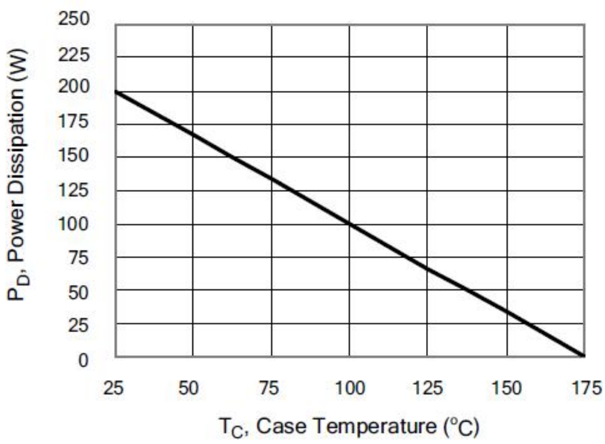


Figure 3. Maximum Continuous Drain Current vs Case Temperature

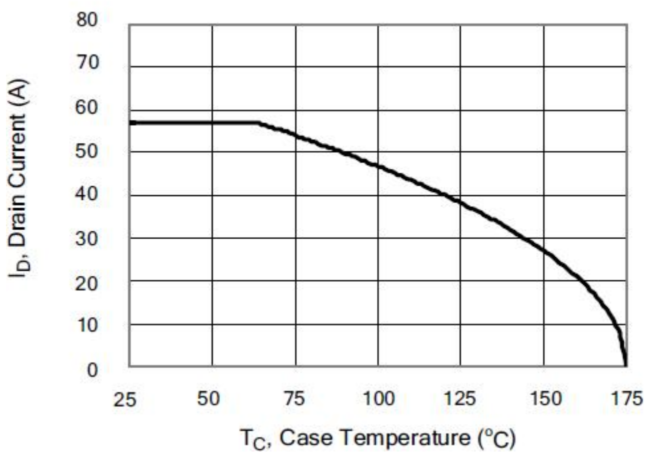


Figure 4. Typical Output Characteristics

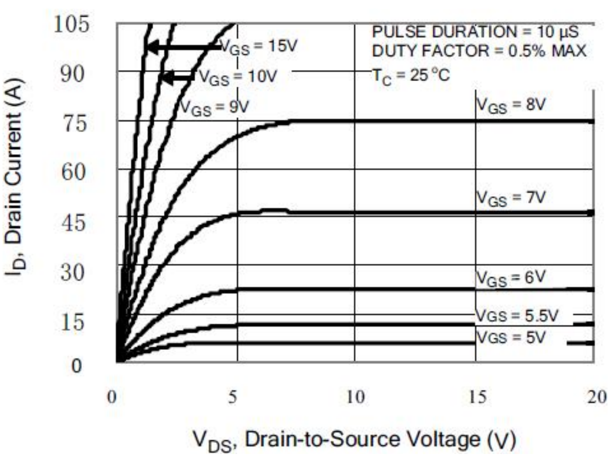
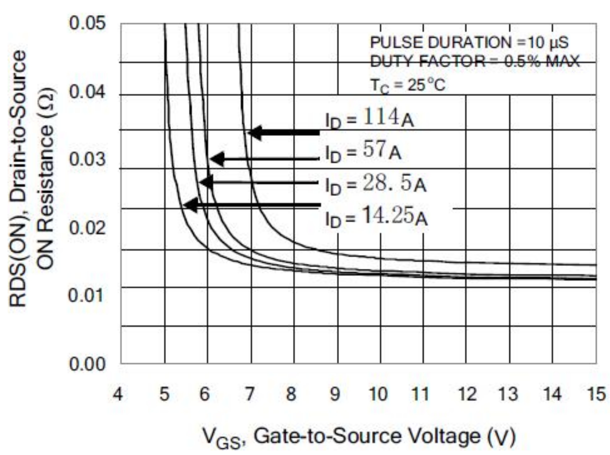


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 6. Maximum Peak Current Capability

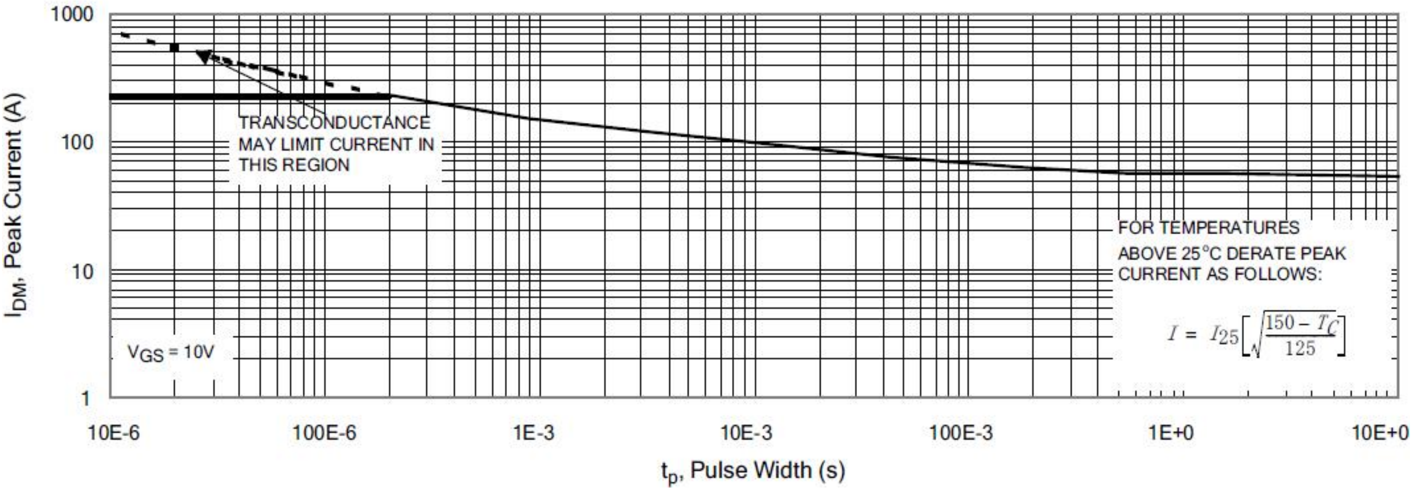


Figure 7. Typical Transfer Characteristics

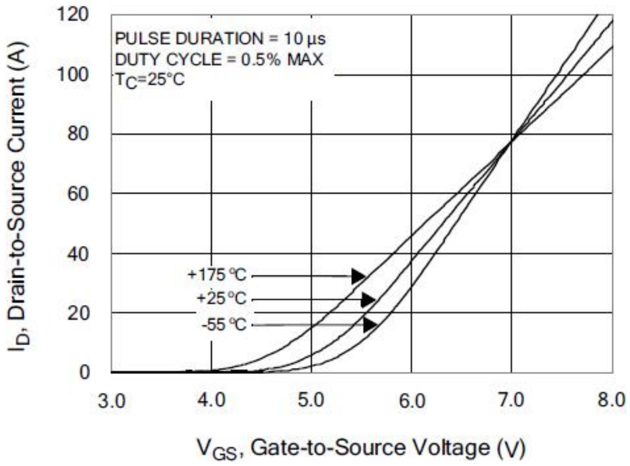


Figure 8. Unclamped Inductive Switching Capability

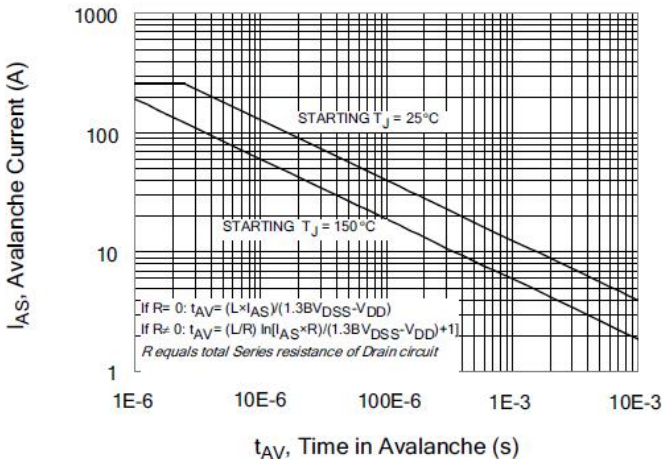


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

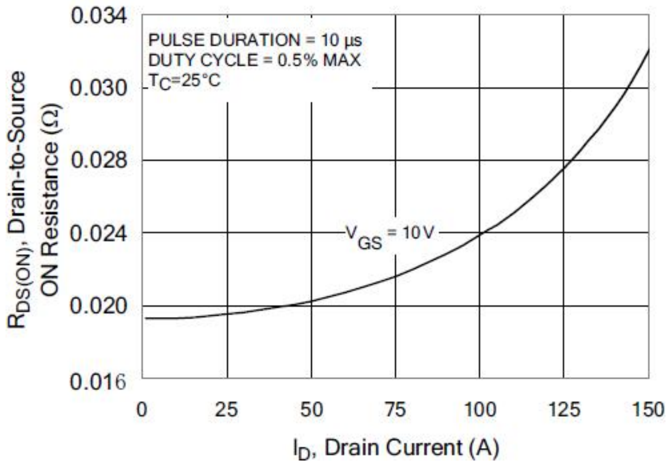
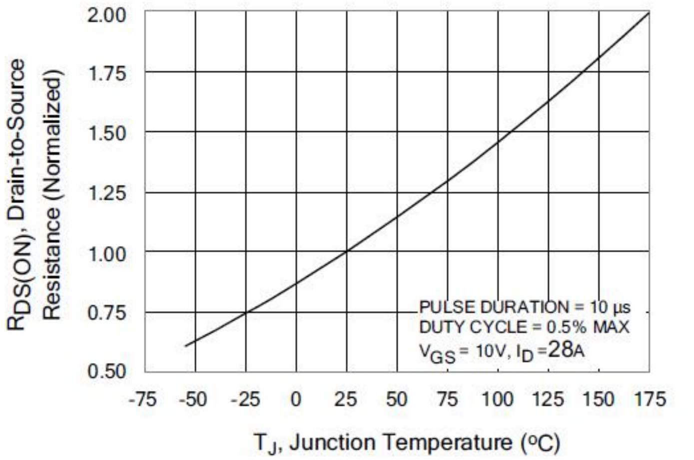


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



Typical Characteristics TJ = 25℃, unless otherwise noted

Figure 11. Typical Breakdown Voltage vs Junction Temperature

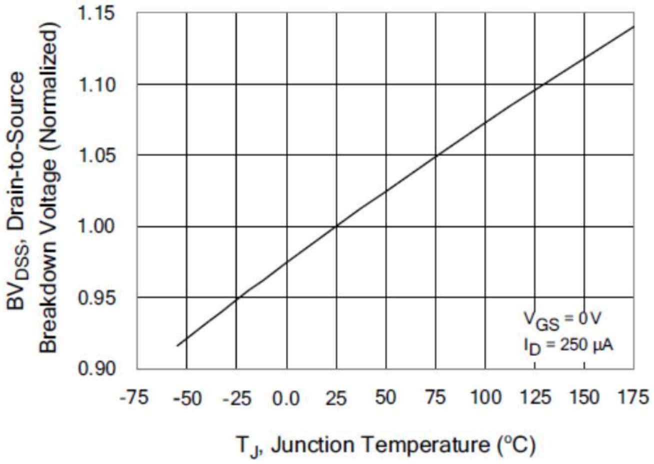


Figure 12. Typical Threshold Voltage vs Junction Temperature

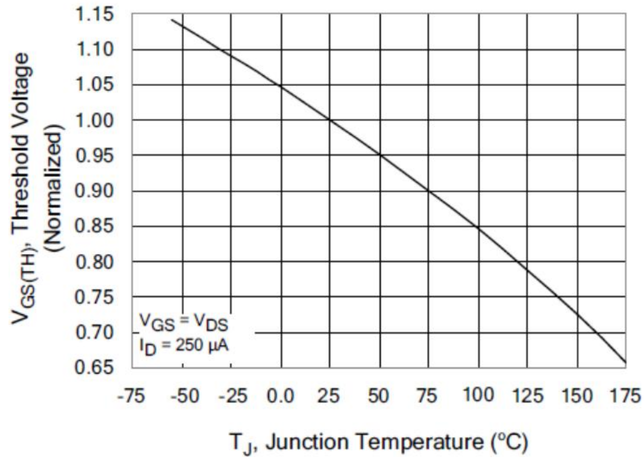


Figure 13. Maximum Forward Bias Safe Operating Area

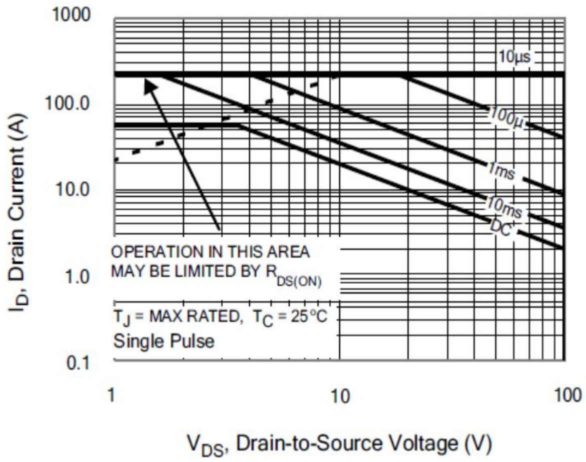


Figure 14. Capacitance vs Vds

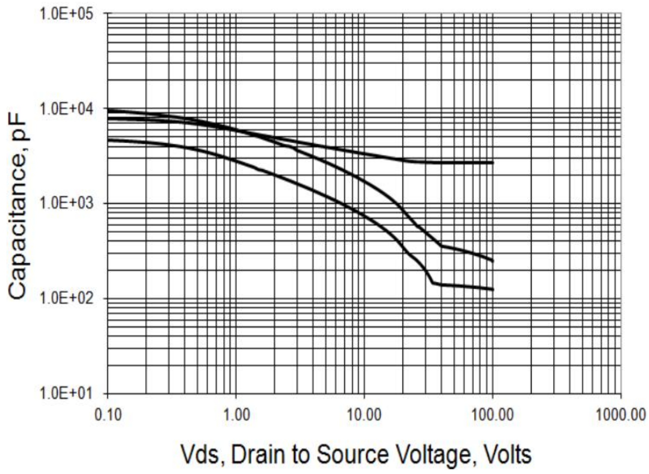


Figure 15 .Typical Gate Charge

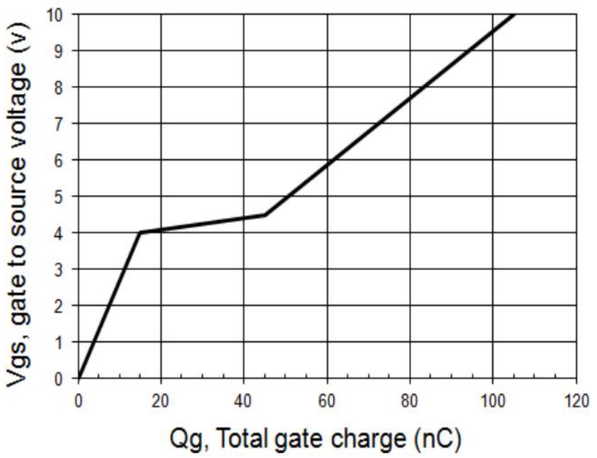


Figure 16. Typical Body Diode Transfer Characteristics

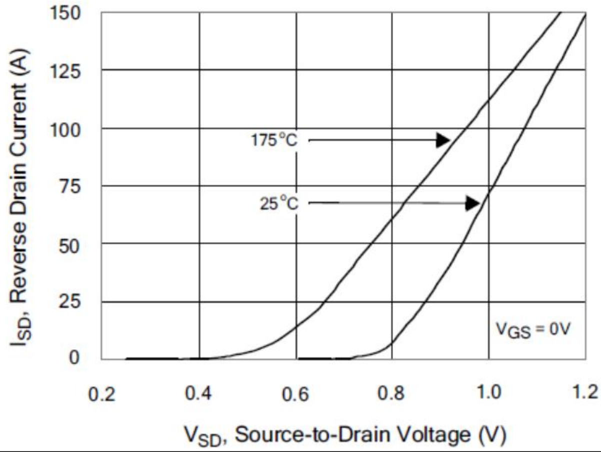


Figure A：Gate Charge Test Circuit and Waveform

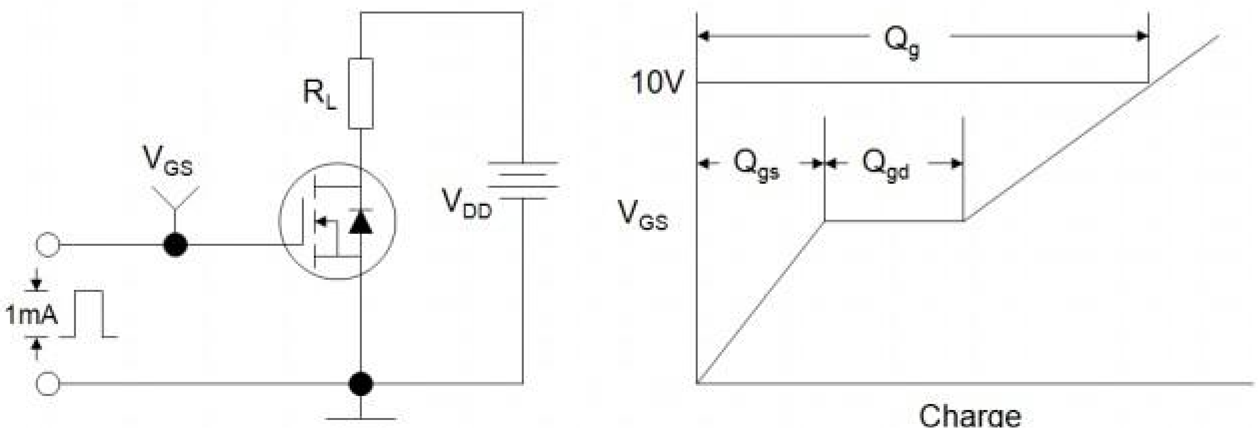


Figure B：Resistive Switching Test Circuit and Waveform

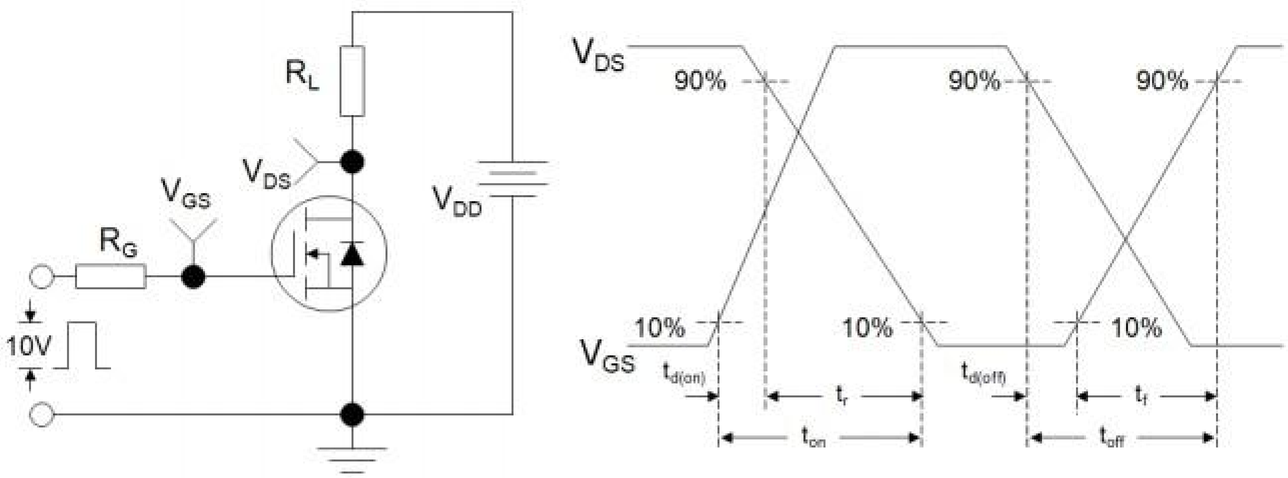
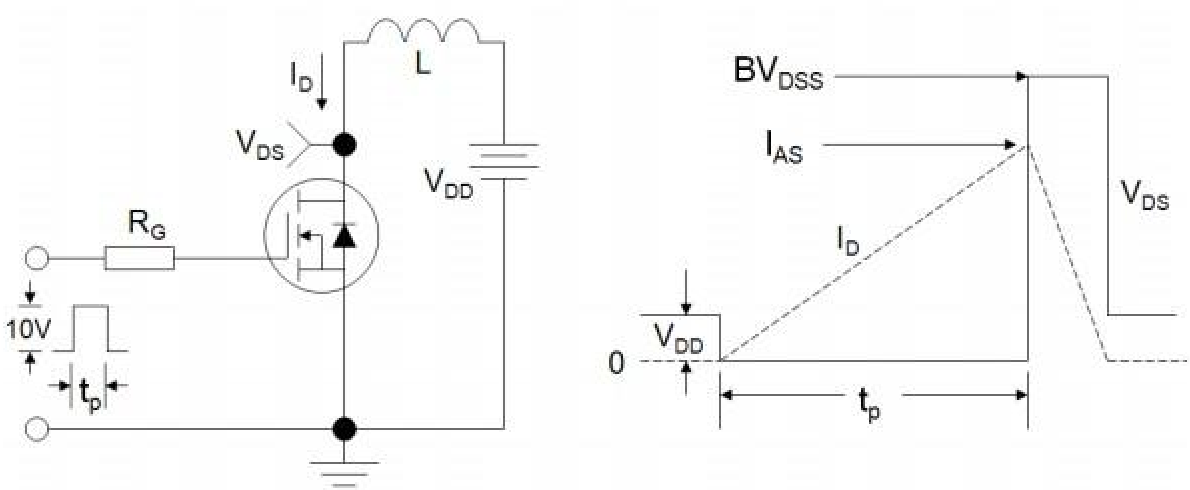


Figure C：Unclamped Inductive Switching Test Circuit and Waveform



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change withoutprior notice.

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