1 Features

- 5kVRMS single channel isolated gate driver
- 2.5A Out peak current
- 14V to 33V output driver supply voltage
- Rail-to-rail output
- 120ns (maximum) propagation delay
- 25ns (maximum) part-to-part delay matching
- 35ns (maximum) pulse width distortion
- 100kV/μs (minimum) common-mode transient immunity (CMTI)
- Stretched SOP6W package with ⩾7.5mm creepage and clearance
- CMOS input
- Operating junction temperature, TJ: –40°C to +125°C
- Safety-related certifications (Planned):
  --UL 1577
  --CQC certification per GB4943.1-2011

2 Applications

- Industrial motor-control drives
- Industrial power supplies, UPS
- Solar inverters
- Induction heating

3 Description

The XN2810 is a single channel, isolated gate driver for IGBTs, MOSFETs and SiC MOSFETs, with 2.5A source and 2.5 A sink peak output current and 5KVRMS reinforced isolation rating. The high supply voltage range of 33V allows the use of bipolar supplies to effectively drive IGBTs and SiC power FETs. XN2810 can drive both low side and high side power FETs. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, and small pulse width distortion. Tight process control results in small part-to-part skew. It is offered in a stretched SOP6W package with⩾7.5mm creepage and clearance. XN2810 high performance and reliability makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances. The higher operating temperature opens up opportunities for applications not previously able to be supported by traditional gate driver.

4 Functional Block Diagram

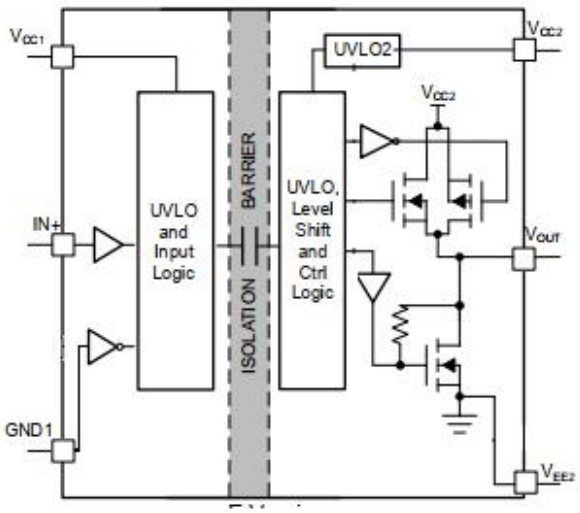


Figure 1. Block Diagram

5 Pin Configuration and Function

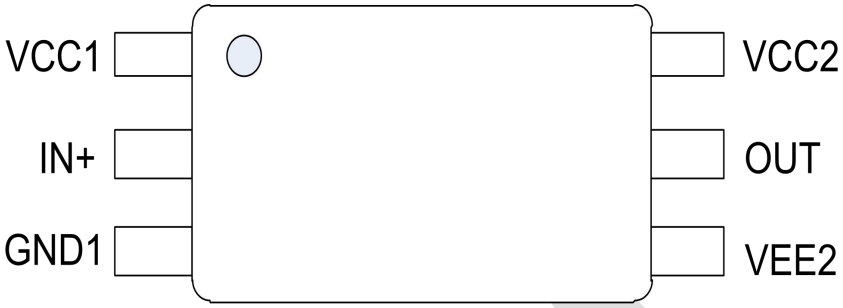


Figure 2、PIN Configuration

PIN		TYPE	DESCRIPTION
NAME	XN2810E		
VCC1	1	P	Input supply voltage.
IN+	2	I	gate-drive voltage-control input.
GND1	3	G	Input ground.
VEE2	4	P	Negative output supply
OUT	5	O	Gate-drive output
VCC2	6	P	Positive output supply/

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)(1)

DESCRIPTION	PARAMETER	MIN	MAX	UNIT
Input bias pin supply voltage	VCC1 – GND1	GND1 – 0.3	18	V
Driver bias supply	VCC2 – VEE2	–0.3	35	V
Output signal voltage	VOUT – VEE2	VEE2 – 0.3	VCC2 + 0.3	V
Input signal voltage	VIN+ – GND1	GND1 – 5	VCC1 + 0.3	V
Junction temperature, TJ(2)		–40	125	°C
Storage temperature, Tstg		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) To maintain the recommended operating conditions for TJ.

6.2 ESD Ratings

PARAMETER	DESCRIPTION	VALUE	UNIT
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001(1)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VCC1	Supply voltage, input side	3		15	V
VCC2	Positive supply voltage output side (VCC2 – VEE2)	12.4		33	V
TA	Ambient temperature	-40		125	°C

6.4 Insulation Specifications for SOP6W Package

	PARAMETER	TEST CONDITIONS	VALUE DWV	UNIT
CLR	External Clearance(1)	Shortest pin–to-pin distance through air	⩾ 7.5	mm
CPG	External Creepage(1)	Shortest pin–to-pin distance across the package surface	⩾ 7.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ⩽ 600 VRMS	I-III	
		Rated mains voltage ⩽ 1000 VRMS	I-II	
DIN V VDE 0884–11: 2017–01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC Voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) ; $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50-μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	⩽ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation resistance, input tooutput(5)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases.Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.

6.5 Electrical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1μF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1μF capacitor from V_{CC2} to V_{EE2}, C_{Load} = 100pF, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input supply quiescent current			1.8	3	mA
I_{VCC2}	Output supply quiescent current			1	2	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
$V_{IT+(UVLO1)}$	VCC1 Positive-going UVLO threshold voltage			2.7	2.9	V
$V_{IT-(UVLO1)}$	VCC1 Negative-going UVLO threshold voltage		2.5	2.6		V
$V_{hys(UVLO1)}$	VCC1 UVLO threshold hysteresis			0.1		V
$V_{IT+(UVLO2)}$	VCC2 Positive-going UVLO threshold voltage			11.4	12.4	V
$V_{IT-(UVLO2)}$	VCC2 Negative-going UVLO threshold voltage		9.4	10.4		V
$V_{hys(UVLO2)}$	VCC2 UVLO threshold voltage hysteresis			1		V
LOGIC I/O						
$V_{IT+(IN)}$	Positive-going input threshold voltage (IN+, IN–)	V_{CC1}=5V		0.55×V_{CC1}	0.7×V_{CC1}	V
$V_{IT-(IN)}$	Negative-going input threshold voltage (IN+, IN–)	V_{CC1}=5V	0.3×V_{CC1}	0.45×V_{CC1}		V
$V_{hys(IN)}$	Input hysteresis voltage (IN+, IN–)			0.1 × V_{CC1}		V
I_{IH}	High-level input leakage at IN+	IN+ = V_{CC1}		40	240	μA
GATE DRIVER STAGE						
V_{OH}	High-level output voltage	I_{OUT} = –20 mA	14.0	14.2		V
V_{OL}	Low level output voltage	IN+ = low, IN– = high; I_O = 20 mA		0.01	0.2	V
I_{OH}	Peak source current	IN+ = high			-2.5	A
I_{OL}	Peak sink current	IN+ = low	2.5			A
ACTIVE PULLDOWN						
V_{OUTSD}	Active pulldown voltage on OUT	I_{OUT} = 0.1 × $I_{OUTL(typ)}$, V_{CC2} =open		1.8	2.5	V

6.6 Switching Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1μF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1μF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output-signal rise time	C_{LOAD} = 1 nF		10	20	ns
t_f	Output-signal fall time	C_{LOAD} = 1 nF		10	20	ns
t_{PLH}	Propagation delay (default versions), high	C_{LOAD} = 100 pF		90	120	ns
t_{PHL}	Propagation delay (default versions), low	C_{LOAD} = 100 pF		90	120	ns
t_{UVLO1_rec}	UVLO recovery delay of V_{CC1}			35	/	us
t_{UVLO2_rec}	UVLO recovery delay of V_{CC2}			60	/	us
t_{PWD}	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	C_{LOAD} = 100 pF		1	20	ns
$t_{sk(pp)}$	Part-to-part skew(1)	C_{LOAD} = 100 pF		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or V_{CC1}, V_{CM} = 1200 V	100	120		kV/μs

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

6.7 Typical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1μF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1μF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)

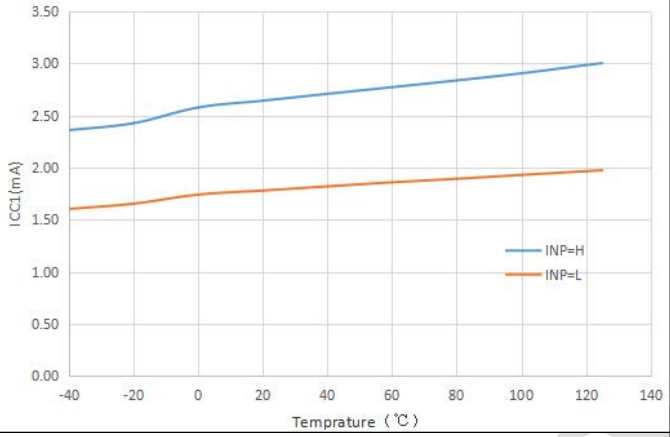


Figure 3. I_{CC1} Supply Current vs Temperature

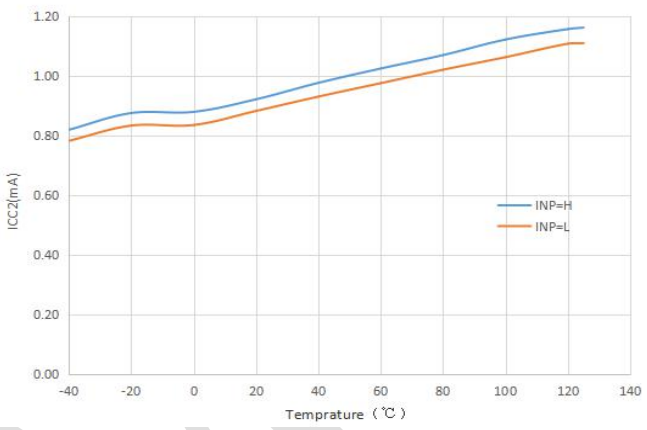


Figure 4. I_{CC2} Supply Current vs Temperature

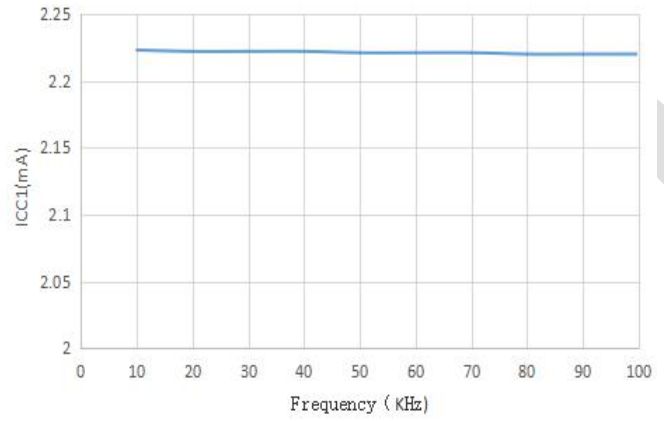


Figure 5. I_{CC1} Supply Current vs Input Frequency

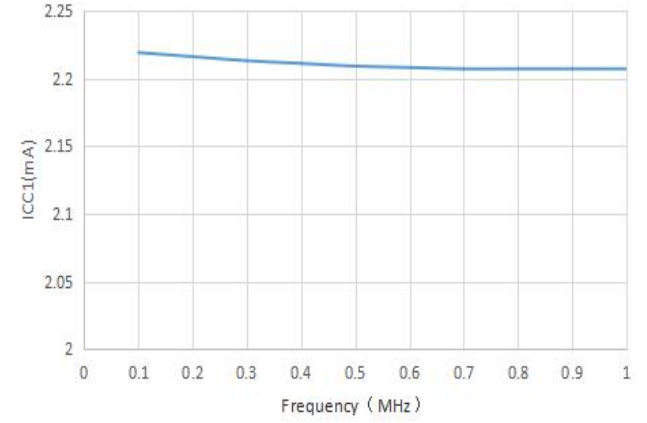


Figure 6. I_{CC1} Supply Current vs Input Frequency

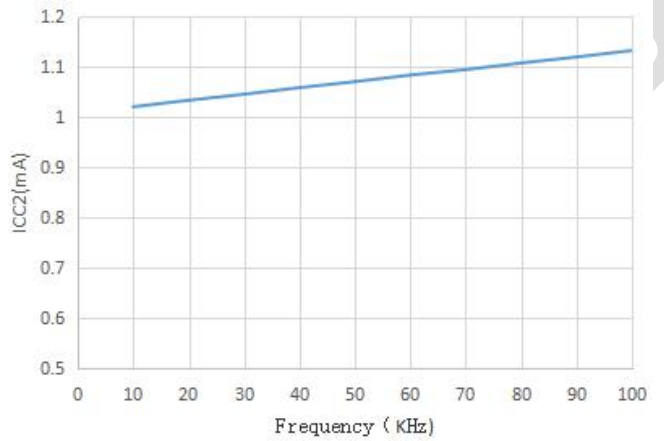


Figure 7. I_{CC2} Supply Current vs Input Frequency

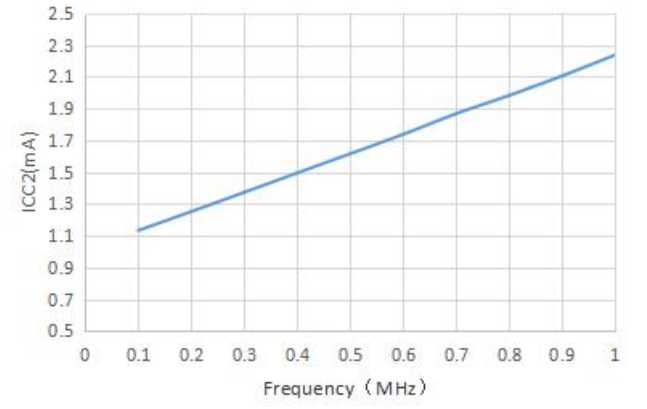


Figure 8. I_{CC2} Supply Current vs Input Frequency

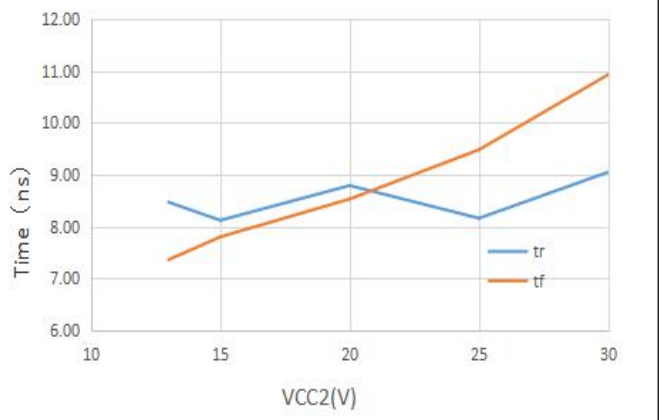


Figure 9. Fall & Rise Time vs VCC2

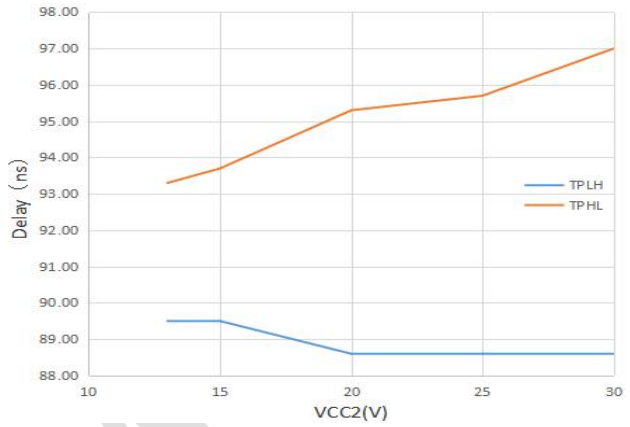


Figure 10. Delay Time vs VCC2

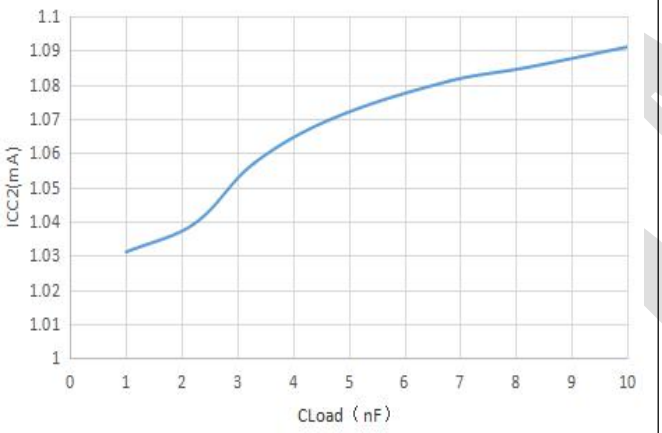


Figure 11. ICC2 vs C_{LOAD}

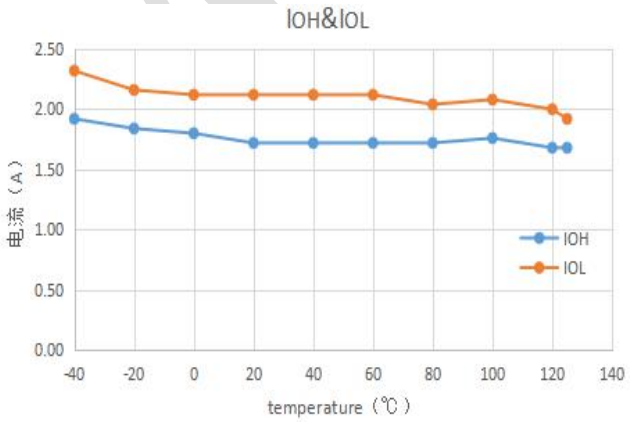


Figure 12. I_{OH}& I_{OL} vs Temperature

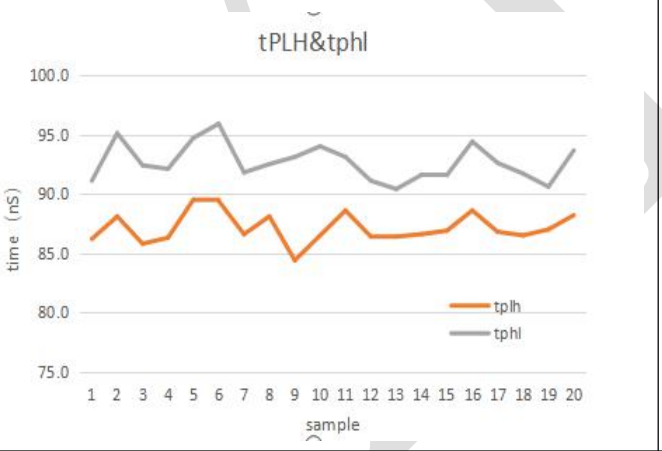


Figure 13. delay time different sample

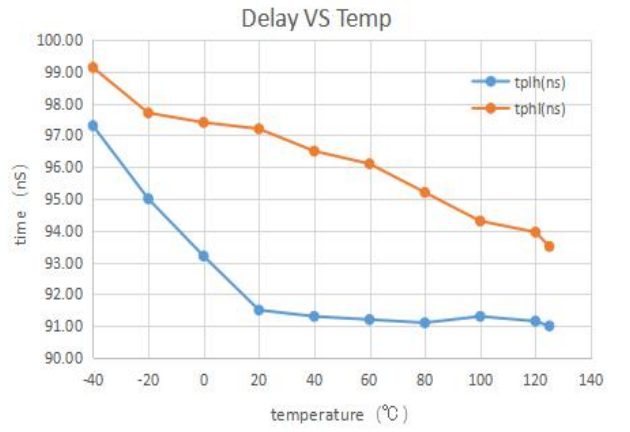


Figure 14. Delay Time vs Temperature

7 Parameter Measurement Information

7.1 Propagation Delay, Inverting, and Noninverting Configuration

Figure 15 shows the propagation delay OUT for noninverting configurations. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

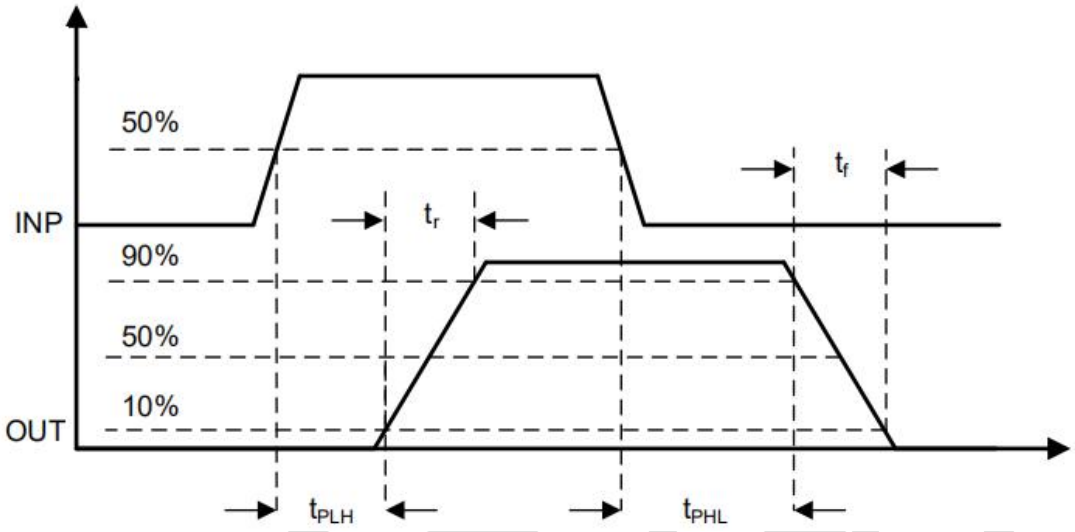


Figure 15. OUTH and OUTL Propagation Delay, Noninverting Configuration

7.2 CMTI Testing

Figure 16 are simplified diagrams of the CMTI testing configuration used for each device type.

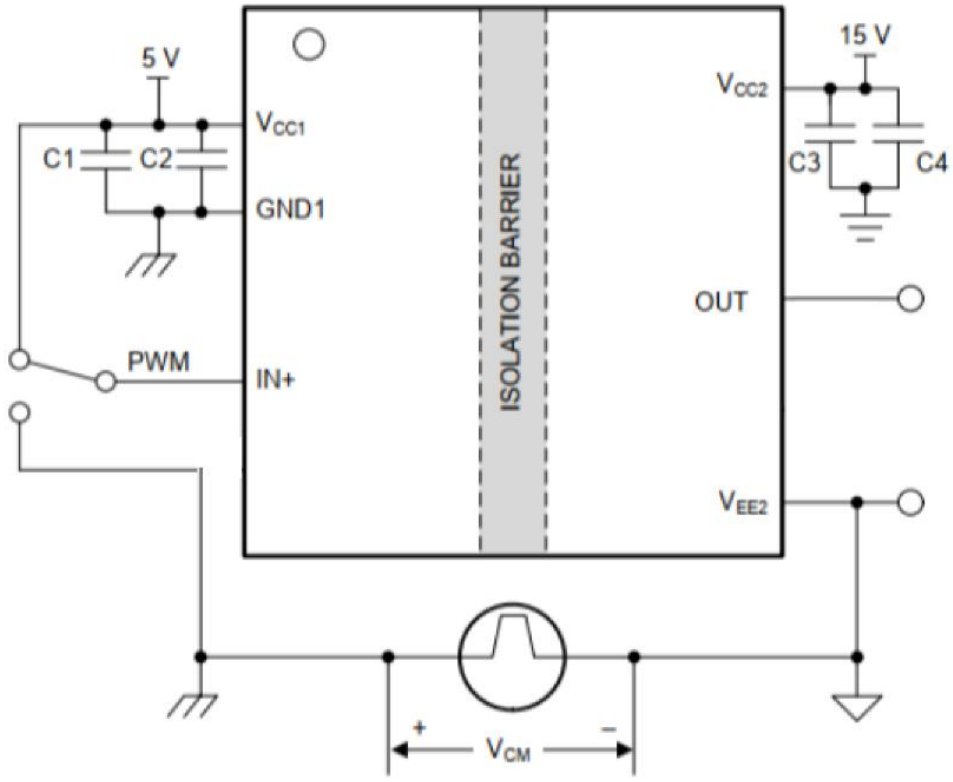


Figure 16. CMTI Test Circuit

8 Detailed Description

8.1 Feature Description

8.1.1 Power Supply

The V_{CC1} input power supply supports a wide voltage range from 3 V to 15 V and the V_{CC2} output supply supports a voltage range from 12 V to 33 V. V_{CC2} supply is connected to 15 V with respect to VEE2 for IGBTs, and 20V for SiC MOSFETs. The V_{EE2} supply is connected to 0 V.

8.1.2 Input Stage

The input pins IN+ of the XN2810 are based on CMOS-compatible input-threshold logic that is completely isolated from the V_{CC2} supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the XN2810 has a typical high threshold ($V_{IT+(IN)}$) of 0.55 × V_{CC1} and a typical low threshold of 0.45 × V_{CC1}. A wide hysteresis ($V_{hys(IN)}$) of 0.1 × V_{CC1} makes for good noise immunity and stable operation. If any of the inputs are left open, 128 kΩ of internal pulldown resistance forces the IN+ pin low.

Because the input side of the XN2810 is isolated from the output driver, the input signal amplitude can be larger or smaller than V_{CC2} provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient V_{CC2} for any gate. However, the amplitude of any signal applied to IN+ must never be at a voltage higher than V_{CC1}.

8.1.3 Output Stage

The output stages of the XN2810 feature a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P channel MOSFET and an additional pullup N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The pulldown structure in the XN2810 versions is simply composed of an N-channel MOSFET.

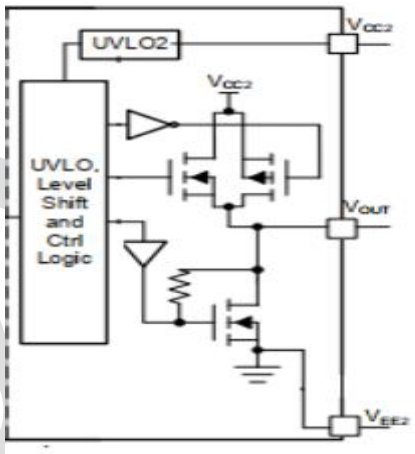


Figure 17. Output Stage

8.1.4 Protection Features

8.1.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V_{CC1} and V_{CC2} supplies between the V_{CC1} and GND1, and V_{CC2} and V_{EE2} pins to prevent an under driven condition on IGBTs and MOSFETs. When V_{CC1} is lower than $V_{IT+\ (UVLO)}$ at device start-up or lower than $V_{IT-(UVLO)}$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+) as shown in Table1 and Table 2. The V_{CC} UVLO protection has a hysteresis feature ($V_{hys(UVLO)}$). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. **Figure 18** shows the UVLO functions.

Table 1. XN2810 V_{CC1} UVLO Logic

CONDITION	INPUTS	OUTPUTS
	IN+	OUT
V_{CC1} – GND1 < $V_{IT-(UVLO1)}$ after device start-up	H	L
	L	L

Table 2. XN2810 V_{CC2} UVLO Logic

CONDITION	INPUTS	OUTPUTS
	IN+	OUT
V_{CC2} – V_{EE2} < $V_{IT+(UVLO2)}$ during device start-up	H	L
	L	L
V_{CC2} – V_{EE2} < $V_{IT-(UVLO2)}$ after device start-up	H	L
	L	L

When V_{CC1} or V_{CC2} drops below the UVLO1 or UVLO2 threshold, a delay, t_{UVLO1_rec} or t_{UVLO2_rec}, occurs on the output when the supply voltage rises above $V_{IT+(UVLO)}$ or $V_{IT+(UVLO2)}$ again. **Figure 18** shows this delay.

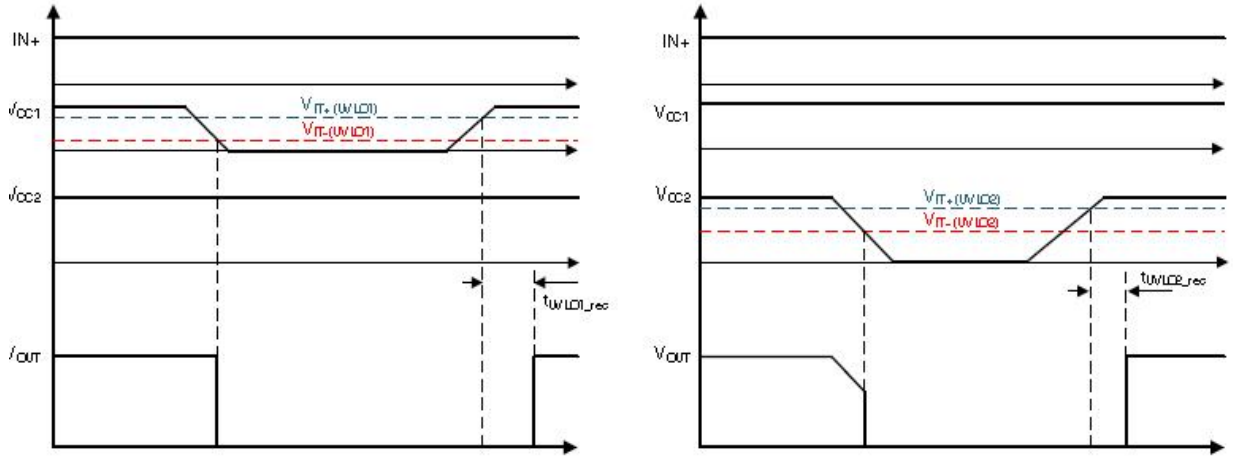


Figure 18. UVLO Functions

8.1.4.2 Active Pulldown

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the V_{CC2} supply. This feature prevents false IGBT and MOSFET turnon on the OUT pins .When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pullup resistor while the lower NMOS gate is tied to the driver output through a 500kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

8.2 Device Functional Modes

Table3 lists the functional modes for the XN2810 devices assuming V_{CC1} and V_{CC2} are in the recommended range.

Table 3. Function Table for XN2810

IN+	OUT
Low	Low
X	Low
High	High

9 Application and Implementation

Note

Information in the following applications sections is not part of the Xinergy component specification, and Xinergy does not warrant its accuracy or completeness. Xinergy's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The XN2810 is a family of simple, isolated gate drivers for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

The XN2810 devices UVLO2 with reference to VEE2. The XN2810 offer true UVLO protection by monitoring the voltage between the V_{CC2} and VEE2 pins to prevent the power transistors from operating in a saturation region. The XN2810 devices comes in an SOP6W package options and have a creepage, or clearance, of 7.5 mm respectively, which are suitable for applications where basic or reinforced isolation is required. Different drive strengths enable a simple driver platform to be used for applications demanding power transistors with different power ratings. Specifically, the XN2810 device offers a 2.5A minimum drive current which can help remove the external current buffer used to drive high power transistors.

9.2 Typical Application

The circuits in **Figure 19** show a typical application for driving IGBTs

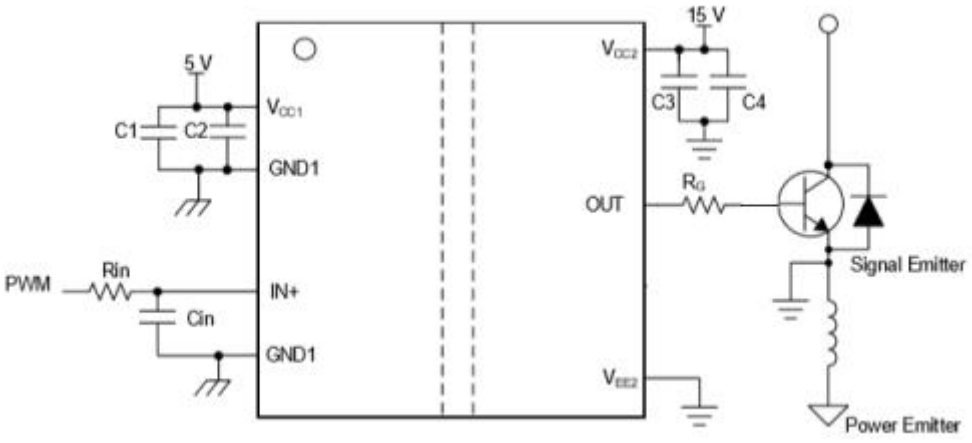


Figure 19. Typical Application Circuit for XN2810 to Drive IGBT

9.2.1 Selecting V_{CC1} and V_{CC2} Capacitors

Bypass capacitors for the V_{CC1} and V_{CC2} supplies are essential for achieving reliable performance. Xinergy recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

Note

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

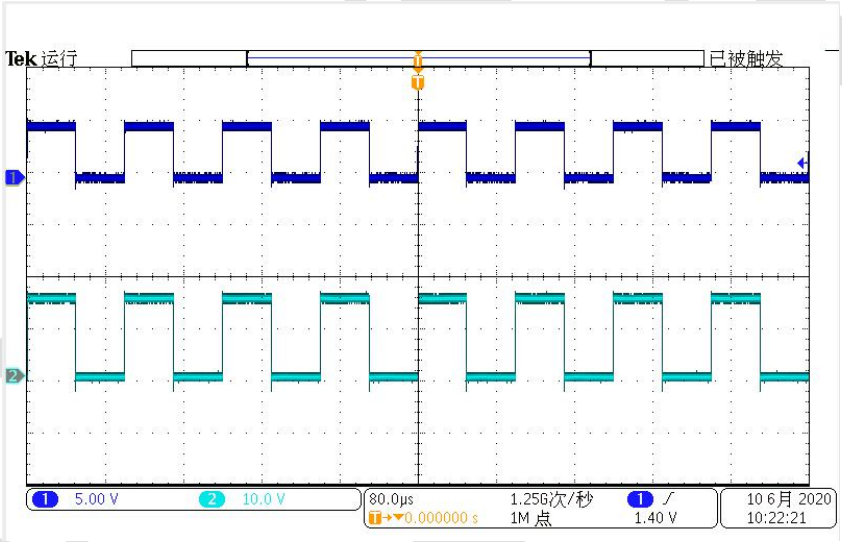
9.2.1.1 Selecting a V_{CC1} Capacitor

A bypass capacitor connected to the V_{CC1} pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V_{CC1} pin, a tantalum or electrolytic capacitor with a value greater than 1µF should be placed in parallel with the MLCC.

9.2.1.2 Selecting a V_{CC2} Capacitor

A 50V, 10µF MLCC and a 50V, 0.22µF MLCC are selected for the C_{VCC2} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC2} pin, a tantalum or electrolytic capacitor with a value greater than 10µF should be used in parallel with C_{VCC2}.

9.2.2 Application Curve



V_{CC1} = 5 V V_{CC2} = 15 V f_{SW} = 15 kHz

Figure 20. PWM Input And Gate Voltage Waveform

10 Power Supply Recommendations

The recommended input supply voltage (V_{CC1}) for the XN2810 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage (V_{CC2}) is determined by the internal UVLO protection feature of the device. The V_{CC1} and V_{CC2} voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 60 µs by the UVLO protection feature. For more information on UVLO, see the *Undervoltage Lockout (UVLO)* section. The higher limit of the V_{CC2} range depends on the maximum gate voltage of the power device that is driven by the XN2810 device, and should not exceed the recommended maximum V_{CC2} of 33 V. A local bypass capacitor should be placed between the V_{CC2} and V_{EE2} pins, with a value of 220nF to 10µF for device biasing. Xinergy recommends placing an additional 100nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the V_{CC1} and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the XN2810 device, this bypass capacitor has a minimum recommended value of 100 nF.

11 Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the XN2810. Some key guidelines are:

• Component placement:

Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CC1} and GND1pins and between the V_{CC2} and V_{EE2} pins to bypass noise and to support high peak currents when turning on the external power transistor.To avoid large negative transients on the VEE2 pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

• Grounding considerations:

Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

• High-voltage considerations:

To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

• Thermal considerations:

A large amount of power may be dissipated by the XN2810 if the driving voltage is high, the load is heavy, or the switching frequency is high . Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to board thermal impedance (θJB).Increasing the PCB copper connecting to the VCC2 and VEE2 pins is recommended, with priority on maximizing the connection to VEE2. However, the previously mentioned high-voltage PCB considerations must be maintained. If the system has multiple layers, Xinergy also recommends connecting the VCC2 and VEE2 pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

12 package

Unit: mm