

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology
- ★ 100% EAS Guaranteed

Product Summary

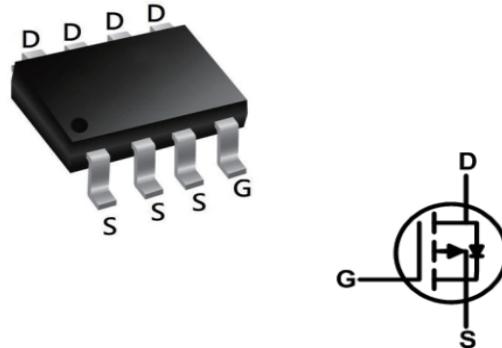
RoHS

BVDSS	RDSON	ID
-40V	14mΩ	-13A

Description

The 4485 is the high cell density trenched P-ch MOSFETs, which provides excellent RDSON and efficiency for most of the small power switching and load switch applications. The 4485 meets the RoHS and Green Product requirement 100% EAS Guaranteed with full function reliability approved.

SOP8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$TC = 25^\circ C$	A
		$TC = 100^\circ C$	A
I_{DM}	Pulsed Drain Current ^{note1}	-52	A
EAS	Single Pulsed Avalanche Energy ^{note2}	80	mJ
P_D	Power Dissipation $TC = 25^\circ C$	3	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C

Thermal Data

Symbol	Parameter	Max.	Units
$R_{\theta JA}$	Thermal Resistance from Junction-to-Ambient ³	1.9	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
Static Characteristics							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-40	-	-	V	
I_{GSS}	Gate-body Leakage current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$	-	-	-1	μA
		$T_J = 100^\circ\text{C}$				-100	
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1	-1.5	-2.2	V	
$R_{DS(on)}$	Drain-Source On-Resistance ⁴	$V_{GS} = -10\text{V}, I_D = -10\text{A}$	-	14	19	$\text{m}\Omega$	
		$V_{GS} = -4.5\text{V}, I_D = -5\text{ A}$	-	19.5	25		
g_{fs}	Forward Transconductance ⁴	$V_{DS} = -10\text{V}, I_D = -10\text{A}$	-	44	-	S	
Dynamic Characteristics ⁵							
C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	2525	-	pF	
C_{oss}	Output Capacitance		-	190	-		
C_{rss}	Reverse Transfer Capacitance		-	172	-		
R_g	Gate Resistance	$f = 1\text{MHz}$	-	10	-	Ω	
Switching Characteristics ⁵							
Q_g	Total Gate Charge	$V_{GS} = -10\text{V}, V_{DS} = -20\text{V}, I_D = -10\text{A}$	-	35	-	nC	
Q_{gs}	Gate-Source Charge		-	5.5	-		
Q_{gd}	Gate-Drain Charge		-	8	-		
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = -10\text{V}, V_{DD} = -20\text{V}, R_G = 3\Omega, I_D = -10\text{A}$	-	14.5	-	ns	
t_r	Rise Time		-	20.2	-		
$t_{d(off)}$	Turn-Off Delay Time		-	32	-		
t_f	Fall Time		-	10	-		
Drain-Source Body Diode Characteristics							
V_{SD}	Diode Forward Voltage ⁴	$I_S = -10\text{A}, V_{GS} = 0\text{V}$	-	-	-1.2	V	
I_S	Continuous Source Current	$T_c = 25^\circ\text{C}$	-	-	-13	A	

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25\text{V}, V_{GS} = -10\text{V}, L = 0.1\text{mH}, I_{AS} = -34\text{A}$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

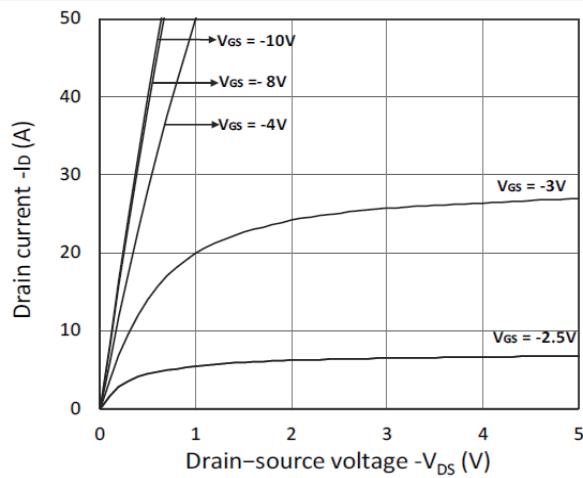


Figure 2: Typical Transfer Characteristics

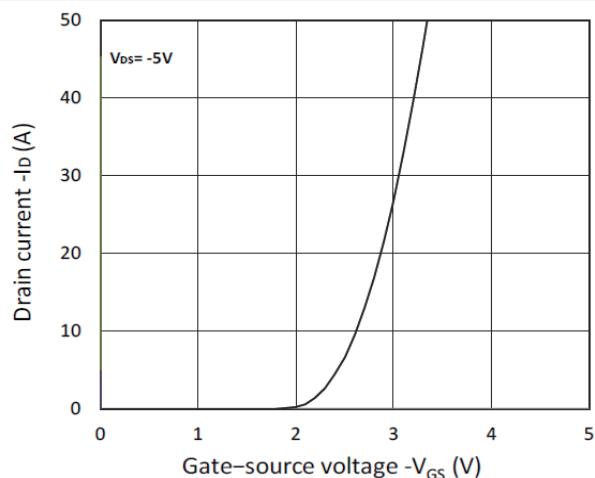


Figure 3: Forward Characteristics of Reverse

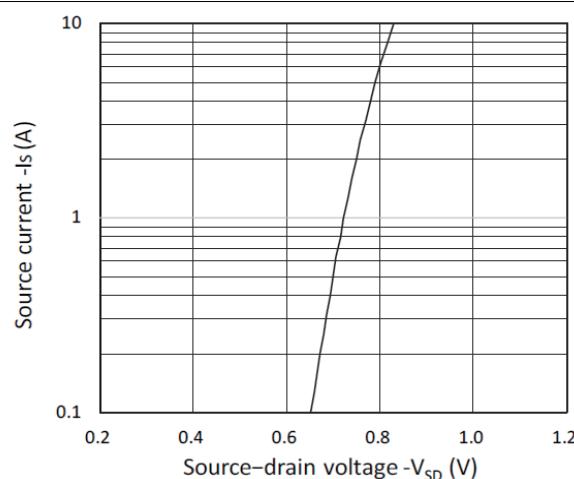


Figure 4: RDS(ON) vs. VGS

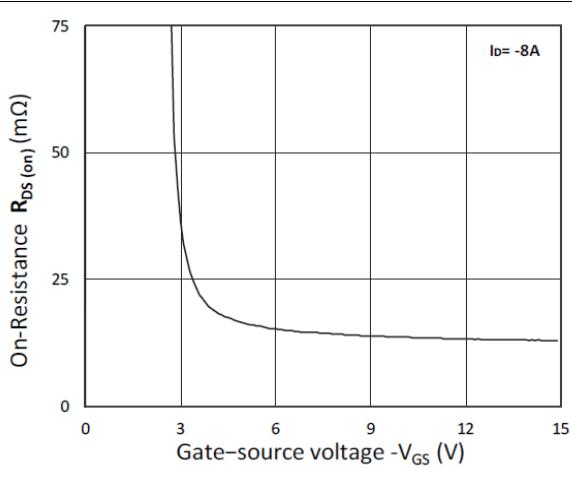


Figure 5: RDS(ON) vs. ID

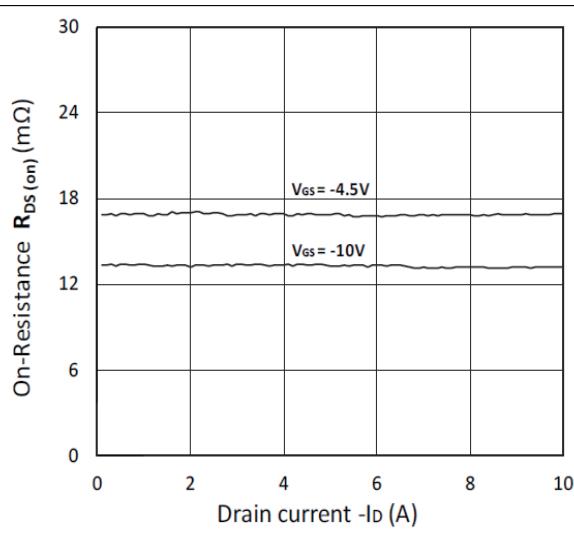
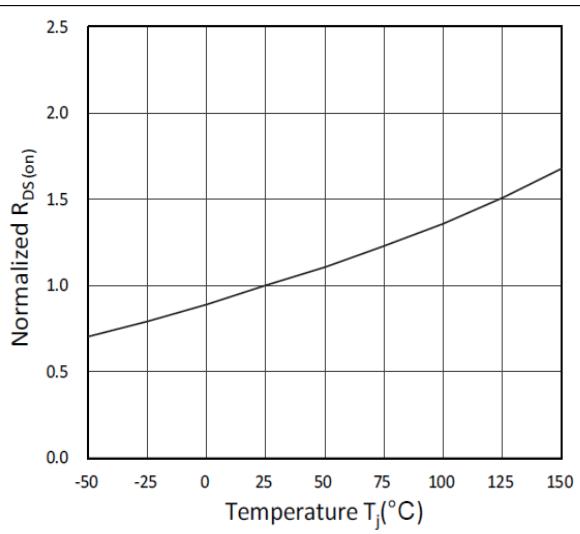


Figure 6: Normalized RDS(on) vs. Temperature



Typical Performance Characteristics

Figure 7: Capacitance Characteristics

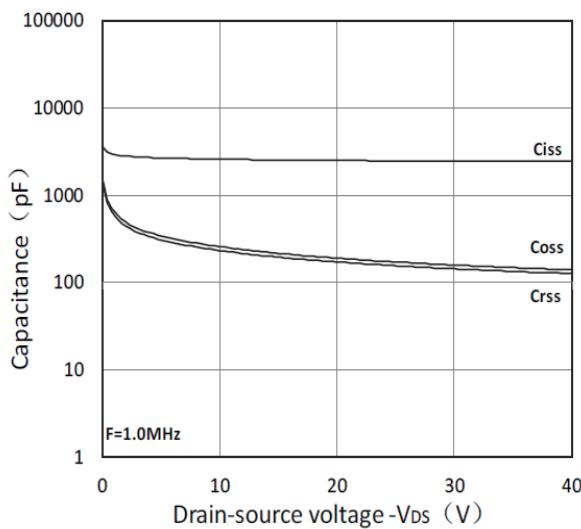


Figure 8: Gate Charge Characteristics

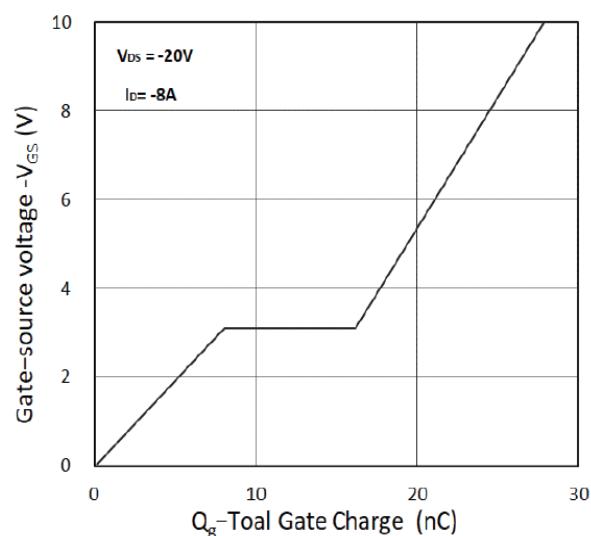


Figure 9: Power Dissipation

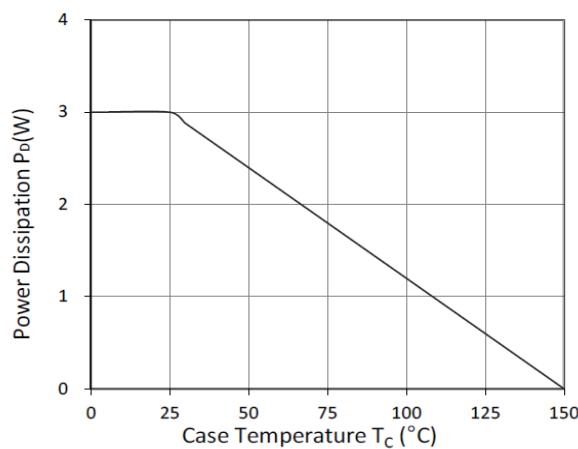


Figure 10: Safe Operating Area

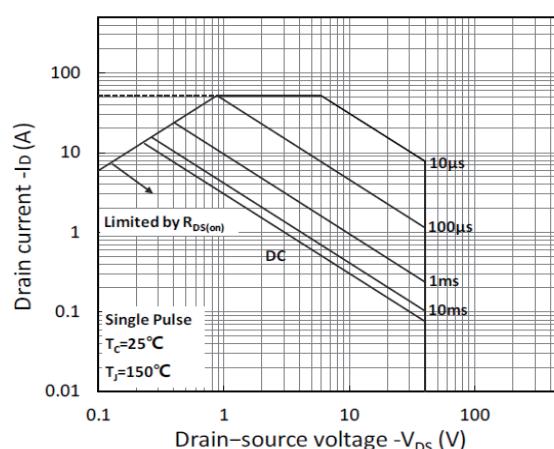
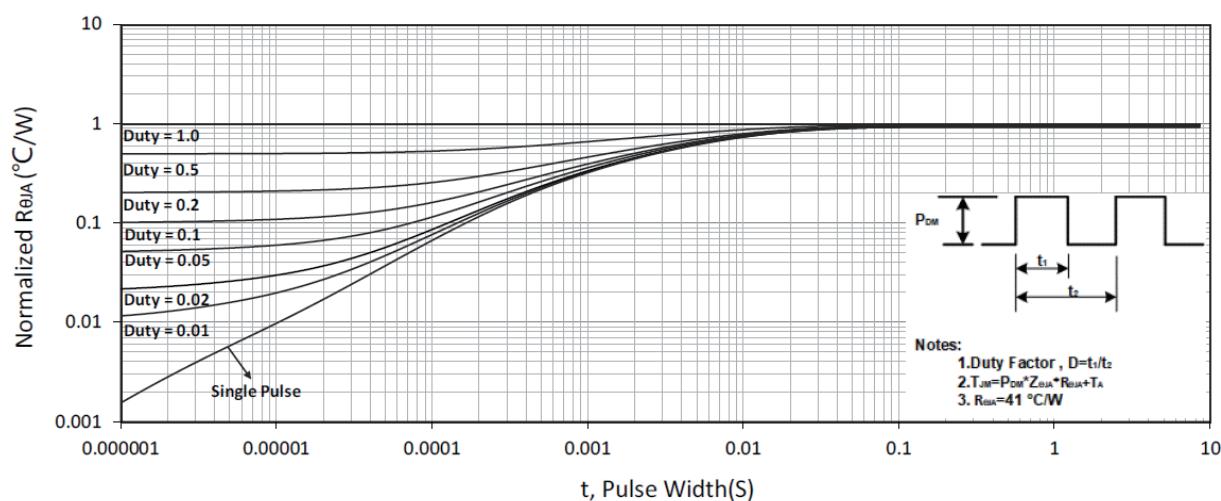
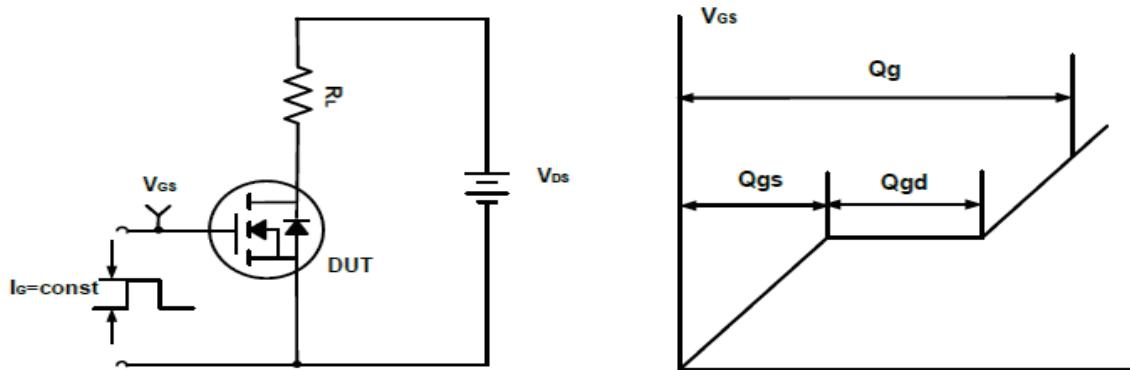
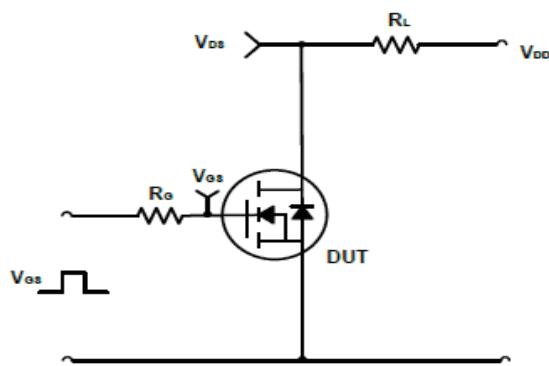
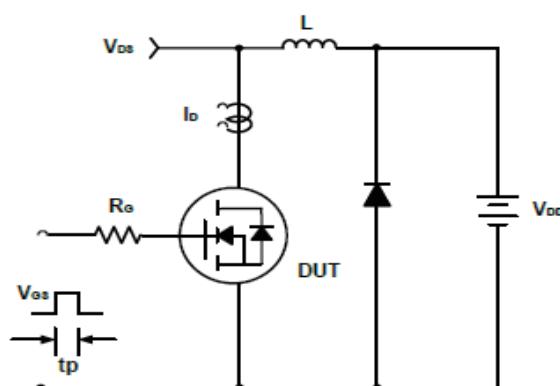
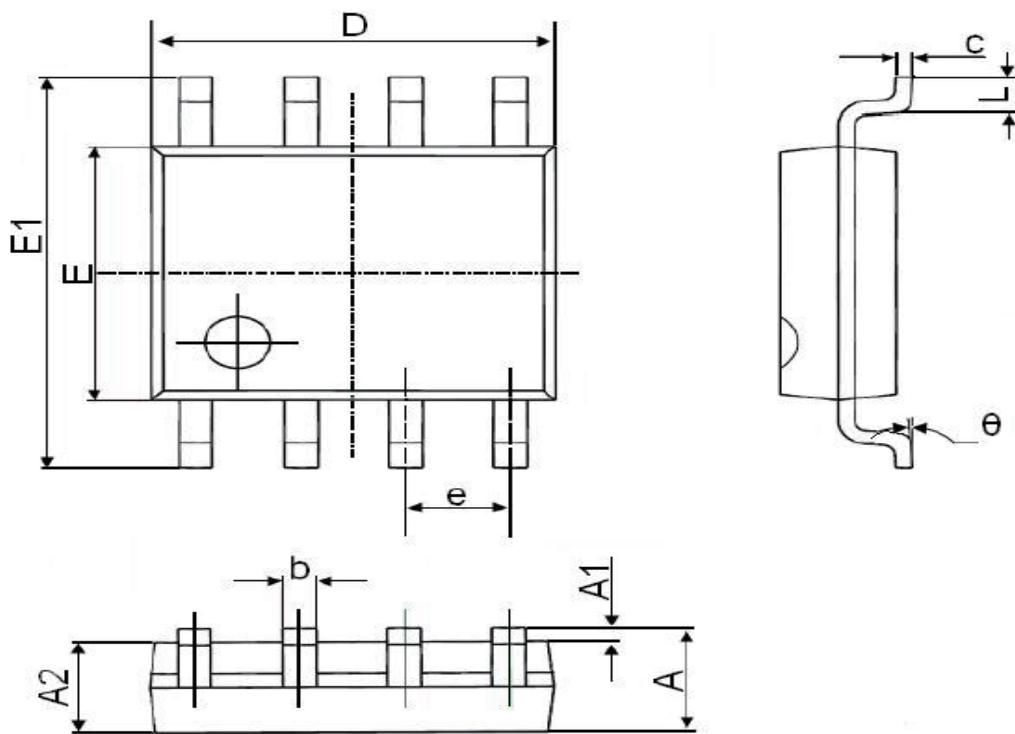


Figure 11: Normalized Maximum Transient Thermal Resistance



Test Circuit

Figure A. Gate Charge Test Circuit & Waveforms

Figure B. Switching Test Circuit & Waveforms

Figure C. Unclamped Inductive Switching Circuit & Waveforms

SOP-8 Package Information



DIMENSIONS (unit : mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.1	0.25	0.004	0.01
A2	1.35	1.55	0.053	0.061
b	0.33	0.51	0.013	0.02
c	0.17	0.25	0.006	0.01
D	4.7	5.1	0.185	0.2
E	3.8	4	0.15	0.157
E1	5.8	6.2	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.4	1.27	0.016	0.05
θ	0°	8°	0°	8°