

N-Channel MOSFET

Lead Free Package and Finish

Applications:

- Adaptor
- Charger
- SMPS

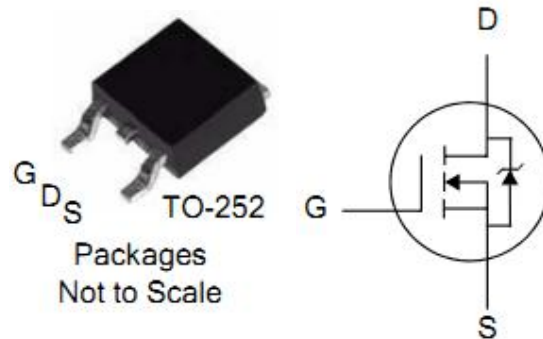
V_{DSS}	$R_{DS(ON)}(Typ.)$	I_D
100V	113m Ω	14A

Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
FTD150N10N	TO-252	IPS



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	FTD150N10N	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	14	A
	Continuous Drain Current $T_C = 100^\circ\text{C}$	8.2	A
I_{DM}	Pulsed Drain Current (NOTE *1)	56	A
P_D	Power Dissipation	43.1	W
	Derating Factor above 25°C	0.34	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	28.8	mJ
I_{AS}	Avalanche Current	7.6	A
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150, -55 to 150	

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	2.9	$^\circ\text{C}/\text{W}$	Water cooled heatsink, P_D adjusted for a peak junction temperature of $+150^\circ\text{C}$.
$R_{\theta JA}$	Junction-to-Ambient	100		1 cubic foot chamber, free air.



FTD150N10N

OFF Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=100V, V_{GS}=0V$ $T_J=25^\circ\text{C}$
		--	--	100		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	$V_{GS}=+20V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-20V$

ON Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	113	150	m Ω	$V_{GS}=10V, I_D=4A$
		--	135	190	m Ω	$V_{GS}=4.5V, I_D=3A$
$V_{GS(TH)}$	Gate Threshold Voltage	1.8	2.4	2.9	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_g	Gate resistance	--	3.4	--	Ω	$V_{GS}=0V, V_{DS}=0V$ $f=1.0\text{MHz}$
C_{iss}	Input Capacitance	--	557	--	μF	$V_{GS}=0V, V_{DS}=25V$ $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	--	34.7	--		
C_{rss}	Reverse Transfer Capacitance	--	18.7	--		
$Q_g(4.5V)$	Total Gate Charge	--	5.8	--	nC	$I_D=4A, V_{DD}=50V$
$Q_g(10V)$	Total Gate Charge	--	11.5	--		
Q_{gs}	Gate-to-Source Charge	--	2.2	--		
Q_{gd}	Gate-to-Drain ("Miller") Charge	--	2.6	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	8.5	--	ns	$V_{DD}=50V, I_D=4A,$ $V_{GS}=10V, R_G=3\Omega$
t_{rise}	Rise Time	--	6.3	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	29.2	--		
t_{fall}	Fall Time	--	3.2	--		



FTD150N10N

Source-Drain Diode Characteristics $T_c=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	14	A	$T_C=25^\circ\text{C}$
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	56	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_{SD}=4\text{A}, V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	--	59.2	--	ns	$I_F=I_S$ $di/dt=100\text{A/us}$
Q_{rr}	Reverse Recovery Charge	--	108	--	nC	
Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$						

Notes:

- *1. Repetitive rating; pulse width limited by maximum junction temperature.
- *2. $L=1\text{mH}$, $I_D=7.6\text{A}$, Start $T_J=25^\circ\text{C}$
- *3. $di/dt \leq 100\text{A/us}$, $V_{DD} \leq BV_{DS}$, Start $T_J=25^\circ\text{C}$

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

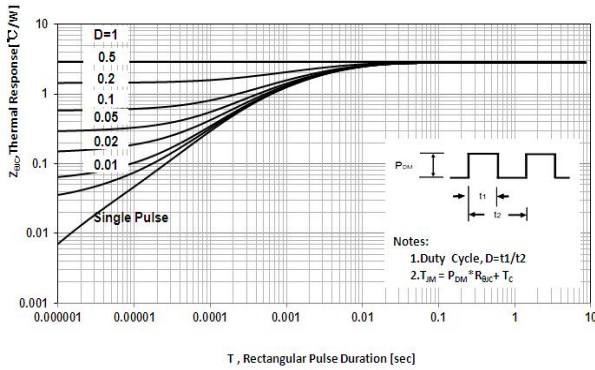


Figure 4. Typical Output Characteristics

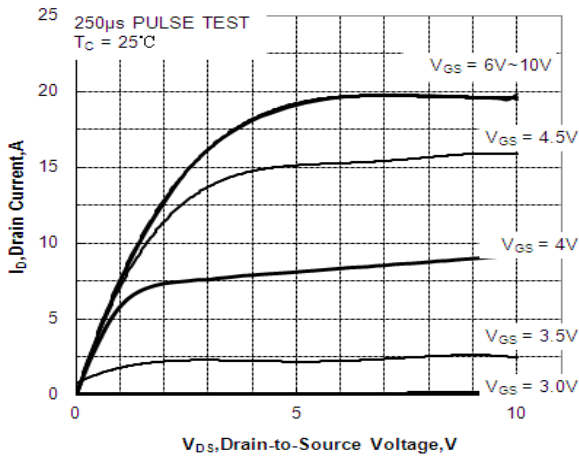


Figure 6. Typical Body Diode Transfer Characteristics

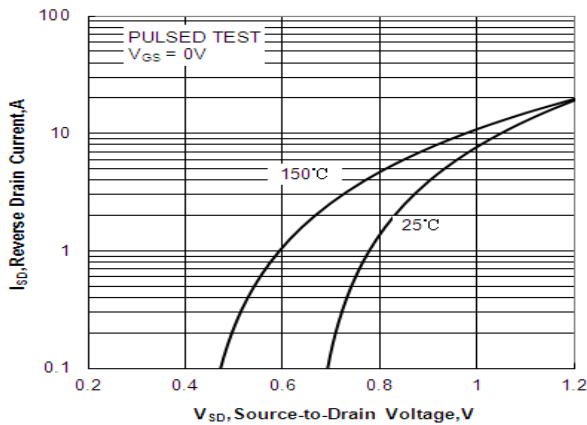


Figure 2 Typical Threshold Voltage vs Junction Temperature

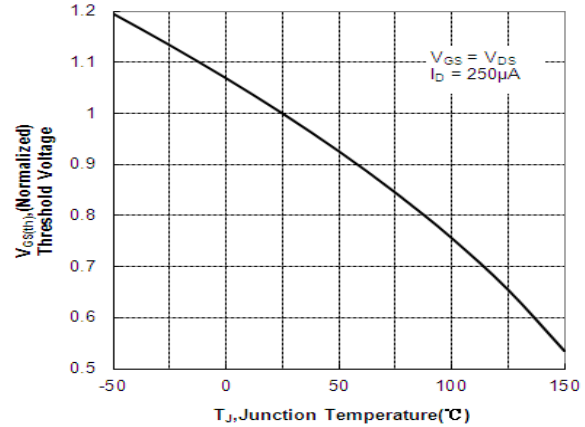


Figure 5. Typical Transfer Characteristics

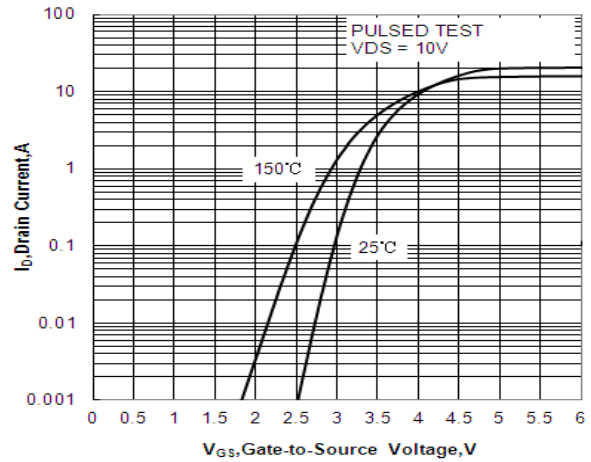


Figure 7. Typical on Resistance VS Drain Current

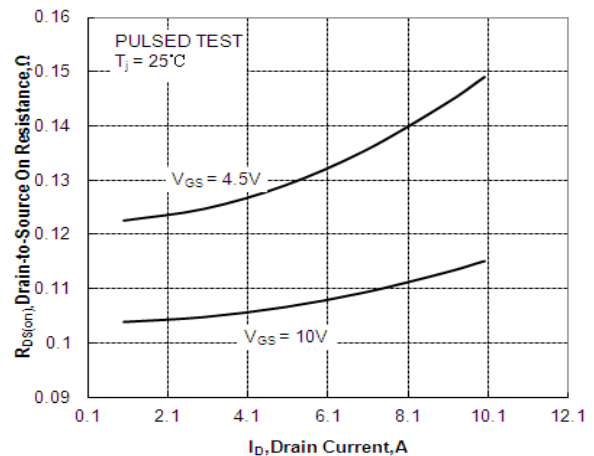


Figure 8. Capacitance VS Drain-to-Source Voltage

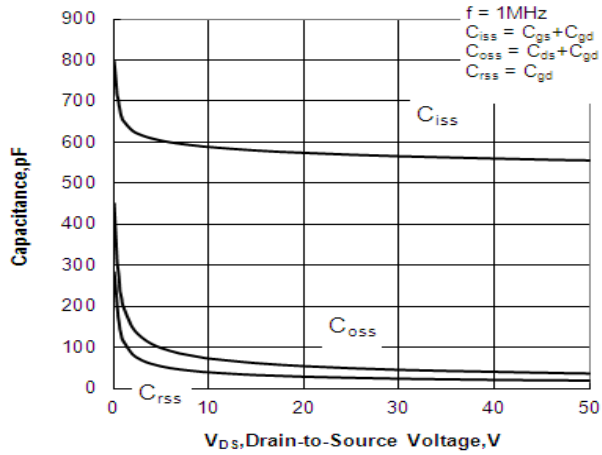


Figure 9. Gate Charge VS Gate-to-Source Voltage

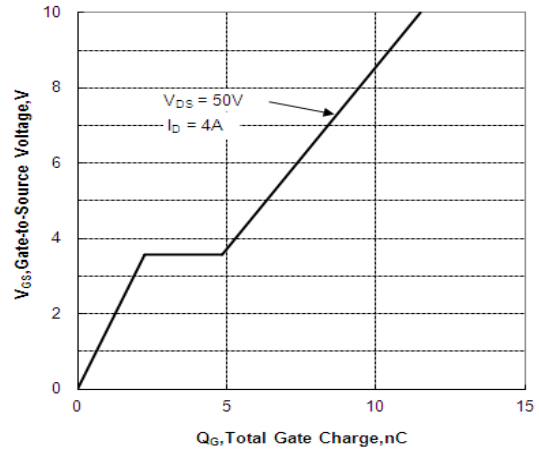


Figure 10. Breakdown Voltage VS Temperature

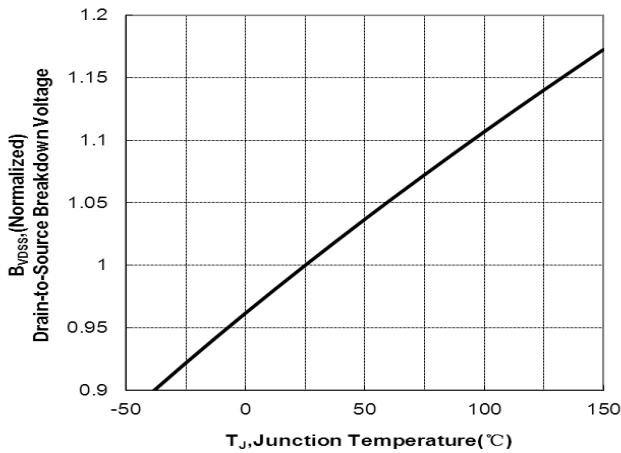


Figure 11. on-Resistance VS Temperature

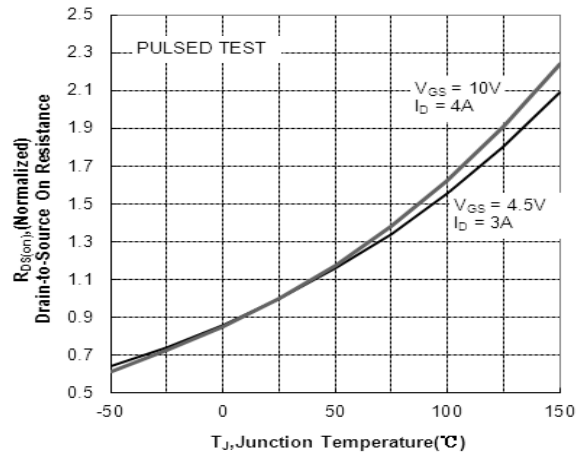


Figure 12. Resistance vs Gate-to-Source Voltage

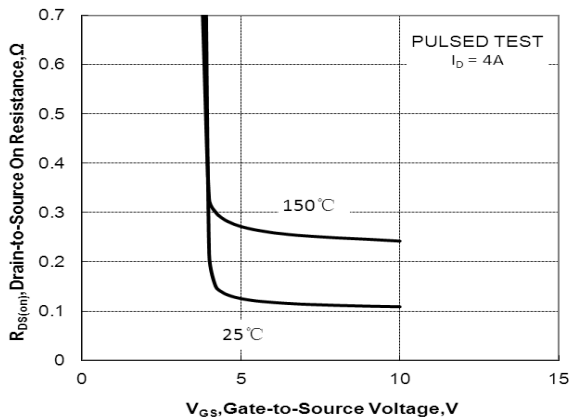
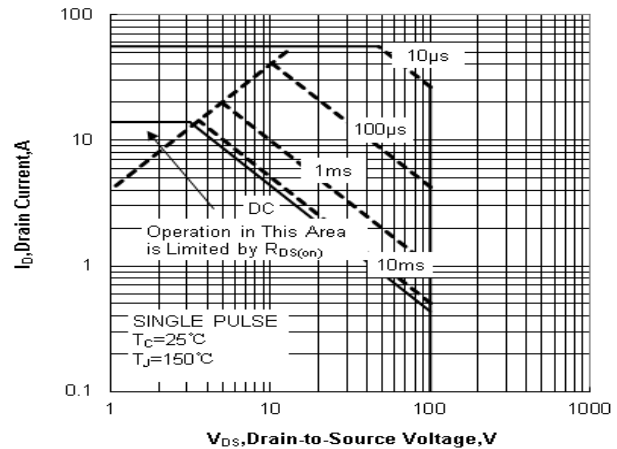


Figure 13. Safe Operating Area



Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit

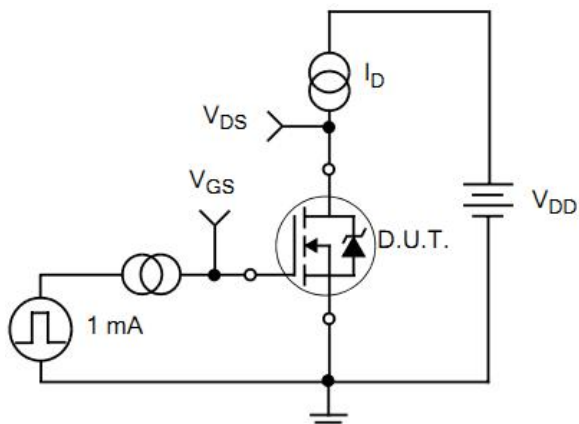


Figure 15. Gate Charge Waveforms

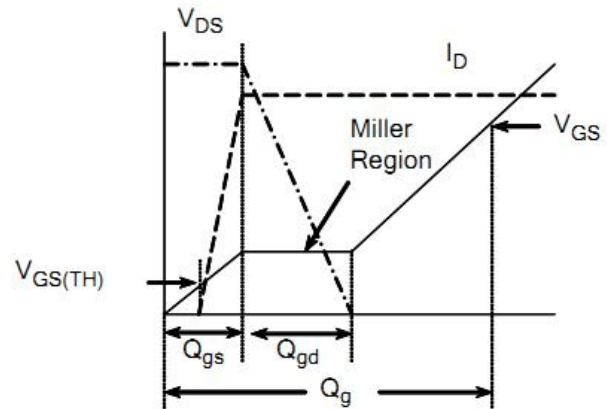


Figure 16. Resistive Switching Test Circuit

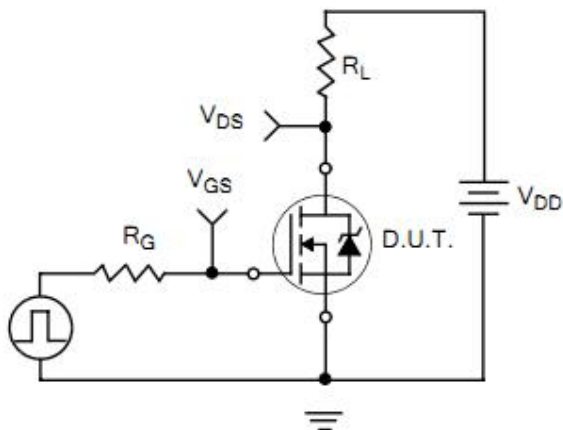


Figure 17. Resistive Switching Waveforms

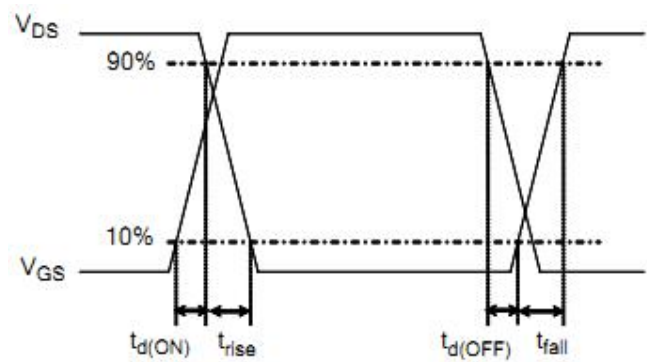


Figure 18. Diode Reverse Recovery Test Circuit

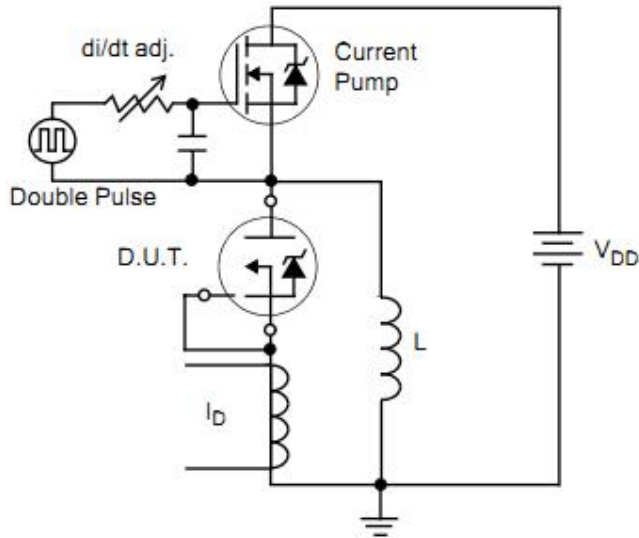


Figure 19. Diode Reverse Recovery Waveform

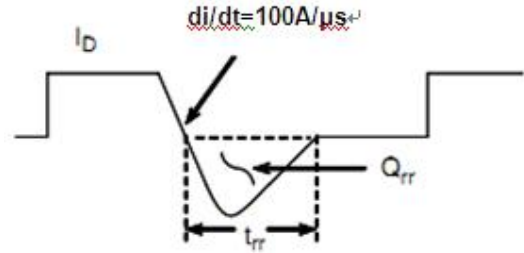


Figure 20. Unclamped Inductive Switching Test Circuit

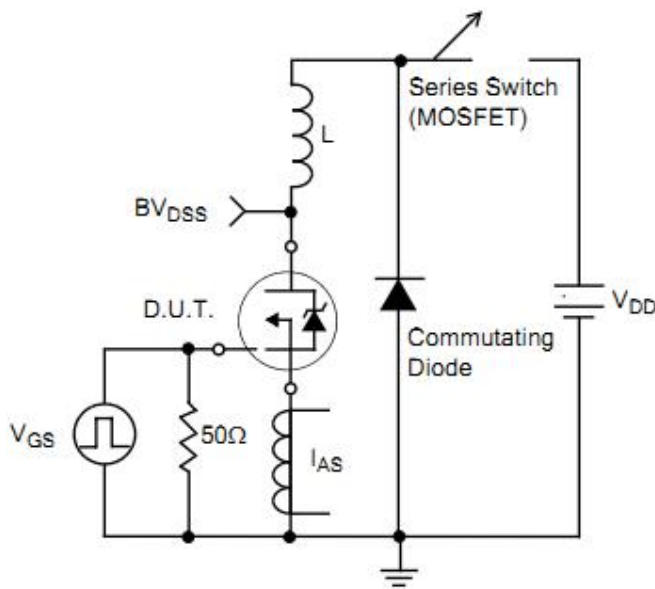
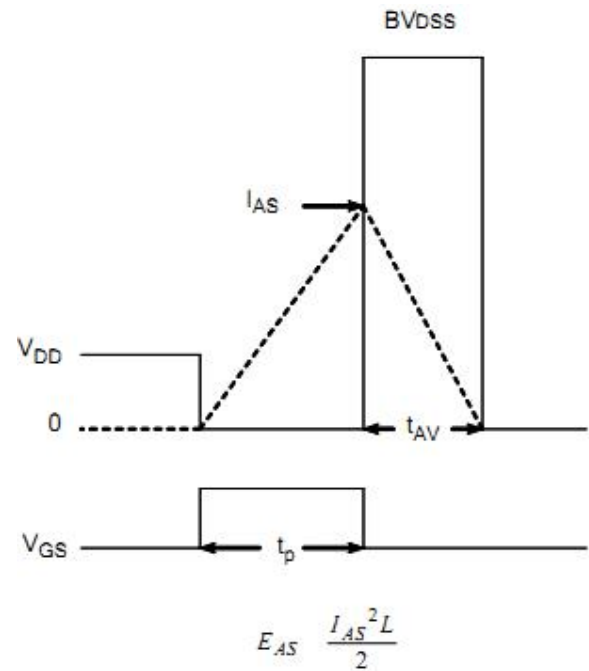


Figure 21. Unclamped Inductive Switching Waveform





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