One out of two analog switch circuit

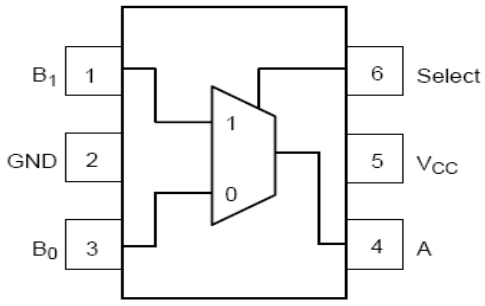
summary

SN74LVC1G3157 is an analog switch based on CMOS technology.It has low power consumption, low transmission delay and low output impedance.The voltage output range of analog signal and digital signal can be from V_{cc} or GND.The select input terminal has over-voltage protection, which allows the input voltage to be higher than V_{cc}, up to 7V, and the pin will not be burned.

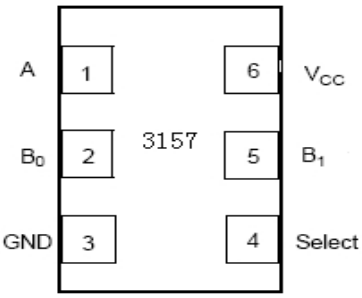
Functional features

- low power consumption
- High transmission speed
- Flip standard CMOS logic level
- High bandwidth, high linearity
- Switch for NTSC / PAL video, audio, SPDIF and HDTV
- It can be used for clock switch and data selection switch
- Low output impedance
- First break and then open protection to prevent short circuit
- Working temperature - 55 ˚C ~ + 125 ˚C
- Package form SC70-6 (3157DCKR), DFN6 (SN74LVC1G3157Y)，SOT23-6(SN74LVC1G3157DBVR)

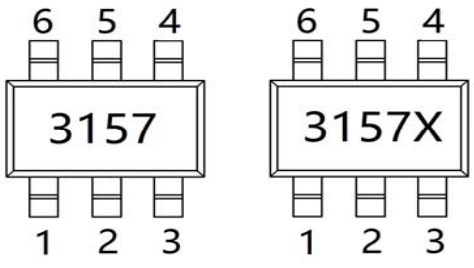
Pin layout



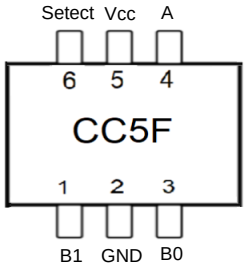
SC70-6



DFN6



SC70-6 Marking



SOT23-6

planform

Pin description

Pin	I/O	function
A, B_0, B_1	I/O	Data port
Select	I	Control selection
V_{CC}	—	Power supply terminal
GND	—	land

Function description

Select input	function
L	B_0 to A
H	B_1 to A

Thermal resistance data

parameter	Symbol	numerical value	Company
thermal resistance	θ_{JA}	270	°C/W

Limit parameter

parameter	Symbol	Range	Company
supply voltage	V_{CC}	−0.5～+7.0	V
Switching voltage (Note 1)	V_S	−0.5～V_{CC}+0.5	V
Input voltage (Note 1)	V_{IN}	−0.5～+7.0	V
Vin @ 0V input current clamp diode	I_{IK}	−50	mA
Output current	Iout	128	mA
Power to ground current	Icc/I_{GND}	100	mA
Storage temperature range	Tstg	−65～+150	℃
Maximum junction temperature	T_J	150	℃
Wire temperature (welding, 10 seconds)	T_L	260	℃
Total power consumption (85 ∪)	P_D	180	mw

Exceeding the maximum value of DC limit parameters may cause irreparable damage to the circuit.If there is no special case, ensure that the power supply voltage, operating temperature and load characteristics of input / output of the whole working system are within the above range.

Note 1: the negative voltage of I / O can be exceeded according to the clamping diode current range of input / output.

Working environment (Note 2)

parameter	Symbol	MID	MXA	Company
supply voltage	V_{CC}	1.65	5.5	V
Select terminal input voltage	V_{IN}	0	V_{CC}	V
Switch input voltage	V_{IN}	0	V_{CC}	V
Output voltage	V_{OUT}	0	V_{CC}	V
Working temperature	T_A	-55	+125	
Enter the rising and falling time. Input voltage VCC = 2.3V 3.6V. Input voltage VCC = 4.5V－5.5V.	t_r,t_f	 0 0	 10 5.0	ns/V

Note: The input voltage of 2:Select terminal must be set to a high level or a low level, and cannot be left floating.

Electrical parameter

parameter	sign	test condition	V_{CC}	T_A=25℃			T_A=-40℃～+85℃		Company
				mid	standard	max	min	max	
DC characteristic									
V_{IH}	High level input		1.65-1.95				0.75Vcc		V
			2.3-2.8				1.5		
			3-4.2				2.4		
			4.5-5.5				0.6Vcc		
V_{IL}	Input low level		1.65-1.95					0.25Vcc	V
			2.3-2.8					0.4	
			3-5.5					0.3Vcc	
I_{IN}	Leakage current input	0< V_{IN}<5.5V	0-5.5		± 0.05	± 0.1		± 1	uA
I_{OFF}	Closed state leakage electric current	0<A,B< Vcc	1.65-5.5		± 0.05	± 0.1		± 1	uA
I_{CC}	Quiescent current	V_{IN} =Vcc or GND I_{OUT} =0	5.5			1.0		10	uA
	Analog level input Into the scope		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{ON}	Switch on resistance (Note 3)	V_{IN}=0V, I_O=30mA	4.5		3.0			7.0	Ω
		V_{IN}=2.4V, I_O=-30mA			5.0			12	Ω
		V_{IN}=4.5V, I_O=-30mA			7.0			15	Ω
		V_{IN}=0V, I_O=24mA	3.0		4.0			9.0	Ω
		V_{IN}=3V , I_O=-24mA			10			20	Ω
		V_{IN}=0V, I_O=8mA	2.3		5.0			12	Ω
		V_{IN}=2.3V, I_O=-8mA			13			30	Ω
		V_{IN}=0V, I_O=4mA	1.65		6.5			20	Ω
		V_{IN}=1.65V, I_O=-4mA			17			50	Ω
R_{RANGE}	Full signal range on resistance (Note 3 () Note 7)	I_A=-30mA 0≤ V_{Bn}≤ V_{CC}	4.5					25	Ω
		I_A=-24mA 0≤ V_{Bn}≤ V_{CC}	3					50	Ω
		I_A=-8mA 0≤ V_{Bn}≤ V_{CC}	2.3					100	Ω
		I_A=-4mA 0≤ V_{Bn}≤ V_{CC}	1.65					300	Ω

ΔR_{ON}	On resistance matching between channels (Note 3) (Note 4) (Note 5)	I_A=-30mA V_{Bn}= 3.15	4.5		0.15				Ω
		I_A=-24mA V_{Bn}= 2.1	3		0.2				Ω
		I_A=-8mA V_{Bn}= 1.6	2.3		0.5				Ω
		I_A=-4mA V_{Bn}= 1.15	1.65		0.5				Ω
R_{FLAT}	On-resistance flatness (Note 3) (Note 4) (Note 6)	I_A=-30mA 0≤ V_{Bn}≤ V_{CC}	5		6.0				Ω
		I_A=-24mA 0≤ V_{Bn}≤ V_{CC}	3.3		12				Ω
		I_A=-8mA 0≤ V_{Bn}≤ V_{CC}	2.5		28				Ω
		I_A=-4mA 0≤ V_{Bn}≤ V_{CC}	1.8		125				Ω
AC characteristics									
t_{PHL} t_{PLH}	Transmission Delay (Note 8)	Fig. 1 V_I=OPEN	1.65-1.95						nS
			2.3-2.7					1.2	nS
			3.0-3.5					0.8	nS
			4.5-5.5					0.3	nS
t_{PZL} t_{PZH}	Open time (a to Bn)	Fig. 1 v_I= 2*v_{CC} for t_{PZL}, v_I= 0v for tpzh	1.65-1.95			23	7.0	24	nS
			2.3-2.7			13	3.5	14	nS
			3.0-3.5			6.9	2.5	7.6	nS
			4.5-5.5			5.2	1.7	5.7	nS
t_{PLZ} t_{PHZ}	turn - off time (port a to port b)	Fig. 1 v_I= 2*v_{CC} for t_{PLZ}, v_I= 0v for tpzh	1.65-1.95			12.5	3.0	13	nS
			2.3-2.7			7.0	2.0	7.5	nS
			3.0-3.5			5.0	1.5	5.3	nS
			4.5-5.5			3.5	0.8	3.8	nS
t_{B-M}	Break before connect time (Note 7)	Fig. 2, C_L=50pF, R_L=600Ω	1.65-1.95				0.5		nS
			2.3-2.7				0.5		nS
			3.0-3.5				0.5		nS
			4.5-5.5				0.5		nS
Q	Charge injection (Note 7)	Fig. 3, C_L=0.1nF, V_{GEN}= 0V R_{GEN}=0Ω	5.0		7.0				pC
			3.3		3.0				pC
OIRR	Close (note 9) Release	Fig. 4, R_L = 50Ω , f = 10MHz	1.65-5.5		-57				dB
Xtalk	cross talk	Fig. 5, R_L= 50Ω , f =	1.65-5.5		-54				dB

		10MHz							
BW	-3dB bandwidth	Fig. 8, R_L = 50 Ω	1.65-5.5		350M				Hz
THD	total harmonic distortion (Note 7)	R_L=600Ω，0.5V_{P-P} f=600Hz—20kHz	5.0		0.011				%
C_{IN}	Input terminal capacitance (Note 10)		0		2.3				pF
C_{IO-B}	B disconnection capacitance when the port is turned off (Note 10)	Figure 6	5.0		5.0				pF
C_{IOA-ON}	A conduction capacitance when the port is open (Note 10)	Figure 7	5.0		15.5				pF

Note3: It is obtained by measuring the ratio of the voltage difference between the two ports A and B to the current flowing through the two ports. On-resistance is determined by the lower voltage port of port A and B

Note4: The load characteristics introduced by encapsulation are not included.

Note5: **ΔRON = RON max- RON min in the given VCC, temperature and level range.**

Note6: On-resistance flatness refers to the difference between the maximum value and the minimum value of on-resistance under specified conditions.

Note 7: Design simulation value.

Note 8: This parameter is the design simulation value rather than the measured value. In the case of an ideal voltage source (zero output load), the transmission delay will be better than that of a 50pF load capacitor.

Note 9: Turn off isolation =20log10[VA/VBn].

Note 10:TA=+25℃,f=1MHz, excluding the load capacitance introduced by packaging.

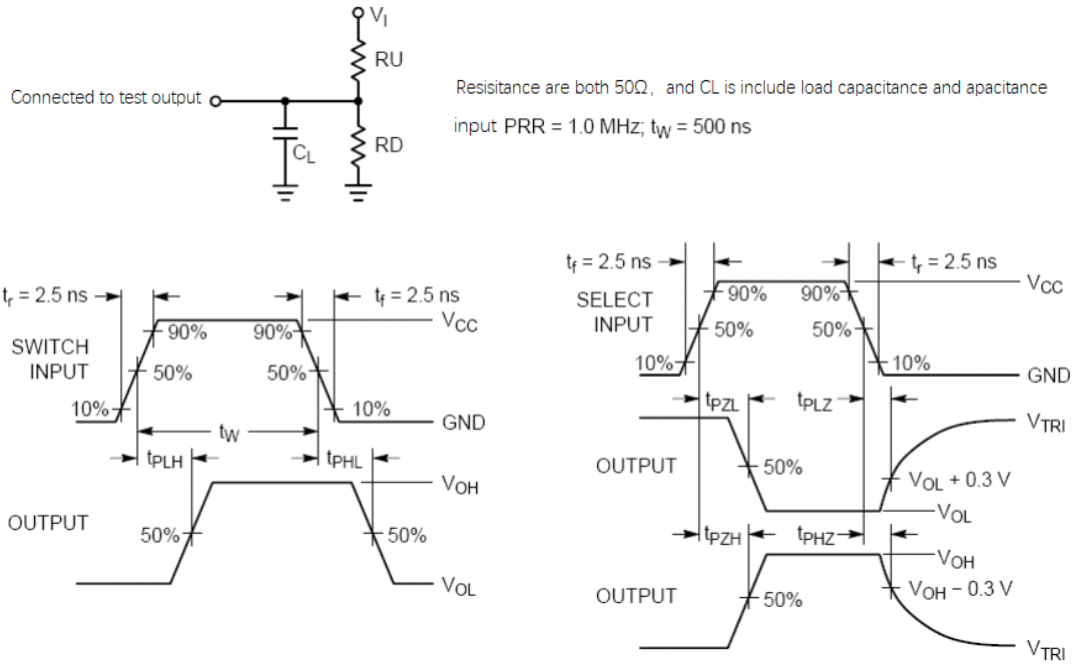


Figure 1 Transmission delay,

Figure 2: Break first and

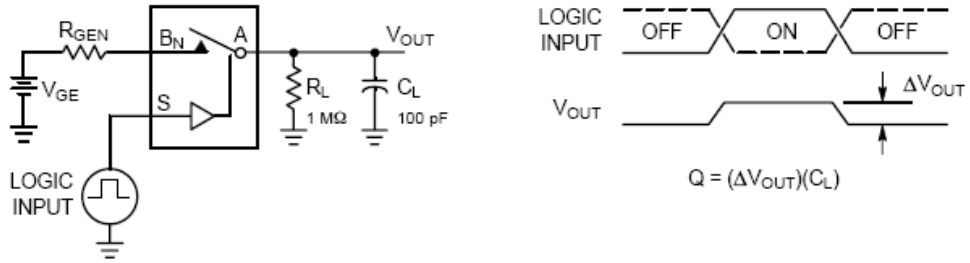


Figure 3 Charge

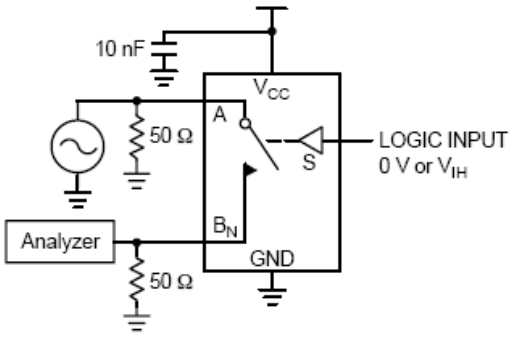


Figure 4 Turning off

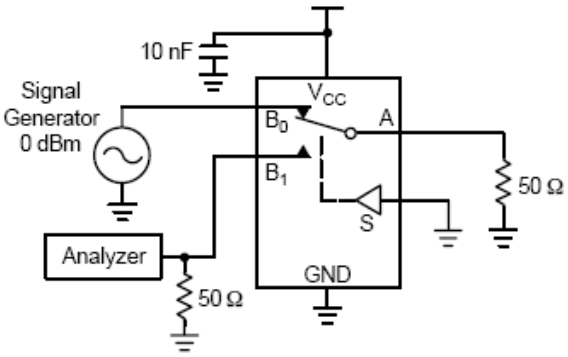


Figure 5 Crosstalk

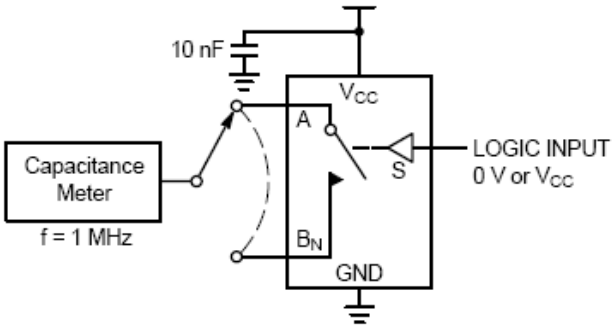


Figure 6 Output

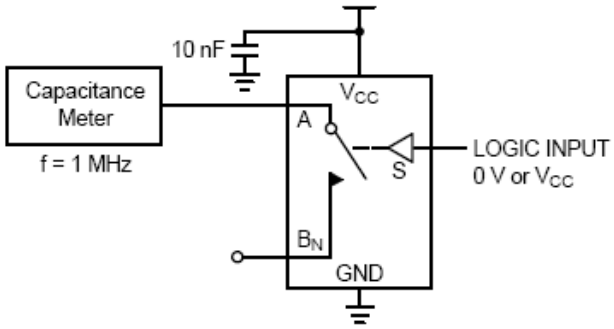


Figure 7 Output

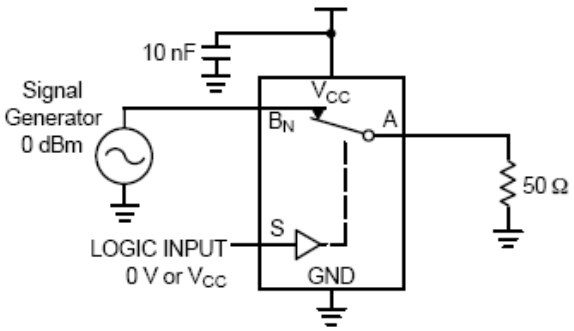
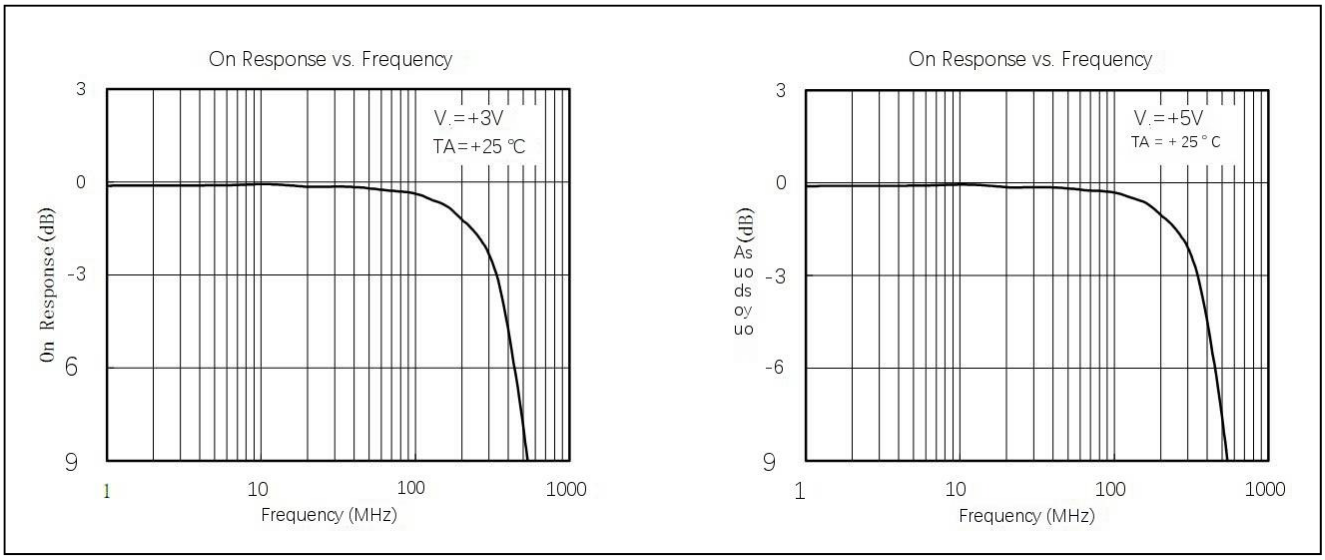
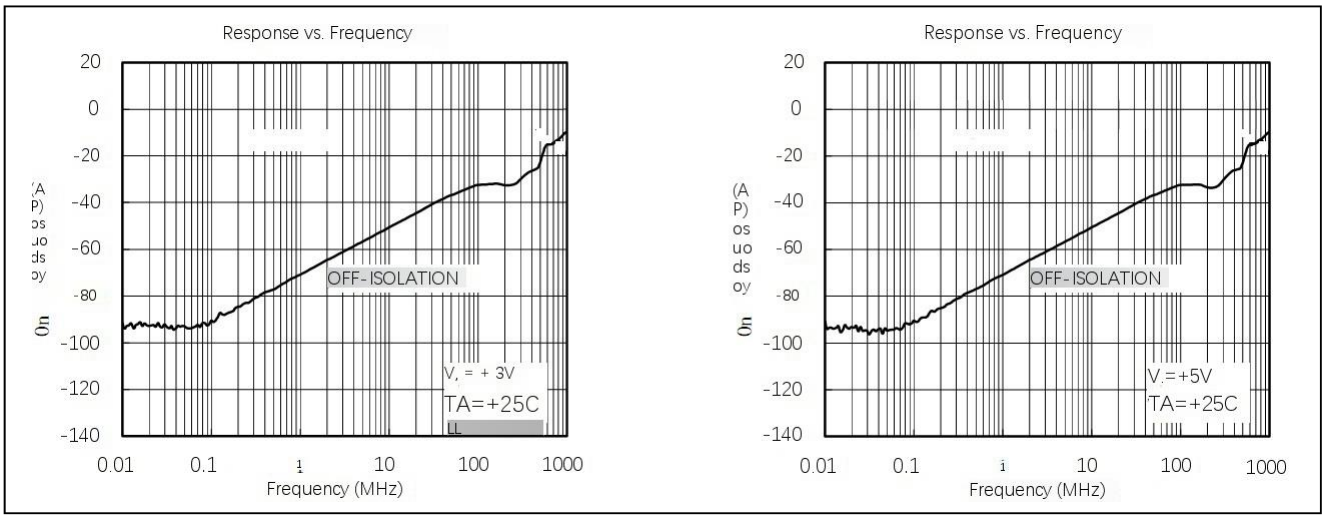


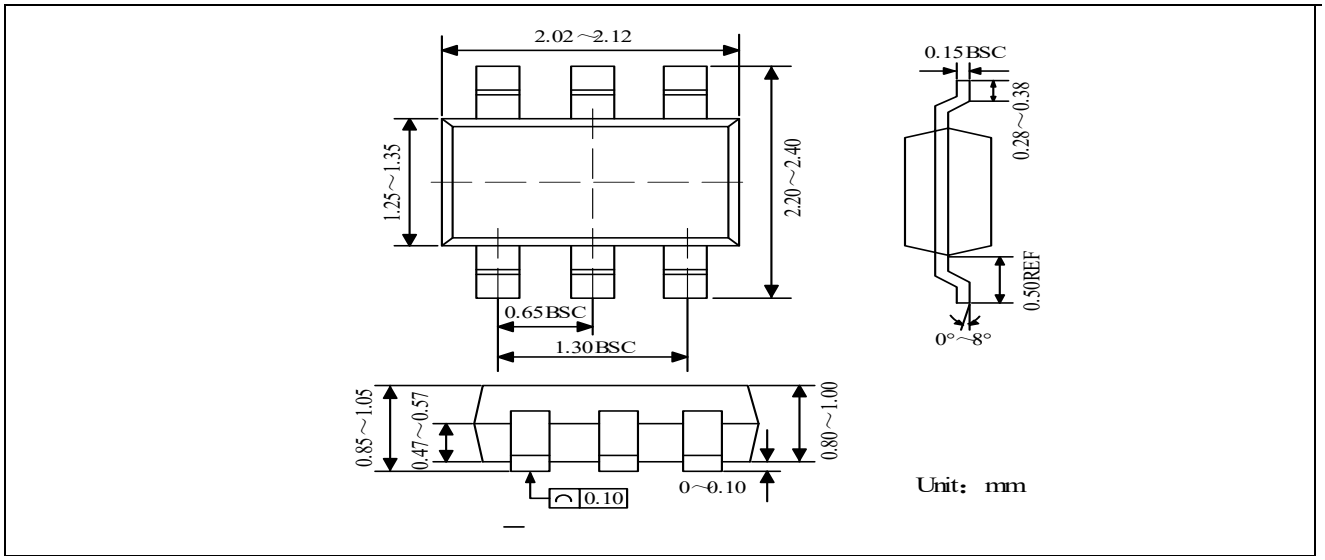
Figure 8 Bandwidth


On Response vs. Frequency
V.=+3V
TA=+25 ℃
On Response (dB)
3
0
-3
6
9
1
10
100
1000
Frequency (MHz)
On Response vs. Frequency
V.=+5V
TA = + 25 ° C
3
0
-3
-6
9
1
10
100
1000
Frequency (MHz)

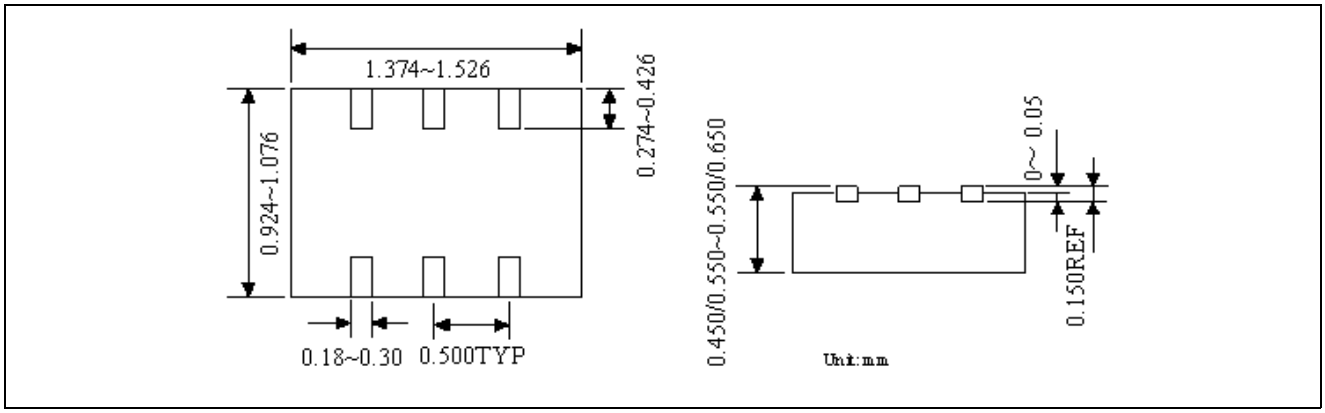

Response vs. Frequency
OFF-ISOLATION
V, = + 3V
TA=+25C
20
0
-20
-40
-60
-80
-100
-120
-140
0.01
0.1
1
10
100
1000
Frequency (MHz)
Response vs. Frequency
OFF-ISOLATION
V.=+5V
TA=+25C
20
0
-20
-40
-60
-80
-100
-120
-140
0.01
0.1
1
10
100
1000
Frequency (MHz)

Package size

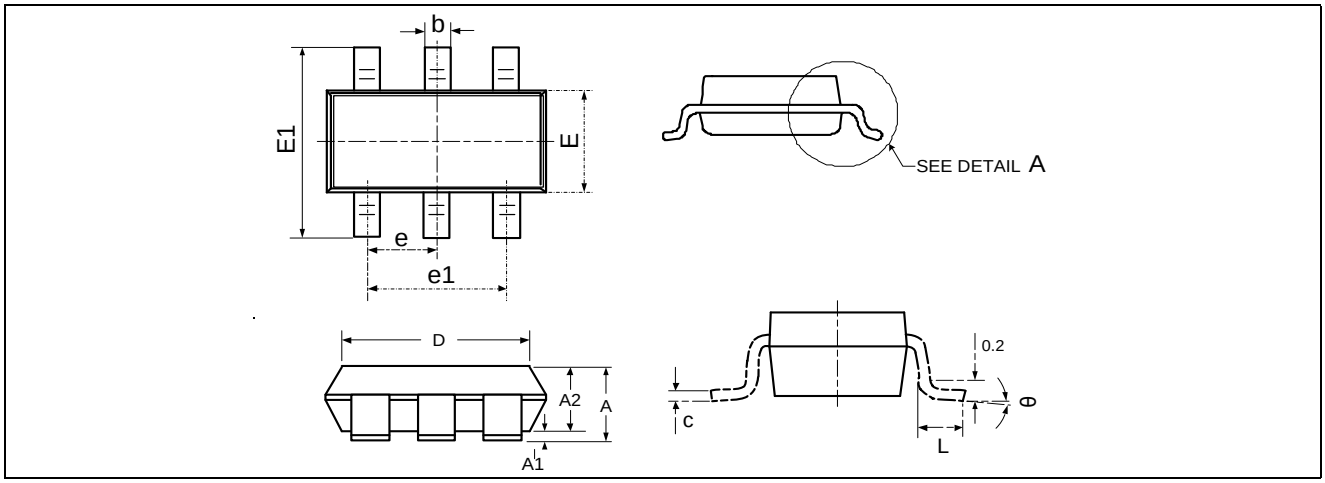
SC70-6



DFN6



SOT23-6



Order information

Order Code	Package	Baseqty	Deliverymode
UMW SN74LVC1G3157DBVR	SOT23-6	3000	Tape and reel
UMW SN74LVC1G3157Y	DFN6	3000	Tape and reel
UMW SN74LVC3157DCKR	SC70-6	3000	Tape and reel