1 Features and Benefits

Microcontroller

- Communication CPU Mlx4 for LIN protocol handling
- Application CPU Mlx16, 16 bit RISC-CPU, C-programmable
- Programmable digital watch-dog with several different modes
- 19 inputs interrupt controller
- Common purpose timer

Memories

- 32 Kbyte Flash + 16 Kbyte ROM with ECC, shared between Mlx16 and Mlx4
- 2 Kbyte RAM , shared by Mlx16 and Mlx4
- 2 x 256 Byte NVRAM with ECC, only accessible by the Mlx16

Periphery

- pre-driver for small NFETs (<30nC@25kHz PWM) to drive 2x DC, BLDC or Stepper motor
- 8 pins for Digital IO, ADC, Timer/Capture, Master/Slave SPI
- 5 programmable 16-bit PWM modules with frequencies 10…50kHz
- PWM-synchronized fast internal current sense circuit for sensorless sine drive
- 28 MHz +/-5% PLL clock derived from internal RC-oscillator
- integrated watchdog, independent from system-clock
- on-chip temperature sensor with +/-10°C accuracy
- 10 bit ADC < 6 µs conversion, auto-DMA storage, 24 channels, 0.75-1.5-2.5V reference
- overcurrent detection; overvoltage and undervoltage protection
- overtemperature protection

Voltage regulator

- normal operating voltage VS = 5.5V...28V (operating voltage up to 36V limited to 24h over lifetime)
- undervoltage interrupt setting between 4V…9V
- 3.3V regulator for >25mA current to supply Hall or Triaxis position sensor
- MCU control in 3.5V...28V range, without losing memory/register content
- low SLEEP MODE current of typ. < 25uA; periodic wake-up timer < 100uA

Bus interface

- support for PWM, LIN 2.x, SAE J2602
- wake-up possible via LIN, external pin IO[3] or internal wake-up timer

2 Application Examples

- Small BLDC pumps or valves
- DC motor positioning for WindowLift, Sunroofs, Seats, Doors with LIN
- DC Blowers or DC Fans with LIN

3 Ordering Information

Order Code	Temp. Range	Package	Delivery	Remark
MLX81325 LLQ-BMA-003-RE	-40 - 150 °C	QFN32 5x5	Reel	MLX81325B (AA)
MLX81325 LLQ-BMA-103-RE	-40 - 150 °C	QFN32 5x5	Reel	MLX81325B (ILS)

Table 3.1: Ordering Information

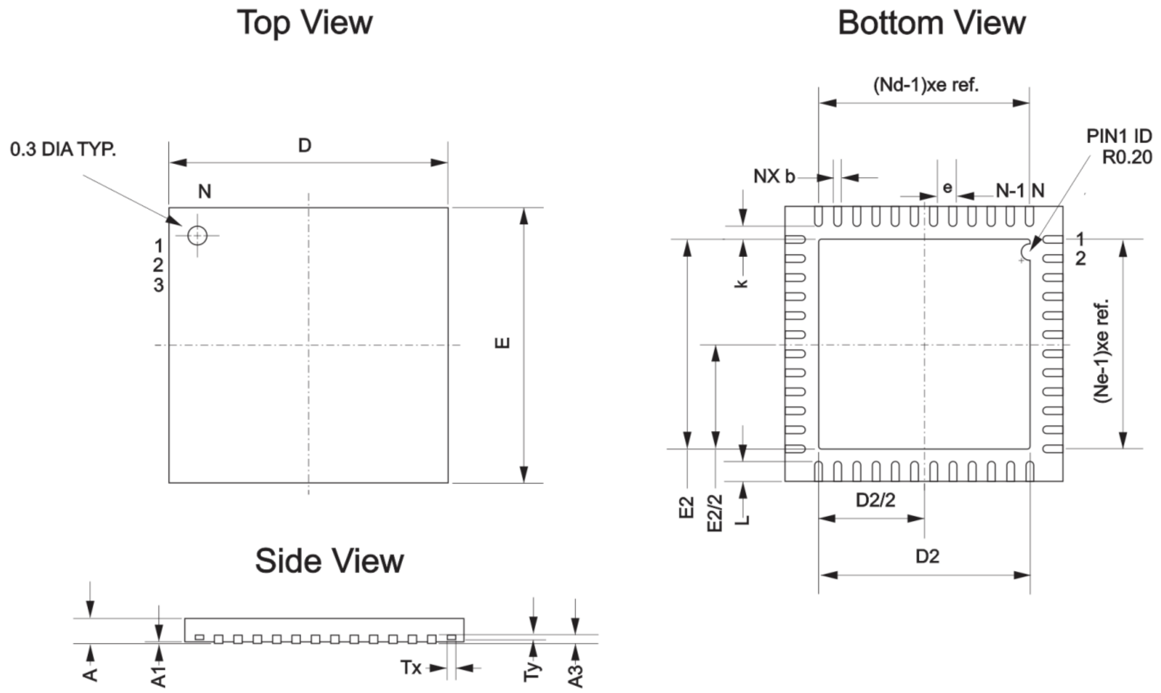
4 Family Concept

	MLX81310	MLX81315	MLX81325
MCU Memory	32 KB Flash	32 KB Flash	**32 KB Flash + 16 KB ROM**
MCU NVRAM	4x 128 Byte	4x 128 Byte	**4x 128 Byte**
MCU RAM	2 KB	2 KB	**2 KB**
Driver / Pre-Driver	4x Driver on-chip typ.5Ω Halfbridge	4x Driver on-chip typ.1Ω Halfbridge	**4x Pre-Driver <30nC ext. NFETs**
IO pins (analog, digital)	7x LV + 1x HV	7x LV + 1x HV	**7x LV + 1x HV**
Motor current sense	Low side, On-chip	Low side, On-chip	**Low-side, differntial external shunt**
Sensor interface (3.3V supply)	analog, pwm, spi	analog, pwm, spi	**analog, pwm, spi**
Sensorless support (hw + sw)	yes	yes	**yes**
LIN auto-address support (AA)	yes	yes	**yes, option 0xx**
Maximum IC Temperature (with validated mission profile)	T_j = 175°C	Tj = 175°C	**Tj = 175°C**
Package	QFN32, 5x5	QFN32, 5x5	**QFN32, 5x5**

Table 4.1: Family features

5 Technical description

5.1 Package data QFN32, 5x5



Symbol [2]	A	A1	A3	b	D	D2	E	E2	e	L	Tx	Ty	N [3]	Nd [4]	Ne [4]
Min	0.80	0.00		0.18		3.50		3.50		0.35					
Nom	0.90	0.02	0.20	0.25	5.00	3.60	5.00	3.60	0.50	0.40	0.16	0.10	32	8	8
Max	1.00	0.05		0.30		3.70		3.70		0.45					

Figure 5-1: Package data QFN32

[1] Dimensions and tolerances conform to ASME Y14.5M-1994
[2] All dimensions are in Millimeters. All angels are in degrees
[3] N is the total number of terminals
[4] ND and NE refer to the number of terminals on each D and E side respectively

5.2 Marking instruction

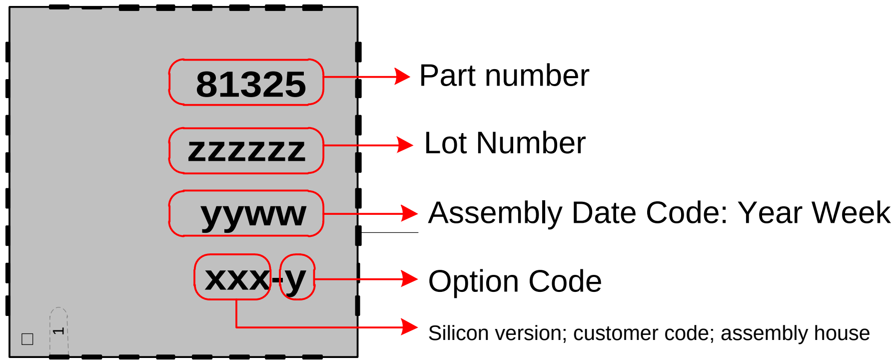


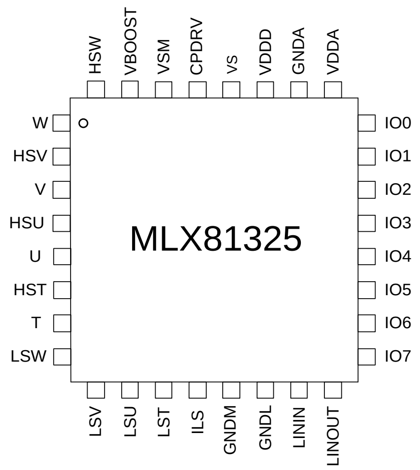
Figure 5-2: Marking example on IC package QFN32 5x5 package

5.3 Pin out description

Pin Nr	Pin name	voltage	remarks and description
1	W	Pwr HV	Motor phase W
2	HSV	Pwr HV	High side driver output phase V
3	V	Pwr HV	Motor phase V
4	HSU	Pwr HV	High side driver output phase U
5	U	Pwr HV	Motor phase U
6	HST	Pwr HV	High side driver output phase T
7	T	Pwr HV	Motor phase T
8	LSW	Pwr HV	Low side driver output phase W
9	LSV	Pwr HV	Low side driver output phase V
10	LSU	Pwr HV	Low side driver output phase U
11	LST	Pwr HV	Low side driver output phase T
12	ILS	Pwr LV	Positive input of the current sensor
13	GNDM	Ground	Power and digital ground
14	GNDL	Ground	LIN ground
15	LININ	Pwr HV	LIN transceiver BUS pin, connected to master side
16	LINOUT	Pwr HV	Option 0xx: LIN transceiver BUS pin connected to end of bus side
16	ILS2	Pwr LV	Option 1xx: negative input of the current sensor
17	IO7	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
18	IO6	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
19	IO5	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
20	IO4	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
21	IO3	Ana HV	General Purpose Digital I/O pins/ Low/High-Voltage input for ADC, Wake up
22	IO2	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
23	IO1	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
24	IO0	Ana LV	General Purpose Digital I/O pins / Analog input for ADC
25	VDDA	Pwr LV	Regulator output (~3.3 V), external blocking capacitors
26	GNDA	Ground	Ground pin for analog
27	VDDD	Pwr LV	Regulator output (~1.8 V), external blocking capacitors for Digital part
28	VS	Supply HV	Battery supply voltage for Analog part; external protection against reverse polarity needed, external blocking capacitors
29	CPDRV	Pwr HV	Charge pump clock
30	VSM	Supply HV	Battery supply voltage for Drivers Part; external protection against reverse polarity needed, external blocking capacitors

Pin Nr	Pin name	voltage	remarks and description
31	VBOOST	Pwr HV	Charge pump voltage
32	HSW	Pwr HV	High side driver output phase W

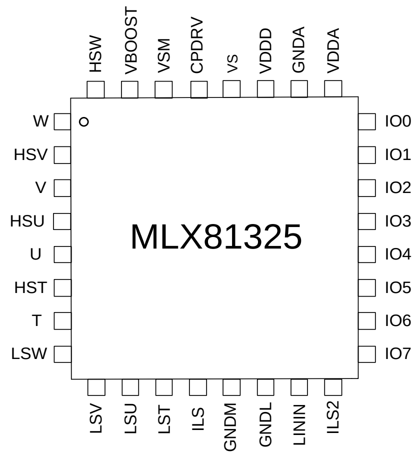
Option code 0xx



Option code 0xx

Table 5.1 Pin out description for option 0xx

Option code 1xx



Option code 1xx

Table 5.2 Pin out description for option 1xx

5.4 Absolute Maximum Ratings

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the MLX81325 is only specified within the limits shown in “Operating conditions”.

Parameter	Symbl	Condition	Limit Min	Max	Unit
Battery supply voltage	VS		-0.5	28 (36V [8])	V
		t < 500 ms	-0.5	45	V
	VSM		VDDA-0.3	28 (36V [8])	V
		t < 500 ms	VDDA-0.3	45	V
	VS.tr1	ISO 7637-2 pulse 1 [1] VS=13.5V, TA=(23 ± 5)°C	-100		V
	VS.tr2	ISO 7637-2 pulse 2 [1] VS=13.5V, TA=(23 ± 5)°C		+75	V
	VS.tr3	ISO 7637-2 pulses 3A, 3B [1] VS=13.5V, TA=(23 ± 5)°C	-150	+100	V
Battery supply current	IVSM_max	maximum DC or RMS supply current VSM		125	mA
Output voltage	VDDA		-0.3	3.6	V
Output voltage	VDD1V8		-0.3	1.95	V
LIN Bus	VLIN	T < 500ms	-27	45	V
	VBUS.tr1	ISO 7637-2 pulse 1 [2] VS=13.5V, TA=(23 ± 5)°C	-100		V
	VBUS.tr2	ISO 7637-2 pulse 2 [2] VS=13.5V, TA=(23 ± 5)°C		+75	V
	VBUS.tr3	ISO 7637-2 pulses 3A, 3B [2] VS=13.5V, TA=(23 ± 5)°C	-150	+100	V
	ILIN_max	Maximum current in LININ or LINOUT	-200	200	mA
Voltage on Analogue HV	VAN_HV	IO3 with internal divider T, U, V, W outputs	-0.3	VS+0.3	V
Voltage on PIN VBOOST	VAN_VBOOST	switching transients at 36V motor drive		45	V
Voltage on Analogue HV	VAN_HSx		-0.3	VBOOST+0.3	V
Voltage on Analogue HV	VAN_LSx		-0.3	VREF+0.3	V
Voltage on pin ILS	VAN_ILS, VAN_ILS2		-0.5	VDDA+0.3	V
Voltage on IO[7:4] and IO[2:0]	VIO_LV		-0.3	VDDA+0.3	V
Voltage on IO[3]	VIO_HV		-0.3	VS+0.3	V
Current on IO[7:0]	IIN_DIG		-10	10	mA

Parameter	Symbl	Condition	Limit Min	Max	Unit
Maximum latch–up free current at any pin	ILATCH	according JEDEC JESD78, AEC-Q100-004	-100	100	mA
Maximum latch–up free current at driver pins	ILATCH_driver	@ t= 10 msec	-250	250	mA
ESD capability of pin LIN	ESD_{HBM_LIN}	Human body model, acc. AEC-Q100-002 [7][4]	-6	+6	kV
ESD capability of pin LIN	ESD_{IEC_LIN}	acc. IEC 61000-4-2 [6]	-6	+6	kV
ESD capability of any other pin, except LIN	ESD_{HBM}	Human body model [7]	-2	+2	kV
ESD capability at any pin	ESD_{CDM}	Charge Device Model, acc. ANSI/ESDA/JEDEC JS-002	-500	+500	V
Storage temperature	Tstg		-55	150	°C
Junction Temperature	TJ		-40	175	°C
Thermal resistance MLF32 [3]	Rth	in free air	~ 32		K/W

Table 5.3: Absolute maximum ratings

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and >22µF/100nF blocking capacitor; ISO 7637 test pulses for 24V car battery needs to be protected by external components;
[2] ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1nF (as required by German OEM) ISO 7637 test pulses for 24V car battery needs to be protected by external components;
[3] Simulated value for low conductance board (JEDEC).
[4] ESD is applied on LIN pin against shorted GND pins
[6] Equivalent to discharging a 150pF capacitor through a 330Ω resistor conform to IEC Standard 1000-4-2.
[7] Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.
[8] 36V operation is limited to maximum 24 hours over life; 28..36V motor driving may require 100..500 Ohm resistor at Vboost pin to protect in case of pcb switching transients >45V

5.5 Operating Conditions

The IC can have 6 different hardware modes. The exact functionality of these modes depends on the hardware and software configuration:

- Reset:
  - Triggered by hardware. When VS or VDDA or VDDD drop below a critical level, the complete chip is powered down.
  - The analogue and digital supply regulators are disabled. No functionality is available in this mode.
- Normal mode. Main application running
  - Microcontroller fully functional
  - Analogue fully functional
- Power Saving Mode
  - Application CPU halted
  - Wake-up by interrupt.
- Under voltage: triggered by the hardware under voltage detection interrupt. (VS_UV)
  - Microcontroller fully functional.
  - Analogue functionality under software control.
  - Reduced current capability on VDDA below VS=5.5V.
- Over voltage: triggered by the hardware over voltage detection interrupt. (VS_OV)
  - Microcontroller fully functional
  - Analogue functionality under software control.
- Sleep Mode: Triggered by the software.
  - Microcontroller powered down
  - Digital and analogue supply powered down.
  - Sleep Mode and wake-up functionality running on help supply Vaux

Parameter	Symbol	Conditions	Limit			Unit
			Min	Typ	Max	
Supply Voltage Range	VS		5.5		28 (36 [2])	V
Supply Voltage Range Low battery	VS_lb		3.5[1]		5.5	V
Ambient Temperature	TA		-40		150	°C
Junction Temperature for FLASH Program and Erase	TJFLPR		0		85	°C
Junction Temperature for NVRAM Program and Erase	TJNVPR		-40		165	°C

Table 5.4: Operating Conditions

[1] IC will work down to 3.5V with reduced analogue characteristics, Digital part still works, Memories will keep their content. Some analogue parameter will drift out of limits, but chip function can be guaranteed. Before going down to 3.5V the VS has to be at the startup of the IC for a certain time > 5.5V to guarantee a correct reset!

[2] IC will work up to 36V with reduced analogue characteristics, Digital part still works, Memories will keep their content. 36V operation is limited to maximum 24 hours over life

5.6 Electrical parameter specification

Following characteristics are valid over the full temperature range of Tj = -40°C to +165°C and a supply range of 28V (36V for max. 24h over life time) ≥ VS=VSM > 5.5V unless otherwise noted.
With 5.5V ≥ VS > 3.5 V the controller still works, Memories keep their contents, analogue parameters cannot be guaranteed. The VS has to be at the startup of the IC for a certain time > 5.5V to guarantee a correct reset!
If several pins are charged with transients above VS and below VSS, the summary of all substrate currents of the influenced pins should not exceed 10mA for correct work of the device.
All voltages refer to ground of IC, which is built by short of all existing ground pins, which were split to meet EMC performance and lowest possible noise influence.

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
Global parameters						
Normal working current	Inom	all pins are inputs, trimmed PLL to 28 MHz; no external loads, Normal LIN communication		10	30	mA
Sleep Mode current	Isleep	chip in sleep mode; T ≤ 150 °C VS = 13 V, T ≤ 35 °C VS = 13 V, T > 35 °C VS = 18 V VS > 18 V			 30 80 100 200	 µA µA µA µA
Holding mode current	Ihold	All pins are inputs, No motor drive, Mlx16 in halt T Wake up MLX16: 25ms ADC: 2 conversions every 25ms Drivers: on , ChargePump on MLX4 LIN: connected Watchdog: on LINAA: off [9]			7	mA
Frequencies						
Frequency of the trimmed RC oscillator	frc_1M	RC oscillator is trimmed	-5%	1	+5%	MHz
Frequency of the PLL	fpll	System RC oscillator is trimmed	-5%	28	+5%	MHz
Settling time of the PLL	tsetpll	RC oscillator is trimmed, PLL is switched on			250	µs
Frequency separate 10kHz RC oscillator for the analogue Watchdog	frc_10k	Value of Frc_10k	5	10	20	kHz
Temperature dependency of the 10kHz RC oscillator	Tc_Frc_10k		-10		10	% of Frc_10k

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
Startup time after Power On	tstartup_POR	C_3.3V=100nF; C_1.8V=100nF Time to 1st Flash instruction			20	ms
Startup time of the Charge pump (CP)	tstartup_CP	Time from CP start to VBOOST = VS+ 6V for VS>12V; motor not running during startup, Cfly=100 nF, Cboost = 1 µF			5	ms
VDDA related parameters (external C: 47nF … 220nF)						
3.3V supply voltage range	VDDA	with trimmed VBG	3.15	3.3	3.45	V
External output current capability	Iddout_VDDA				25	mA
VDDD related parameters (external C: 47nF … 220nF)						
1.8V supply voltage range	VDDD	after trimming	1.77	1.85	1.93	V
External output current capability	Iddout_VDDD				0	mA
VDDA based UV RESET parameters						
Undervoltage reset on	Vuvr_hl_VDDA		2.7	2.85	3	V
Undervoltage reset off	Vuvr_lh_VDDA		2.85	3	3.15	V
Hysteresis for undervoltage reset	Vhyst_uvr_VDDA	guaranteed by design	0.1			V
Debouncing for UVR	tuvr_VDDA		1	3	10	µs
VDDD based UV RESET parameters						
Undervoltage reset on	Vuvr_hl_VDDD		1.525	1.6	1.675	V
Undervoltage reset off	Vuvr_lh_VDDD		1.6	1.675	1.75	V
Hysteresis for undervoltage reset	Vhyst_uvr_VDDD	guaranteed by design	0.05			V
Debouncing for UVR	tuvr_VDDD		1	3	10	µs
POR parameters (VS based; for information only)						
POR off	Vpor_lh	only for information		3.6		V
POR on	Vpor_hl	only for information		3.15		V
Hysteresis for POR	Vhyst_por	only for information	60			mV
VS – Programmable under voltage interrupt parameters (Brown out)[1]						
Programmable range for under voltage level	Vuv_range	PRUV[2:0]: 000 001 010 011 100 101	 3.5 4.5 5.5 6.5 7.5 8.5	 4 5 6 7 8 9	 4.5 5.5 6.5 7.5 8.5 9.5	 V V V V V V

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
Hysteresis for under voltage	Vhyst_uv		0.1		1	V
Debouncing for under voltage	Tuv	only for information	10	30	60	µs
VS - Over Voltage (Load dump) interrupt related parameters						
Level for load dump interrupt on	Vld_lh	PROV: 0 1	31.5 37	33 38.5	34.5 40	V V
Level for load dump interrupt off	Vld_hl	PROV: 0 1	29.5 34.5	31 36	32.5 37.5	V V
Hysteresis for load dump interrupt	Vhyst_ld		1	2	3	V
Debouncing for load dump interrupt	Tld	only for information	50		100	µs
ADC (10Bit) related parameters						
ADC full scale range (code 0x3FF corresponds to fsr)	fsr3	ADC_REF[1:0]=11	2.45	2.5	2.55	V
	fsr2	ADC_REF[1:0]=10	1.47	1.5	1.53	V
	fsr1	ADC_REF[1:0]=01	0.735	0.75	0.765	V
	fsr0	ADC_REF[1:0]=00 ADC reference disabled		off		V
Differential nonlinearity	DNL	only characterized; no production test	-1		+1	LSB
Integral nonlinearity	INL	only characterized; no production test	-3		+3	LSB
Quantization steps	RESADC	guaranteed by design	1024			LSB
Minimum conversion Time	Tconv	frequency = 2MHz frequency = 4MHz guaranteed by design		6 3		µs
Minimum sampling time	Tsamp	Time between channel select and start conversion (4 MHz) guaranteed by design	3			µs
Minimum time between 2 ADC conversions	Tcycl	Tcycl = Tsamp + Tconv (for 4MHz) w/o channel change Tcycl = Tsamp + Tconv (for 4MHz) with channel change guaranteed by design	6 7			µs
ADC error (excluding ADC reference and INL)	ErrADC	LV channels	-1		1	%
		HV channels (with predivider)	-3		3	%
IO[7:0] related parameters						
Leakage current in IO[7:0]	Ileakio[7:0]	1/16 divider on IO3 disabled.	-5		5	µA

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
Fast Digital Input; (not active in SLEEP MODE)						
Digital input threshold level L => H	Vinhio[7:0]				2.4	V
Digital input threshold level H => L	vinlio[7:0]		1			V
Digital input Hysteresis	Vinhystio[7:0]		0.1			
Digital Input for WAKE UP on IO3 (VAUX supplied)						
Digital WU input threshold level L => H	Vinlhio_wu	Active in SLEEP MODE			2.7	V
Digital WU input threshold level H => L	Vinhlio_wu	Active in SLEEP MODE	1.2			V
Hysteresis	Vhystio_wu		0.1			V
Low Voltage Push-Pull Stage of IO7..4, IO2..0 (not active in SLEEP MODE)						
Output voltage low	VoutlIO[7:4, 2:0]	Iload = 2mA			0.4	V
Output voltage high	VouthIO[7:4, 2:0]	Iload = 2mA	VDDA - 0.4			V
Low Voltage Push-Pull Stage of IO3 (not active in SLEEP MODE)						
Output voltage low	VoutlIO[3]	Iload = 1mA, SPI_EN = 1; SPIOUT = 0			0.4	V
Output voltage high	VouthIO[3]	Iload = 1mA, SPI_EN = 1; SPIOUT = 1	VDDA - 0.4			V
IO Voltage Range for ADC measurement						
Input Voltage Range for ADC measurement	Vin_adc_IO[7:4, 2:0]	For information only	0		2.5	V
IO3_HV Input Voltage range for ADC measurement	Vin_adc_IO3	For information only Measurement of V(IO3)/16	0		36	V
Temperature Sensor related parameters						
Temperature Shutdown circuit						
Over temperature shutdown interrupt	Tot_on	tested by special test mode only	170	180	190	°C
	Tot_off		140	150	160	°C
	Tot_hyst	guaranteed by design	10			°C
Temperature Sensor (for ADC measurement)						
Temperature range	Trange	Sensor measures IC junction temperature	-40		180	°C
Temperature	TEMP_GAIN			0.5		°C/LSB

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
measurement gain						
Accuracy	Tacc	Measurement error versus T-junction temperature after calibration	-10		10	°C
VSM Sensor related parameters						
Input range	VS_min		5.5			V
	VS_max	@ ADC_REF[1:0]=11 @ ADC_REF[1:0]=10 @ ADC_REF[1:0]=01 @ ADC_REF[1:0]=00			36 24 12 off	V
Output Capability	Tsettling_ADC	Time to charge the ADC sampling cap, only characterized; no production test		0.3	0.5	µs
Low-Pass Filter cut-off frequency (@VSM)	Fvs_filter	-3dB cut=off frequency, only characterized; no production test	0.7		1.5	kHz
VSM sensor filter Offset	Vadc_vsm_off	Referred to input voltage (VSM)	-300		300	mV
Motor Driver related parameters						
Bottom pre-driver						
FET Gatedrive voltage	VREF	Assured output voltage when VSM ≥ 7 V 5.5 V < VSM < 7 V If no undervoltage detected	6 VSM - 1	8	9	V V
Ron charge	R_LS_HIGH	VS=VSM = 8V…36V Tested at 13V in production	10	30	60	Ohm
Ron discharge	R_LS_LOW	VS=VSM = 8V…36V Tested at 13V in production	10	25	50	Ohm
Top pre-driver						
Ron charge	R_HS_HIGH	VS=VSM = 8V…36V Tested at 13V in production	8	40	80	Ohm
Ron discharge	R_HS_LOW	VS=VSM = 8V…36V Tested at 13V in production	8	40	80	Ohm
Charge Pump						
Charge pump output	VBOOST	VSM ≥ 10 V 8V < VSM < 10 V 5.5V < VSM < 8V (BAT54S, Tj<150degC)	VSM + 7 VSM + 5.5 VSM + 3	VSM + 8	VSM + 9.5 VSM + 9.5 VSM + 8	V V V

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
CPDRV output resistance	R_CPDRV_HIGH	Iload=2mA Tested at 13V in production	15	40	120	Ohm
	R_CPDRV_LOW		10	26	60	
CP output frequency	CP_FREQ		40	50	60	kHz
Dead Time for FET switching						
Dead Time	T_DEAD	Programmable with 3 bits. ANA_OUTG[4:2] 000 001 010 011 100 101 110 111		 0.4 0.8 1.2 1.6 2.0 2.4 2.8 3.2		 µs µs µs µs µs µs µs µs
Motor Current Sensor parameters						
Current sensor input range	V_CURR_IR	Allowed input range of shunt voltage (eg. 100 mOhm shunt: 1A = 100mV)	-100		100	mV
Current sensor Gain	Acs		9.5	10	10.5	
Current sensor reference	Vcs0	V(ILS) = 0		1.25		V
Current sensor calibration error	Vcs_err	measured at the output of the current sensor (ADC input)	-20		20	mV
Current sensor low pass filter time	tcs_filter	Guaranteed by design Typical RC is formed with R = 40kOhm and C = 5pF	0.25	0.5	1	µs
Overcurrent detection (via comparator)						
Short circuit detection level	Voc		260	300	330	mV
Debouncing for OC	Toc	Digital filter based on RC clock Programmable with 2 bits. DEB_OC[1:0] 00 01 10 11	 1 2 4 8		 2 4 8 16	 µs µs µs µs
External FET monitoring						

Parameter	Symbol	Conditions	Limit Min	Limit Typ	Limit Max	Unit
Detection level	Vds	Vds over voltage level when FET is on	1.5	2	2.5	V
Filter Time	Tvds	Time from Fet on till Vds monitoring start. Programmable with 2 bits. IO:VDS_MASKTIME[1:0] 00 01 10 11		 1.6 3.2 4.8 6.4		 µs µs µs µs
LIN related parameters ISO_DIS_17987-4 , SAE J2602, 8V ≤ VBAT ≤ 18V.						
DC Parameters						
Transmitter						
Short circuit bus current	IBUS_LIM	$V_{BUS} = V_{BAT}$ = 18V, driver on $V_{BUS} = V_{BAT}$ = 36V , driver on	40 75		200 300	mA
Pull up resistance bus, normal & standby mode [8]	RSLAVE		20		60	kOhm
Pull up current, SLEEP MODE	ILIN_PU-Sleep	V_{BUS}=0, V_{BAT}=12V, SLEEP MODE	-100			µA
Input Leakage at the receiver incl. PU	IBUS_PAS_dom	V_{BUS}=0, V_{BAT}=12V V_{BUS}=0, V_{BAT}=24V	-1 -2			mA
Bus reverse current, recessive	IBUS_PAS_rec	driver off, 8V<V_{BAT}≤27V, 27V<V_{BAT}<36V, V_{BUS} > V_{BAT}			20 50	µA
Bus reverse current loss of battery	IBUS_NO_BAT	VS = 0V, 0V < V_{BUS} < 18V 18V < V_{BUS} < 36V LIN 2.1		1	23 100	µA
Bus current during loss of ground	IBUS_NO_GND	VS=VGND=12V, 0 < V_{BUS} < 18V VS=VGND=24V, 0 < V_{BUS} < 36V	-1 -2		1 2	mA
Transmitter dominant voltage	Vol_{BUS}	network load =500Ω / TxDx = 0	0		0.2	VS
Transmitter recessive voltage	Voh_{BUS}	TxDx open	0.8		1	VS
BUS input capacitance; MLX Value for LIN conformance test	CBUS	Pulse response via 10kΩ, V_{PULSE} = 12V, VS open		25	35	pF
Receiver						
Receiver dominant voltage	VBUSdom				0.4	VS

Parameter	Symbol	Conditions	Limit			Unit
			Min	Typ	Max	
Receiver recessive voltage	VBUSrec		0.6			VS
Centre point of receiver threshold	VBUS_CNT	VBUS_CNT=(VBUSdom+ VBUSrec)/2	0.475	0.5	0.525	VS
Receiver Hysteresis	VBUS_hys	VBUS_cnt =(VBUSrec - VBUSdom)	0.15		0.175	VS
AC Parameters						
Propagation delay receiver [2], [3], [6]	trx_pdf	CRxD =25pF falling edge			6	µs
Propagation delay receiver [2], [3], [6]	trx_pdr	CRxD =25pF rising edge			6	µs
Prop. delay receiver symmetry [6]	trx_sym	trx_pdf - trx_pdr	-2		2	µs
Receiver debounce time [7]	trec_deb	LIN rising & falling edge	0.5		4	µs
LIN duty cycle 1 [3] [4]	D1	20kbps operation , normal mode	0.396			-
LIN duty cycle 2 [3] [4]	D2	20kbps operation , normal mode			0.581	-
LIN duty cycle 3 [3] [4]	D3	10.4kbs operation , low speed mode	0.417			-
LIN duty cycle 4 [3] [4]	D4	10.4kbs operation , low speed mode			0.590	-
trec(max) – tdom(min) [5]	Δt3	10.4kbs operation , low speed mode			15.9	µs
trec(min) – tdom(max) [5]	Δt4	10.4kbs operation , low speed mode			17.28	µs
TxD dominant timeout [6]	tTxD_to	Normal mode, VTxD = 0V		64		ms

Table 5.5: Electrical parameters

[1] PLL should be switched off at brown out condition. Analog parameters are not guaranteed during brown out.
[2] This parameter is tested by applying a square wave signal to the LIN. The access to internal signals RxD,TxD will be performed by test mode. The minimum slew rate for the LIN rising and falling edges is 50V/µs.
[3] See Figure 5-3: LIN timing diagram
[4] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled
[5] In accordance to SAE J2602
[6] Parameter in relation to internal signal TxD
[7] Internal MLX value to suppress spikes; only proved during characterisation: not measured in production
[8] The pull-up resistance is always connected to the LIN-bus; Only when LIN Auto-addressing firmware code is included, the pull-up can be disconnected during the LIN Auto-Addressing sequence
[9] IHOLDmax increases by ~0.5mA in case LINAA is switched on.

As shown in figure, both worst case duty cycles can be calculated as follows :

$$D_{wc1} = t_{BUS\_rec(min)} / 2 * t_{Bit}$$
$$D_{wc2} = t_{BUS\_rec(max)} / 2 * t_{BIT}$$

Thresholds for duty cycle calculation in accordance to LIN2.x:

Baud rate	20kBaud	10.4kBaud
t_{Bit}	50µs	96µs
D_{wc1}	D1	D3
D_{wc2}	D2	D4
$TH_{REC(MAX)}$	0.744 V_{S_TX}	0.778 V_{S_TX}
$TH_{DOM(MAX)}$	0.581 V_{S_TX}	0.616 V_{S_TX}
$TH_{REC(MIN)}$	0.422 V_{S_TX}	0.389 V_{S_TX}
$TH_{DOM(MIN)}$	0.284 V_{S_TX}	0.251 V_{S_TX}

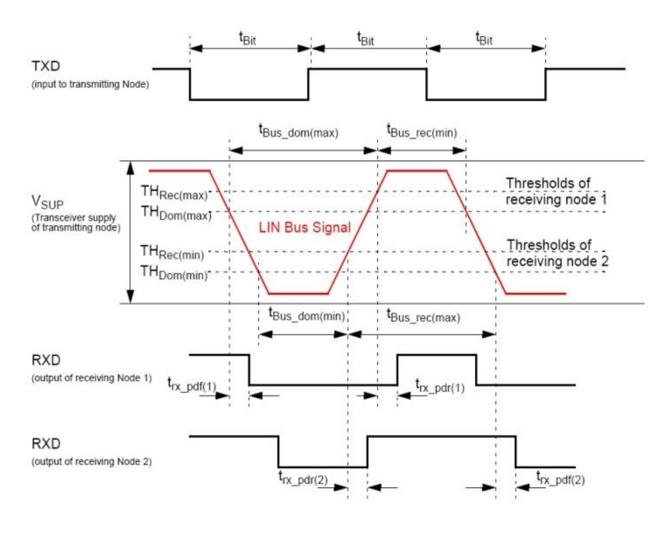


Figure 5-4: LIN timing diagram: Relation between propagation delay and duty cycle

6 MLX81325 – Typical application schematic

In the following schematic example, all external components are indicated that are needed to protect the IC against EMC / ESD pulses.

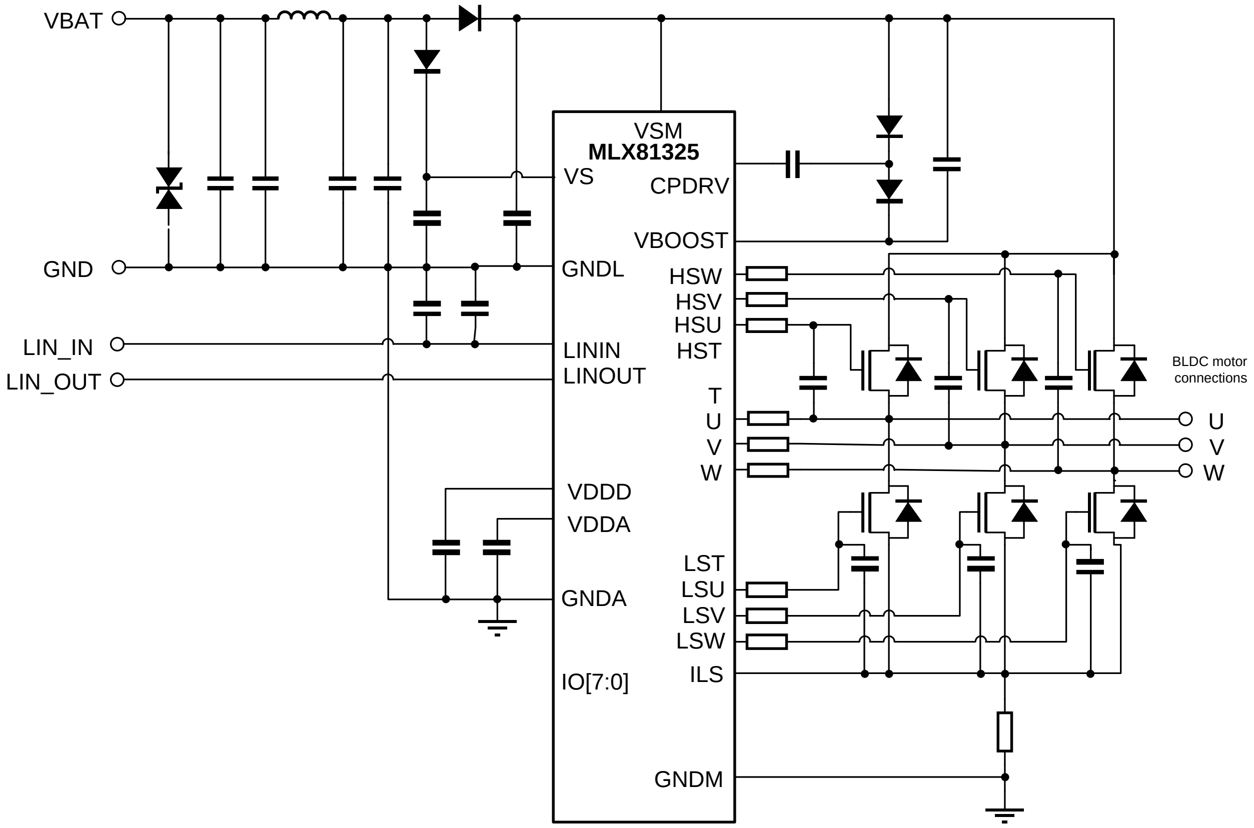


Figure 6-1: Typical BLDC motor schematic with MLX81325

The following schematic is an example for a differential shunt measurement of the external current. All external components are indicated that are needed to protect the IC against EMC / ESD pulses.

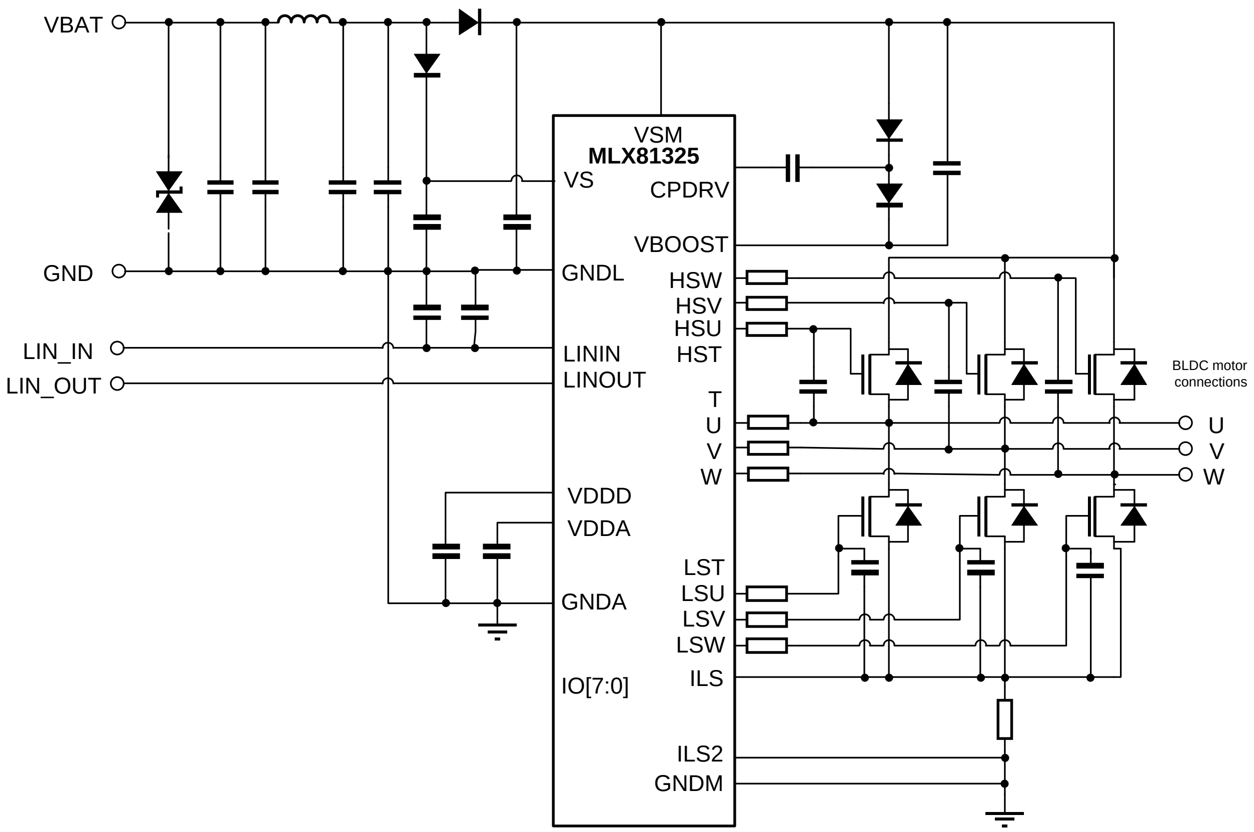


Figure 6-2: Typical BLDC motor schematic with MLX81325 with option 1xx (differential shunt measurement)

7 Functional description

7.1 Block-Diagram

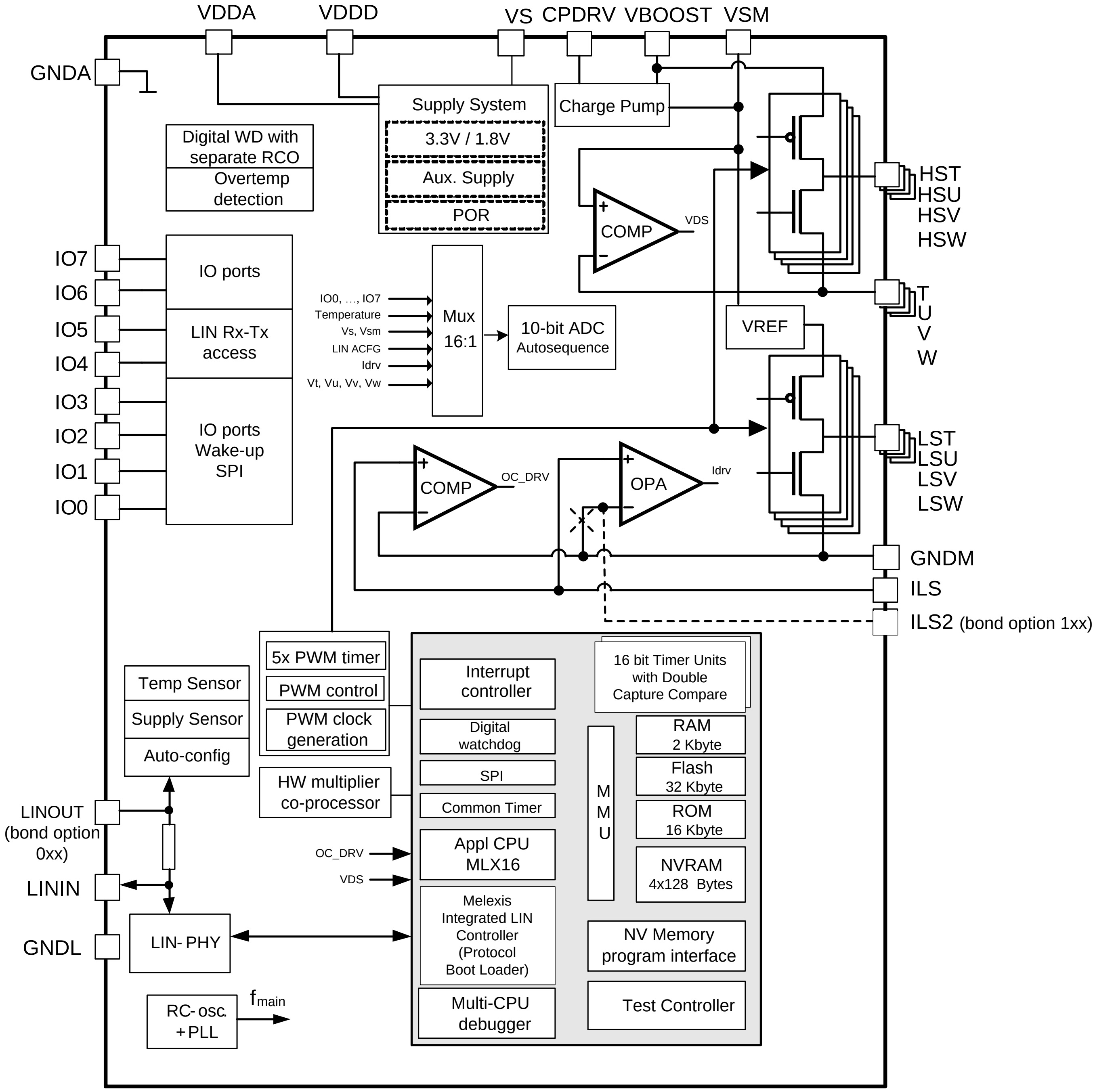


Figure 7-1: Functional block diagram

8 Debugging Facilities

Hardware and software debugging tools are available for MLX81325, the description of the available tool set is not a part of this document.

9 Assembly Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.
The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.
Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.aspx

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