


High-side driver with MultiSense analog feedback for automotive applications



PowerSSO-36

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Minimum cranking supply voltage (V_{CC} decreasing)	$V_{USD_Cranking}$	3 V
Typ. on-state resistance	R_{ON}	1.3 m Ω
Current limitation (typ)	I_{LIMH}	200 A
Standby current (max)	I_{STBY}	20 μ A

- AEC-Q100 qualified 
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Single channel smart high-side driver
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
 - Multiplexed analog feedback of: load current, V_{CC} supply voltage and T_{CHIP} device temperature
 - Overload and short to ground indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Latch-off on over-temperature (ΔT_{J_SD} or TSD)
 - Loss of ground and loss of V_{CC}
 - Reverse battery with self switch of the PowerMOS
 - Electrostatic discharge protection

Product status

VN7000AY

Product summary

Order code	VN7000AYTR
Package	PowerSSO-36
Packing	Tape and reel

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Especially intended for Automotive power distribution applications

Description

The device is a single channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation and overload management by ΔT_J and over-temperature shut-down with latch-off.

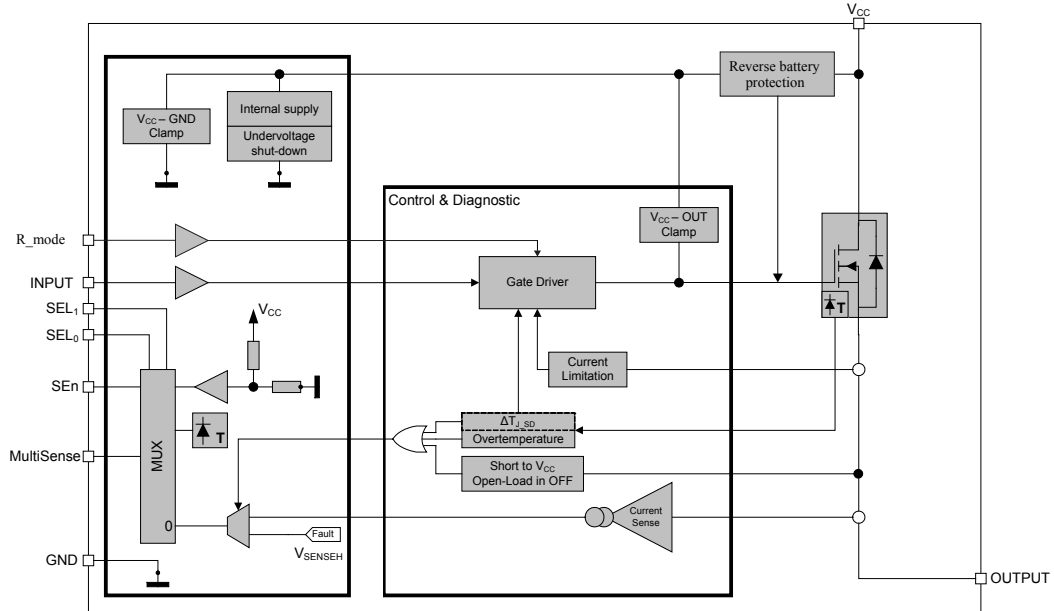
A toggling on the INPUT pin unlatches the output in case of fault.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

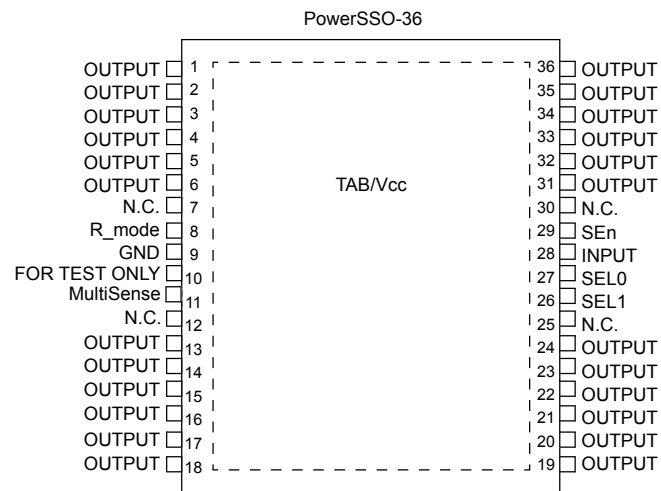
A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

A R_mode pin allows to switch low respectively high R_{DSon} operating mode, so to adapt current sense precision and current limitation accordingly to the selected load.

1 Block diagram and pin description

Figure 1. Block diagram

Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state. It unlatches the output in case of fault.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
SEL _{0,1}	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
R_mode	Active high CMOS compatible input pin; it enables the high R _{DSon} mode. If kept low, sets the low R _{DSon} mode

Figure 2. Configuration diagram (top view)


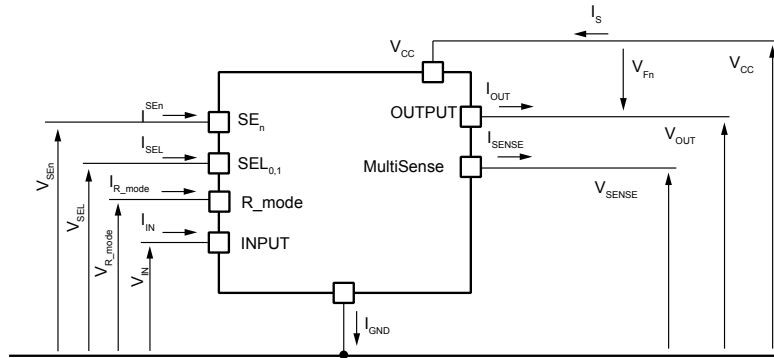
Note: The pins from 1 to 6, from 13 to 18, from 19 to 24 and from 31 to 36 have to be soldered together on the PCB.

Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SE _n , SEL _x , R _{mode}	FOR TEST ONLY
Floating	Not allowed	X ⁽¹⁾	X	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor	Through 10 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions


GAPG220120191445FSR

Note: $V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and $INPUT = LOW$.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3. Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO 7637-2:2004 Pulse 5b level IV clamped to 40 V; $R_L = 4 \Omega$)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	140	
I_{IN}	DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1} DC input current		
I_{R_mode}	R_mode DC input current	10	mA
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0 V$)		
	MultiSense pin DC output current in reverse ($V_{CC} < 0 V$)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4 ms$; $T_{jstart} = 150 \text{ }^\circ\text{C}$, R_mode = Low)	190	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)	4000	V
	INPUT		

Symbol	Parameter	Value	Unit
V _{ESD}	MultiSense	2000	V
	SEn, SEL _{0,1} , R_mode	4000	
	OUTPUT	4000	
	V _{CC}	4000	
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
R _{thj-case}	Thermal resistance junction-case ⁽¹⁾	1.4	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽²⁾	50.7	
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾	15.3	

1. Device mounted on four-layer 2s2p PCB

2. Device mounted on two-layer 2s0p PCB with 2 cm² heatsink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; - 40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 5. Electrical characteristics during cranking

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{USD_Cracking}	Minimum cranking supply voltage (V _{CC} decreasing)				3	V
R _{ON_L}	On-state resistance	I _{OUT} = 30 A; V _{CC} = 3 V; V _{CC} decreasing; T _j = 150 °C			7	mΩ
R _{ON_H}	On-state resistance	I _{OUT} = 7.5 A; V _{CC} = 3 V; V _{CC} decreasing; T _j = 150 °C			28	mΩ
T _{TSD} ⁽¹⁾	Shutdown temperature (V _{CC} decreasing)	V _{CC} = 3 V	140			°C

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				3	V
$V_{USDReset}$	Undervoltage shutdown reset				5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R_{ON_H}	On-state resistance in high R_{mode}	$I_{OUT} = 7.5\text{ A}; T_j = 25^\circ\text{C}$		4.2		mΩ
		$I_{OUT} = 7.5\text{ A}; T_j = 150^\circ\text{C}$			9	
		$I_{OUT} = 7.5\text{ A}; V_{CC} = 4\text{ V}; T_j = 25^\circ\text{C}$			6.8 ⁽¹⁾	
R_{ON_L}	On-state resistance in low R_{mode}	$I_{OUT} = 30\text{ A}; T_j = 25^\circ\text{C}$		1.3		mΩ
		$I_{OUT} = 30\text{ A}; T_j = 150^\circ\text{C}$			2.8	
		$I_{OUT} = 30\text{ A}; V_{CC} = 4\text{ V}; T_j = 25^\circ\text{C}$			2.3 ⁽¹⁾	
R_{ON_REV}	On-state resistance in reverse battery	$I_{OUT} = -30\text{ A}; V_{CC} = -13\text{ V}; T_j = 25^\circ\text{C}$		1.3		mΩ
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}; T_j = -40^\circ\text{C}$	38			V
		$I_S = 20\text{ mA}; 25^\circ\text{C} < T_j < 150^\circ\text{C}$	41	46	52	
I_{STBY}	Supply current in standby at $V_{CC} = 13\text{ V}$ ⁽²⁾	$V_{CC} = 13\text{ V}; V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}; V_{SELO,1} = 0\text{ V}; V_{R_mode} = 0\text{ V}; T_j = 25^\circ\text{C}$			0.5	μA
		$V_{CC} = 13\text{ V}; V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}; V_{SELO,1} = 0\text{ V}; V_{R_mode} = 0\text{ V}; T_j = 85^\circ\text{C}$ ⁽³⁾			2.5	
		$V_{CC} = 13\text{ V}; V_{IN} = V_{OUT} = V_{SEn} = 0\text{ V}; V_{SELO,1} = 0\text{ V}; V_{R_mode} = 0\text{ V}; T_j = 125^\circ\text{C}$			20	
t_{D_STBY}	Standby mode blanking time	$V_{CC} = 13\text{ V}; V_{IN} = V_{OUT} = V_{SELO,1} = 0\text{ V}; V_{R_mode} = 0\text{ V}; V_{SEn} = 5\text{ V to } 0\text{ V}$	60	300	550	μs
$I_{S(ON)}$	Supply current	$V_{CC} = 13\text{ V}; V_{SEn} = V_{SELO,1} = 0\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 0\text{ A}; V_{R_mode} = 0\text{ V}$		4	8	mA
$I_{GND(ON)}$	Control stage current consumption in ON state.	$V_{CC} = 13\text{ V}; V_{SEn} = 5\text{ V}; V_{SELO,1} = 0\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 30\text{ A}; V_{R_mode} = 0\text{ V}$			8	mA
$I_{L(off)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 125^\circ\text{C}$	0		20	
V_F	Output - V_{CC} diode voltage	$I_{OUT} = -30\text{ A}; T_j = 150^\circ\text{C}$			0.7	V

1. Parameter guaranteed only at $V_{CC} = 4\text{ V}$ and $T_j = 25^\circ\text{C}$
2. PowerMOS leakage included.
3. Parameter specified by design; not subjected to production test.

Table 7. Switching ($R_{mode} = \text{Low}$)

$V_{CC} = 13\text{ V}; -40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ ⁽¹⁾	Turn-on delay time at $T_j = 25^\circ\text{C}$	$R_L = 0.43\ \Omega$	85	160	265	μs
$t_{d(off)}$ ⁽¹⁾	Turn-off delay time at $T_j = 25^\circ\text{C}$		100	145	200	

V _{CC} = 13 V; -40°C < T _j < 150°C, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
(dV _{OUT} /dt) _{on} ⁽¹⁾	Turn-on voltage slope at T _j = 25 °C	R _L = 0.43 Ω	0.04	0.1	0.25	V/μs
(dV _{OUT} /dt) _{off} ⁽¹⁾	Turn-off voltage slope at T _j = 25 °C		0.04	0.1	0.25	
W _{ON}	Switching energy losses at turn-on (t _{won})	R _L = 0.43 Ω	—	9	20 ⁽²⁾	mJ
W _{OFF}	Switching energy losses at turn-off (t _{woff})	R _L = 0.43 Ω	—	9	20 ⁽²⁾	mJ
t _{SKEW} ⁽¹⁾	Differential pulse skew (t _{PHL} - t _{PLH})	R _L = 0.43 Ω	-130	-30	70	μs

1. See Figure 8. Switching time and Pulse skew.
2. Parameter guaranteed by design and characterization; not subjected to production test.

Table 8. Switching (R_{mode} = High)

V _{CC} = 13 V; -40°C < T _j < 150°C, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} ⁽¹⁾	Turn-on delay time at T _j = 25 °C	R _L = 1.72 Ω	85	160	265	μs
t _{d(off)} ⁽¹⁾	Turn-off delay time at T _j = 25 °C		80	115	160	
(dV _{OUT} /dt) _{on} ⁽¹⁾	Turn-on voltage slope at T _j = 25 °C	R _L = 1.72 Ω	0.05	0.14	0.3	V/μs
(dV _{OUT} /dt) _{off} ⁽¹⁾	Turn-off voltage slope at T _j = 25 °C		0.05	0.14	0.3	
W _{ON}	Switching energy losses at turn-on (t _{won})	R _L = 1.72 Ω	—	1.9	3.8 ⁽²⁾	mJ
W _{OFF}	Switching energy losses at turn-off (t _{woff})	R _L = 1.72 Ω	—	1.9	3.8 ⁽²⁾	mJ
t _{SKEW} ⁽¹⁾	Differential pulse skew (t _{PHL} - t _{PLH})	R _L = 1.72 Ω	-140	-40	60	μs

1. See Figure 8. Switching time and Pulse skew.
2. Parameter guaranteed by design and characterization; not subjected to production test.

Table 9. Logic inputs

7 V < V _{CC} < 28 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
R_mode characteristics						
V _{R_modeL}	Input low level voltage				0.9	V
I _{R_modeL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{R_modeH}	Input high level voltage		2.1			V
I _{R_modeH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{R_mode(hyst)}	Input hysteresis voltage		0.2			V
V _{R_modeCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEL _{0,1} characteristics (7 V < V _{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V _{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 10. Protections

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH}	DC short circuit current	V _{CC} = 13 V; V _{IN} = 5 V; V _{R_mode} = 0 V	140	200	280	A
		4 V < V _{CC} < 18 V; V _{IN} = 5 V; V _{R_mode} = 0 V ⁽¹⁾				
		V _{CC} = 13 V; V _{IN} = 5 V; V _{R_mode} = 5 V	45	63	90	
		4 V < V _{CC} < 18 V; V _{IN} = 5 V; V _{R_mode} = 5 V ⁽¹⁾				
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 7		
T _{RS}	Thermal reset of fault diagnostic indication	V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽¹⁾			7		
ΔT _{J_SD}	Dynamic temperature	V _{CC} = 13 V		60		K
t _{LATCH_RST}	Fault reset time for output unlatch ⁽¹⁾	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40°C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25°C to 150°C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V

1. Parameter guaranteed by design and characterization; not subjected to production test.

Table 11. MultiSense

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	MultiSense clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		7		
Current sense characteristics						
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 3 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = High	-50%	5100	50%	
dK ₁ /K ₁ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 3 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = High	-20		20	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = High	-20%	5100	20%	
dK ₂ /K ₂ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = High	-15		15	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 30 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = Low	-20%	25000	20%	
dK ₃ /K ₃ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 30 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = Low	-8		8	%

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₄	I _{OUT} /I _{SENSE}	I _{OUT} = 45 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = Low	-15%	25000	15%	
dK ₄ /K ₄ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 45 A; V _{SENSE} = 4 V; V _{SEn} = 5 V; R _{mode} = Low	-6		6	%
I _{SENSE0}	MultiSense leakage current	MultiSense disabled: V _{SEn} = 0 V	0		0.5	μA
		MultiSense disabled: V _{SEn} = 0 V -1 V < V _{SENSE} < 5 V ⁽¹⁾	-0.5		0.5	
		MultiSense enabled: V _{SEn} = 5 V; diagnostic selected; V _{IN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 0 A			25	
		MultiSense enabled: V _{SEn} = 5 V; diagnostic selected: V _{IN} = 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT0} = 0 A	0		2	
V _{OUT_MSD} ⁽¹⁾	Output Voltage for MultiSense shutdown	V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ; V _{IN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 30 A		5		V
V _{SENSE_SAT}	Multisense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{SEn} = 5 V; V _{IN0} = 5 V; V _{SEL} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 30 A; T _j = -40°C; R _{mode} =0V	4.75			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; T _j = 150°C; R _{mode} =0V	4			mA
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; T _j = 150°C; R _{mode} =0V	110			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{SEn} = 5 V; V _{IN} = 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V	2	3	4	V
I _{L(off2)} ⁽³⁾	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C	-100		-15	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 11. T _{DSTKON})	V _{SEn} = 5 V; V _{IN} = 5 V to 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 0 A; V _{OUT} = 4 V	100	350	750	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V _{IN} = 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{OUT} = 4 V; V _{SEn} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{SEn} = 5 V; V _{IN} = 0 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{OUT} = 0 V to 4 V		5	30	μs
Chip temperature analog feedback						
V _{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V; V _{IN} = 0 V; R _{SENSE} = 1 kΩ; T _j = -40°C	2.325	2.41	2.495	V
		V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V; V _{IN} = 0 V; R _{SENSE} = 1 kΩ; T _j = 25°C	1.985	2.07	2.155	V

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V _{SEn} = 5 V; V _{SELO} = 0 V; V _{SEL1} = 5 V; V _{IN} = 0 V; R _{SENSE} = 1 kΩ; T _j = 125°C	1.435	1.52	1.605	V
dV _{SENSE_TC} /dT ⁽¹⁾	Temperature coefficient	T _j = -40°C to 150°C		-5.5		mV/K
Transfer function		V _{SENSE_TC} (T) = V _{SENSE_TC} (T ₀) + dV _{SENSE_TC} /dT * (T - T ₀)				
V _{CC} supply voltage analog feedback						
V _{SENSE_VCC}	MultiSense output voltage proportional to V _{CC} supply voltage	V _{CC} = 13 V; V _{SEn} = 5 V; V _{SELO} = 5 V; V _{SEL1} = 5 V; V _{IN} = 0 V; R _{SENSE} = 1 kΩ	1.55	1.62	1.69	V
Transfer function ⁽⁴⁾		V _{SENSE_VCC} = V _{CC} / 8				
Fault diagnostic feedback (see Table 12. Truth table)						
V _{SENSEH}	MultiSense output voltage in fault condition	V _{CC} = 13 V; R _{SENSE} = 1 kΩ; V _{IN} = 0 V; V _{SEn} = 5 V; V _{SELO} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 0 A; V _{OUT} = 4 V	5		6.6	V
I _{SENSEH}	MultiSense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see Figure 9. MultiSense timings (current sense mode)) ⁽⁵⁾						
t _{DSENSE1H}	Current sense settling time from rising edge of SE _n	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 0.43 Ω			60	μs
t _{DSENSE1L}	Current sense disable delay time from falling edge of SE _n	V _{IN} = 5 V; V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 0.43 Ω		5	20	μs
t _{DSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.43 Ω		470	720	μs
Δt _{DSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 0.43 Ω			300	μs
t _{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.43 Ω		210	330	μs
MultiSense timings (chip temperature sense mode - see Figure 10. Multisense timings (chip temperature and V _{CC} sense mode)) ⁽⁵⁾						
t _{DSENSE3H}	V _{SENSE_TC} settling time from rising edge of SE _n	V _{SEn} = 0 V to 5 V; V _{SELO} = 0 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSENSE3L}	V _{SENSE_TC} disable delay time from falling edge of SE _n	V _{SEn} = 5 V to 0 V; V _{SELO} = 0 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (V _{CC} voltage sense mode - see Figure 10. Multisense timings (chip temperature and V _{CC} sense mode)) ⁽⁵⁾						
t _{DSENSE4H}	V _{SENSE_VCC} settling time from rising edge of SE _n	V _{SEn} = 0 V to 5 V; V _{SELO} = 5 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSENSE4L}	V _{SENSE_VCC} disable delay time from falling edge of SE _n	V _{SEn} = 5 V to 0 V; V _{SELO} = 5 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (Multiplexer transition times) ⁽⁵⁾						
t _{D_CStoTC}	MultiSense transition delay from current sense to T _C sense	V _{IN} = 5 V; V _{SEn} = 5 V; V _{SELO} = 0 V; V _{SEL1} = 0 V to 5 V; I _{OUT} = 30 A; R _{SENSE} = 1 kΩ			60	μs

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{D_TcToCS}	MultiSense transition delay from T _C sense to current sense	V _{IN} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 5 V to 0 V; I _{OUT} = 30 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CStoVCC}	MultiSense transition delay from current sense to V _{CC} sense	V _{IN} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 0 V to 5 V; I _{OUT} = 30 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_VCCtoCS}	MultiSense transition delay from V _{CC} sense to current sense	V _{IN} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V to 0 V; I _{OUT} = 30 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_TcToVCC}	MultiSense transition delay from T _C sense to V _{CC} sense	V _{CC} = 18 V; T _j = 125°C; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_VCCtoTc}	MultiSense transition delay from V _{CC} sense to T _C sense	V _{CC} = 18 V; T _j = 125°C; V _{SEn} = 5 V; V _{SEL0} = 5 V to 0 V; V _{SEL1} = 5 V; R _{SENSE} = 1 kΩ			20	μs

1. Parameter guaranteed by design and characterization; not subjected to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
3. Parameter granted at -40 °C < T_j < 125 °C
4. V_{CC} sensing and T_C sensing are referred to GND potential.
5. Transition delay are measured up to +/- 10% of final conditions.

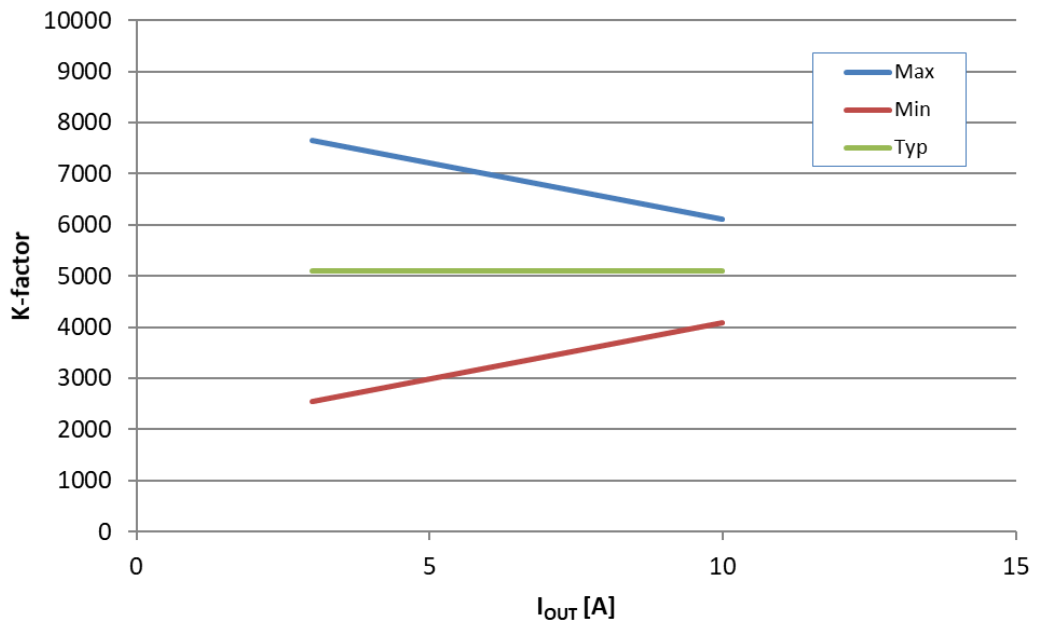
Figure 4. I_{OUT}/I_{SENSE} vs. I_{OUT} - High R_{DS(on)} mode


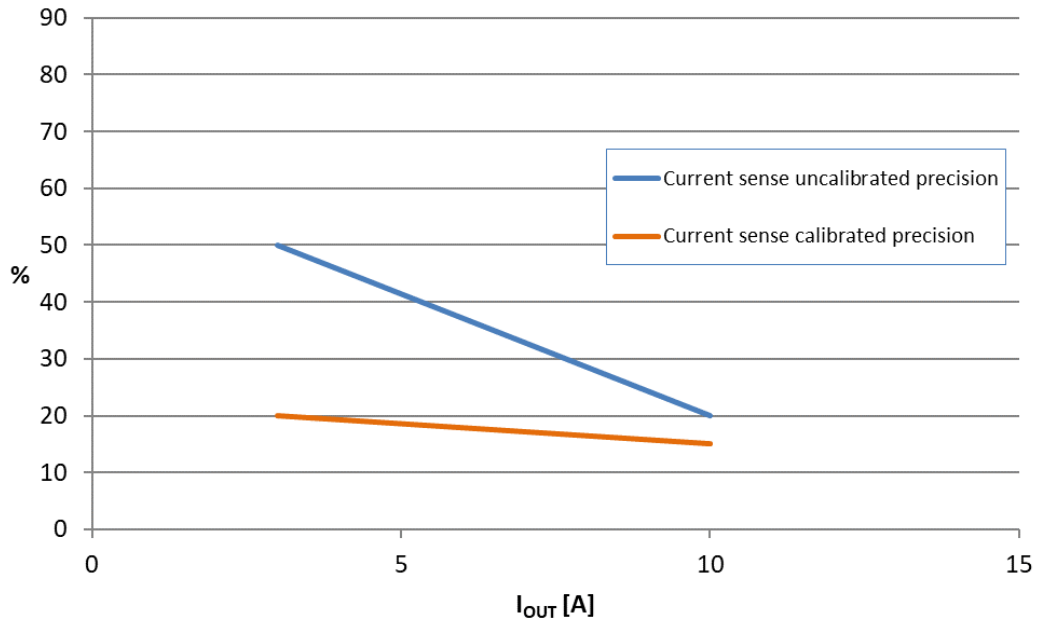
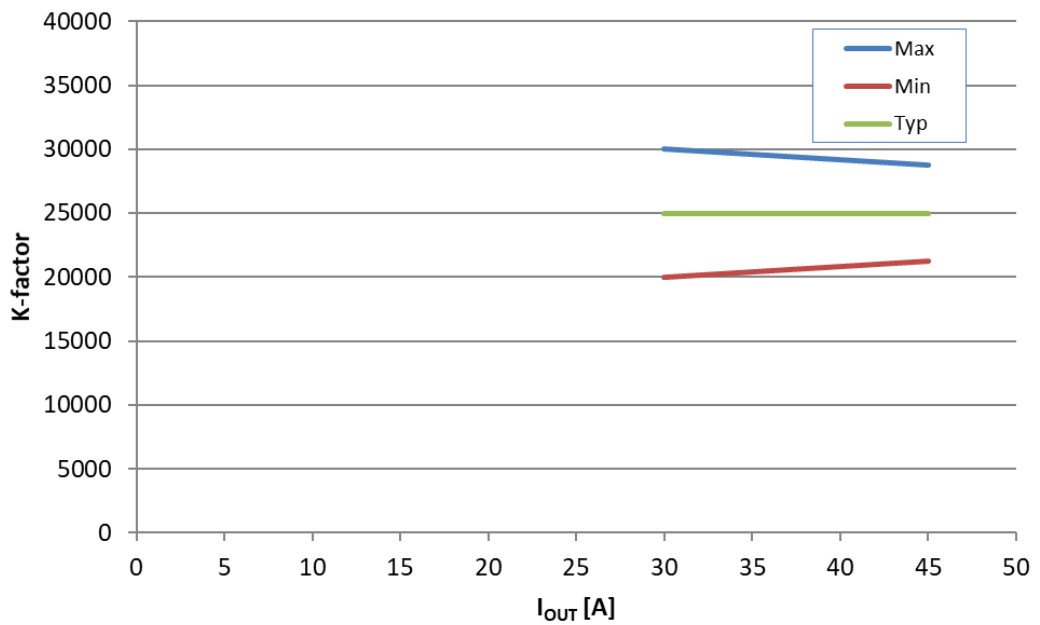
Figure 5. Current sense precision vs. I_{OUT} - High R_{DS(on)} mode

Figure 6. I_{OUT}/I_{SENSE} vs. I_{OUT} - Low R_{DS(on)} mode


Figure 7. Current sense precision vs. IO_{UT} - Low R_{DS(ON)} mode

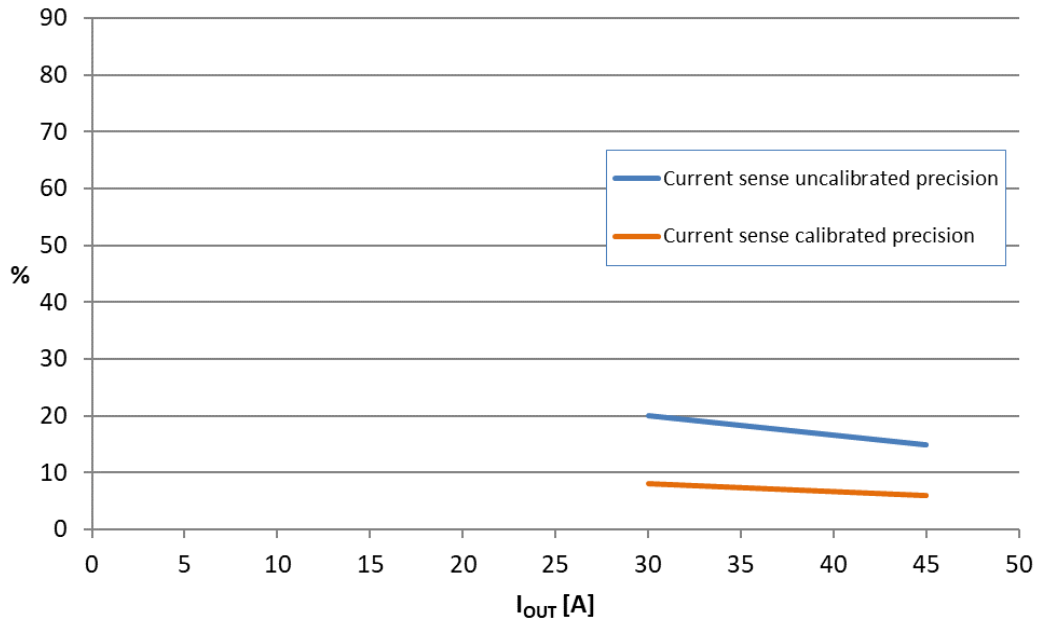


Figure 8. Switching time and Pulse skew

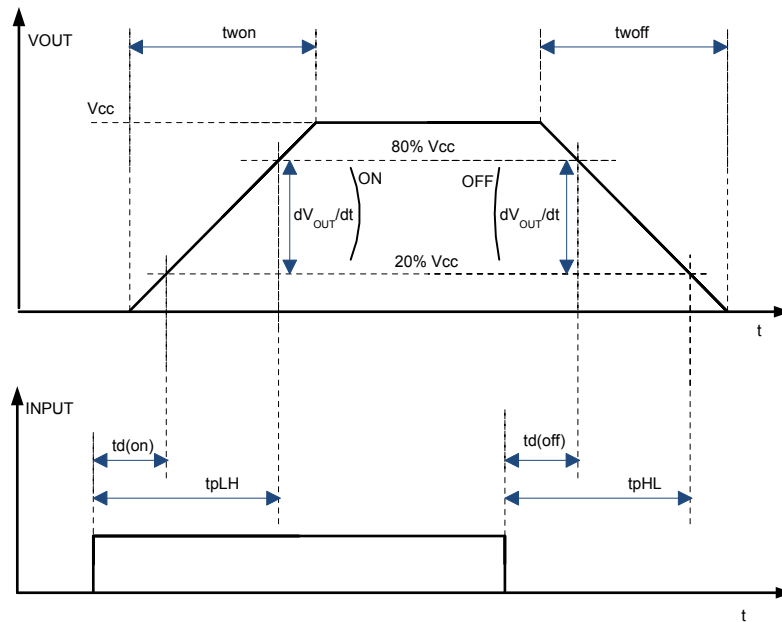


Figure 9. MultiSense timings (current sense mode)

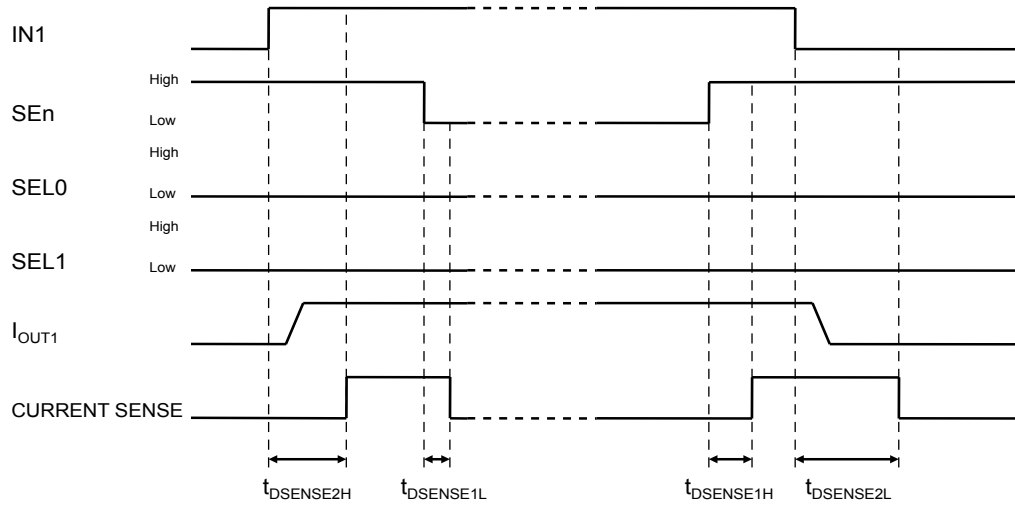
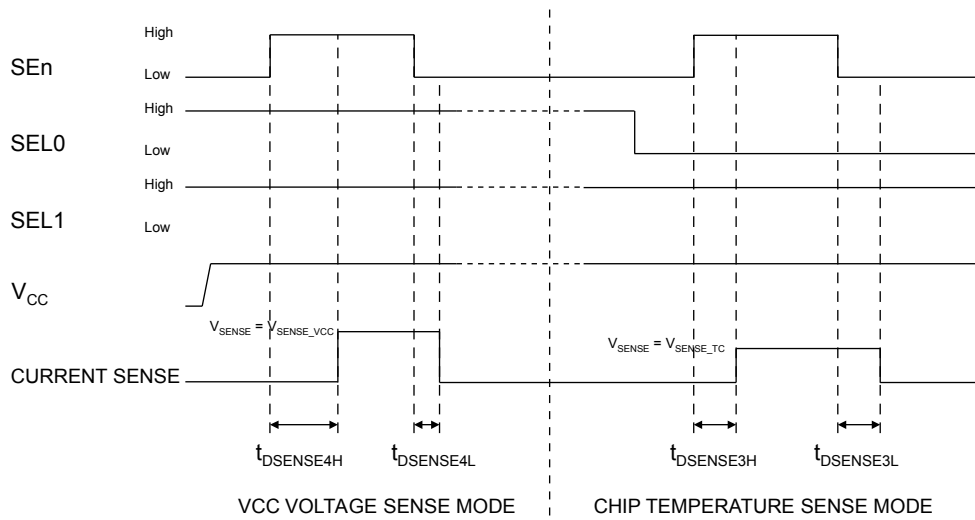
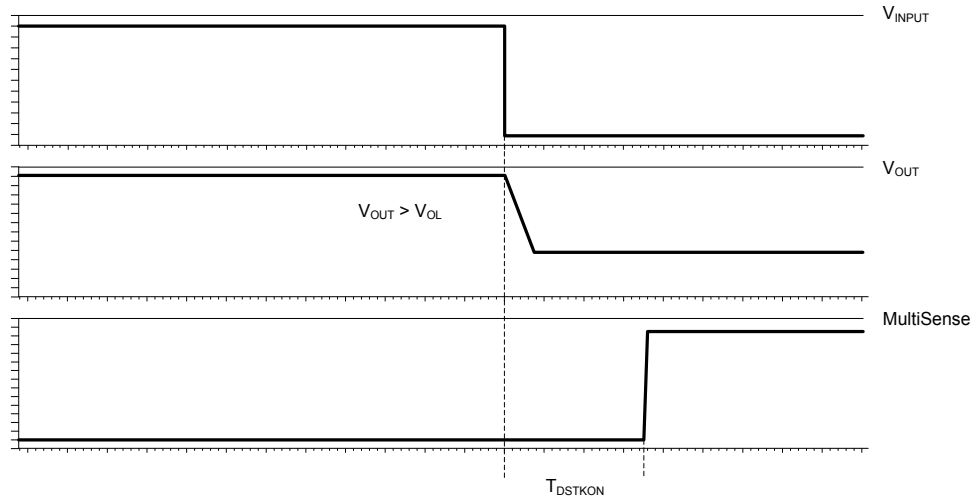


Figure 10. Multisense timings (chip temperature and V_{CC} sense mode)



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Figure 11. T_{DSTKON}


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Table 12. Truth table

Mode	Conditions	IN _x	SE _n	SEL _x	OUT _x	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150\text{ °C}$	L	See (1)		L	See (1)	
		H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	L	See (1)		L	See (1)	
		H			L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	L	Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
		L			L	Hi-Z	
OFF-state diagnostics	Short to V_{CC}	L	See (1)		H	See (1)	
	Open-load	L			H	See (1)	External pull-up
Negative output voltage	Inductive loads turn-off	L	See (1)		< 0 V	See (1)	

1. Refer to Table 13. MultiSense multiplexer addressing

Table 13. MultiSense multiplexer addressing

SEn	SEL ₁	SEL ₀	R_mode	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag.	Negative output
L	X	X	X		Hi-Z			
H	L	X	L	Channel diagnostic with Gain1	$I_{SENSE} = 1/K_{Gain1} * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	X	H	Channel diagnostic with Gain2	$I_{SENSE} = 1/K_{Gain2} * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	X	T _{CHIP} Sense	$V_{SENSE} = V_{SENSE_TC}$			
H	H	H	X	V _{CC} Sense	$V_{SENSE} = V_{SENSE_VCC}$			

Note: K_{Gain1} and K_{Gain2} are related to K-factor in Low respectively High R_{DSON} mode

2.4 Waveforms

Figure 12. Latch functionality - behavior in hard short circuit condition ($T_{AMB} \ll T_{TSD}$)

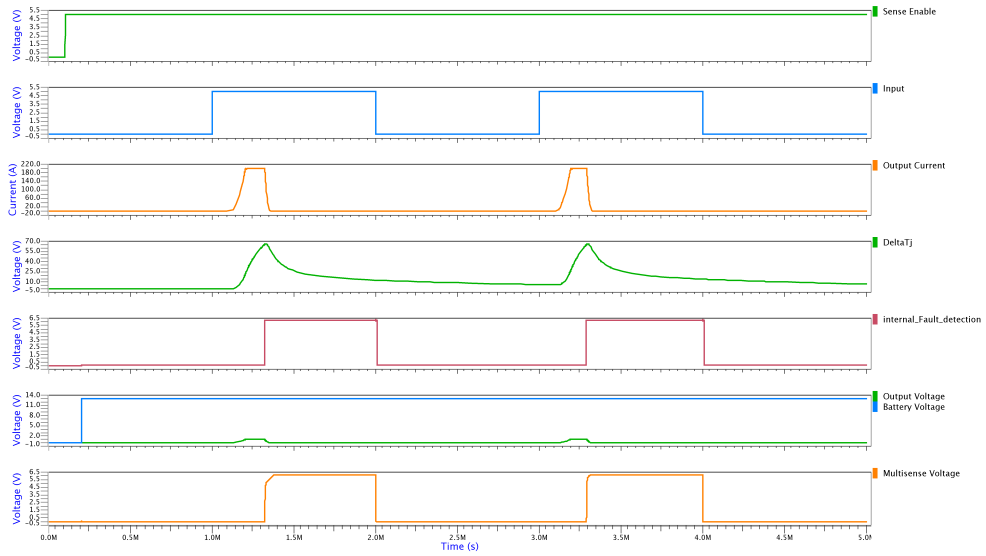
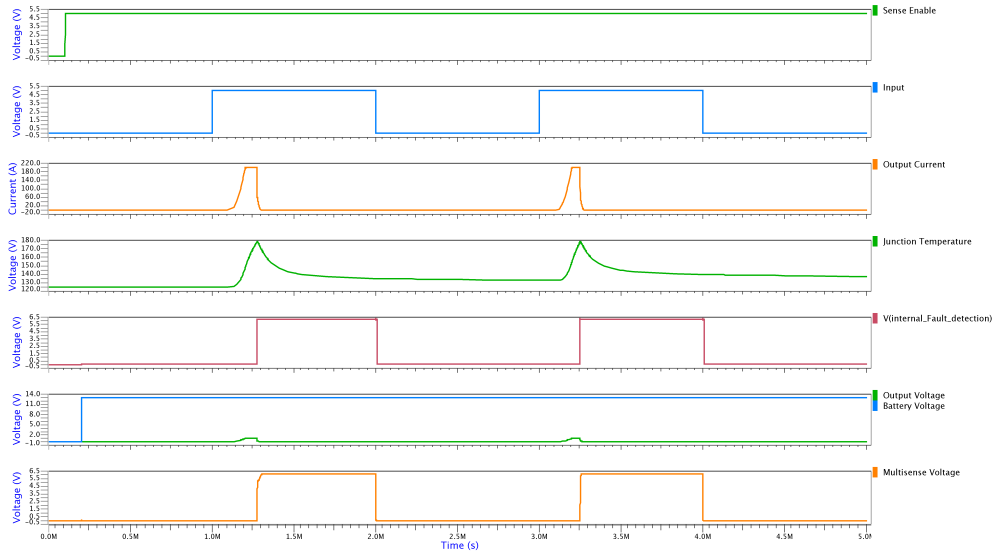


Figure 13. Latch functionality - behavior in hard short circuit condition



2.5 Electrical characteristics curves

Figure 14. OFF-state output current

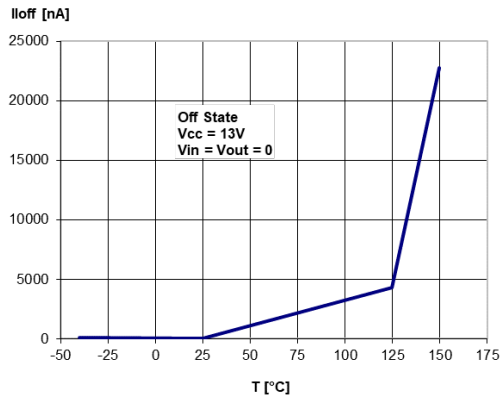


Figure 15. Standby current

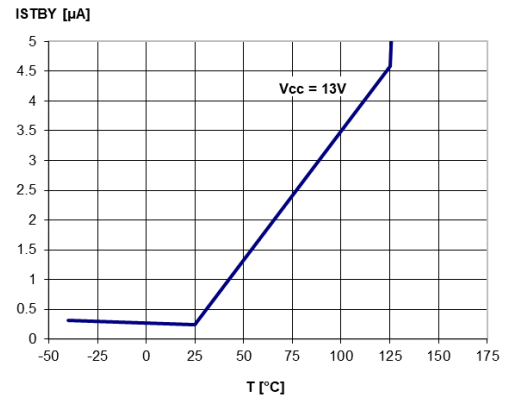


Figure 16. $I_{GND(ON)}$ vs. I_{out}

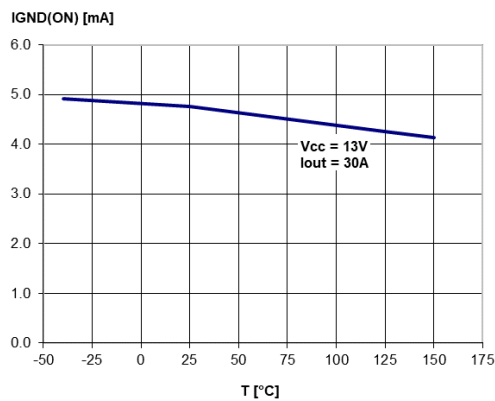


Figure 17. Logic input high level voltage

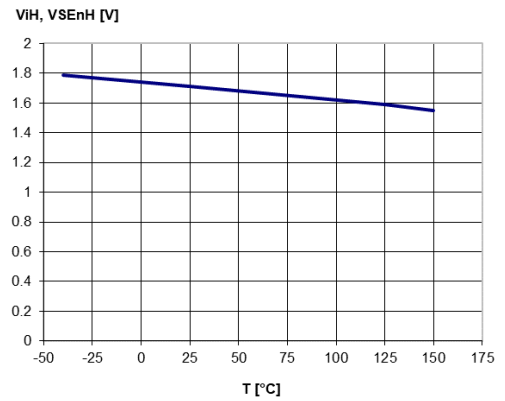


Figure 18. Logic input low level voltage

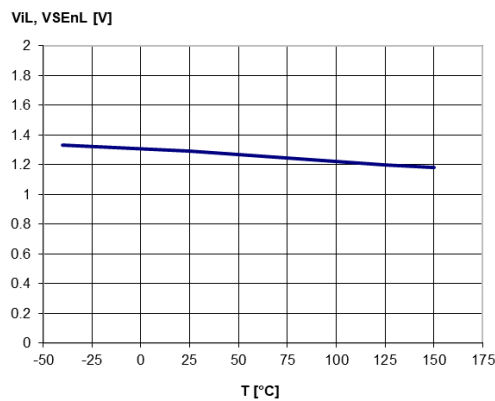


Figure 19. High level logic input current

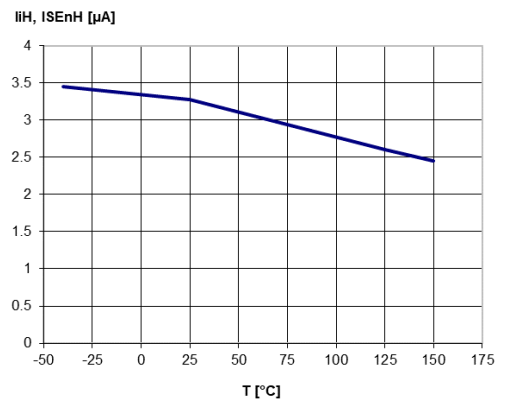


Figure 20. Low level logic input current

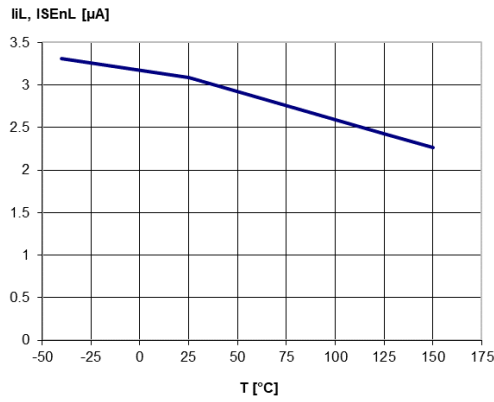


Figure 21. Logic input hysteresis voltage

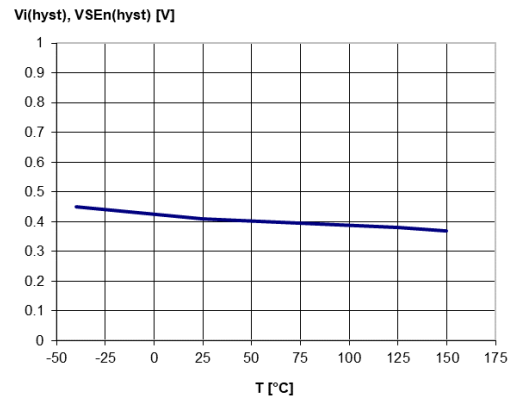


Figure 22. Undervoltage shutdown

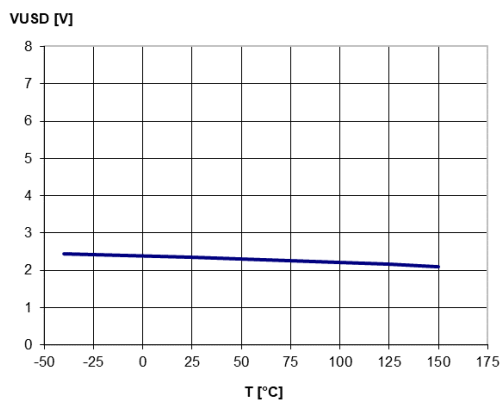


Figure 23. On-state resistance vs. T_{case}

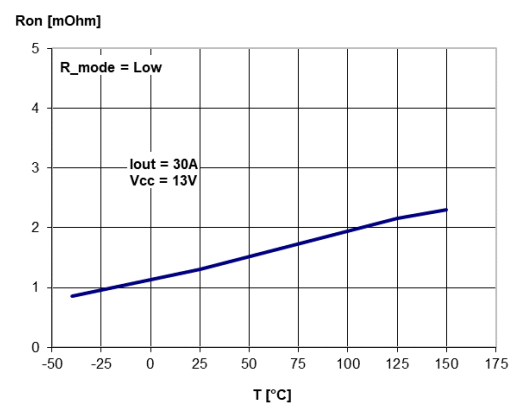


Figure 24. On-state resistance vs. V_{CC}

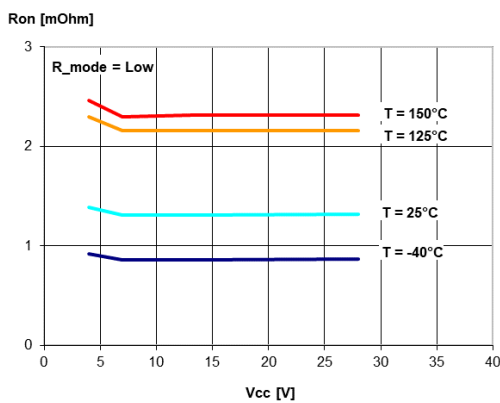


Figure 25. Turn-on voltage slope

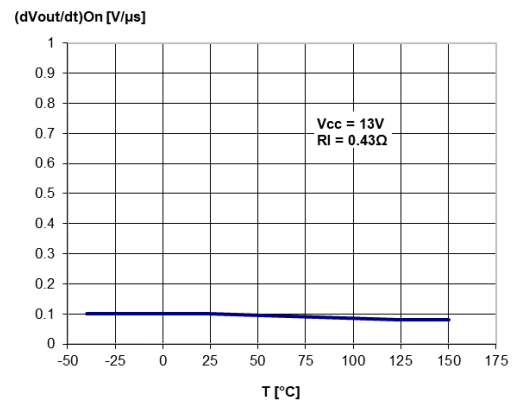


Figure 26. Turn-off voltage slope

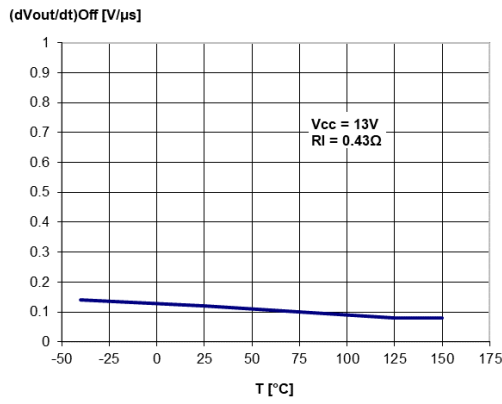


Figure 27. Won vs. T_{case}

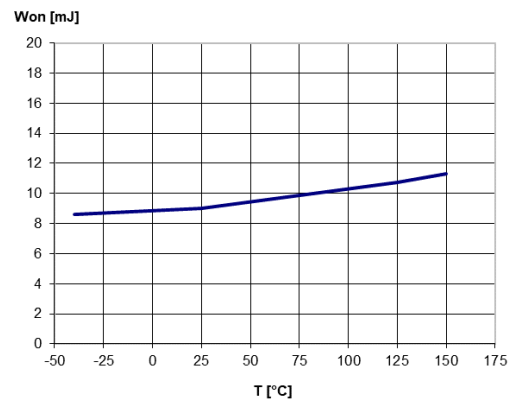


Figure 28. Woff vs. T_{case}

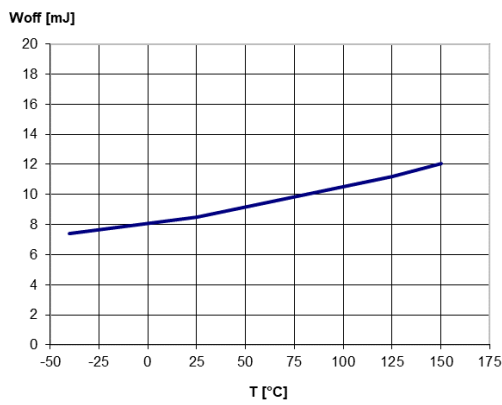


Figure 29. I_{LIMH} vs. T_{case}

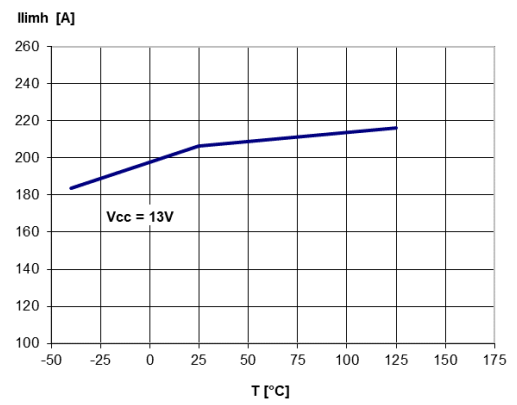


Figure 30. Turn-off output voltage clamp

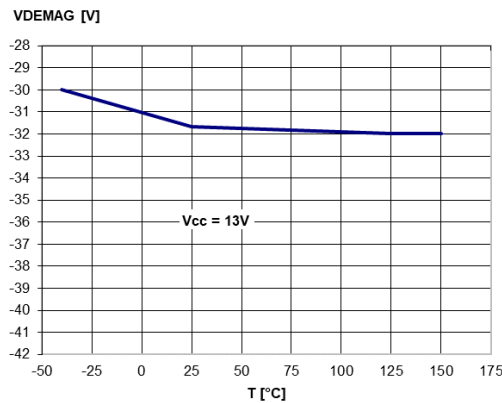
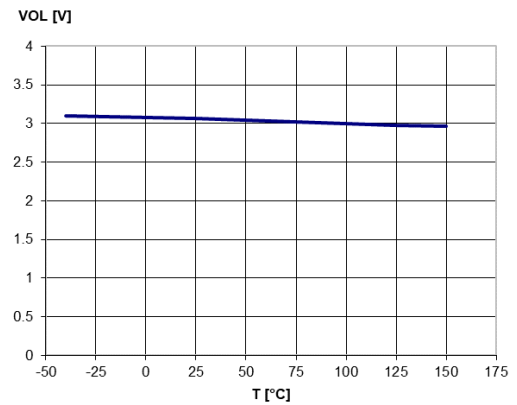
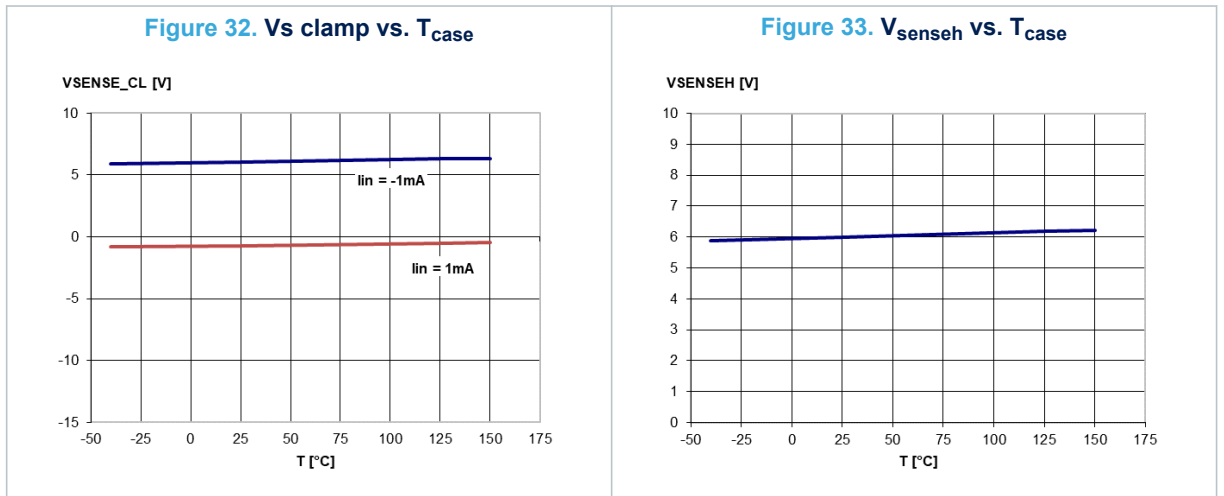


Figure 31. OFF-state open-load voltage detection threshold





3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered.

3.3 Current limitation

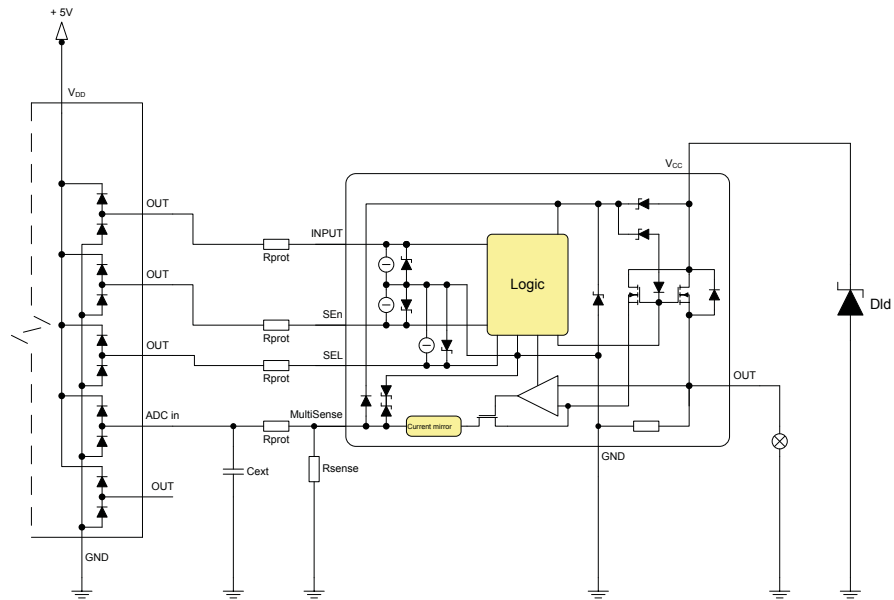
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

4 Application information

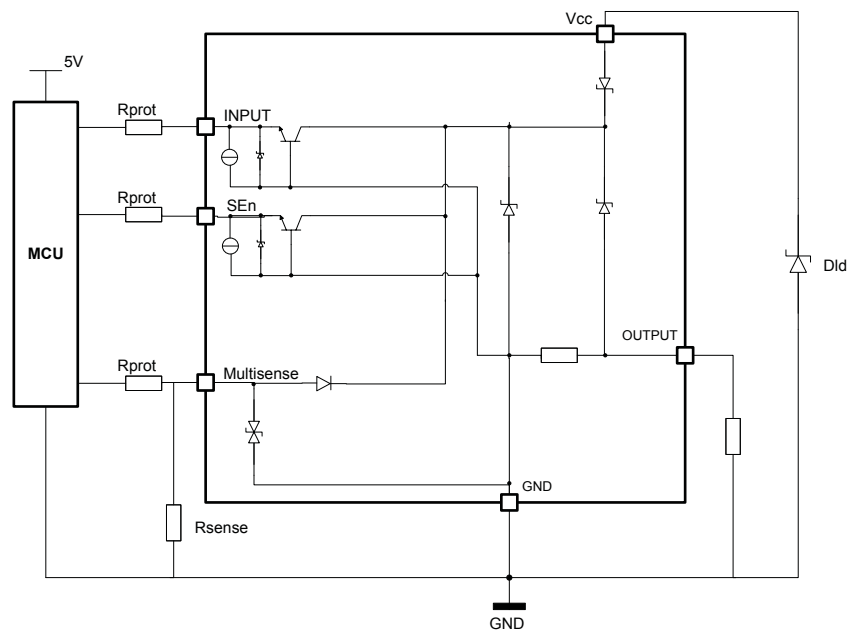
Figure 34. Application diagram



GADG0407191047LM

4.1 GND protection network against reverse battery

Figure 35. Simplified internal structure



GADG0407191059LM

The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 14. ISO 7637-2 - electrical transient conduction along supply line.](#)

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 14. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S ⁽¹⁾		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽²⁾	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40 V	5 pulse	1 min		400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

$$\text{For } V_{CCpeak} = -150 \text{ V; } I_{latchup} \geq 20 \text{ mA; } V_{OH\mu C} \geq 4.5 \text{ V}$$

$$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega.$$

Recommended values: $R_{prot} = 15 \text{ k}\Omega$

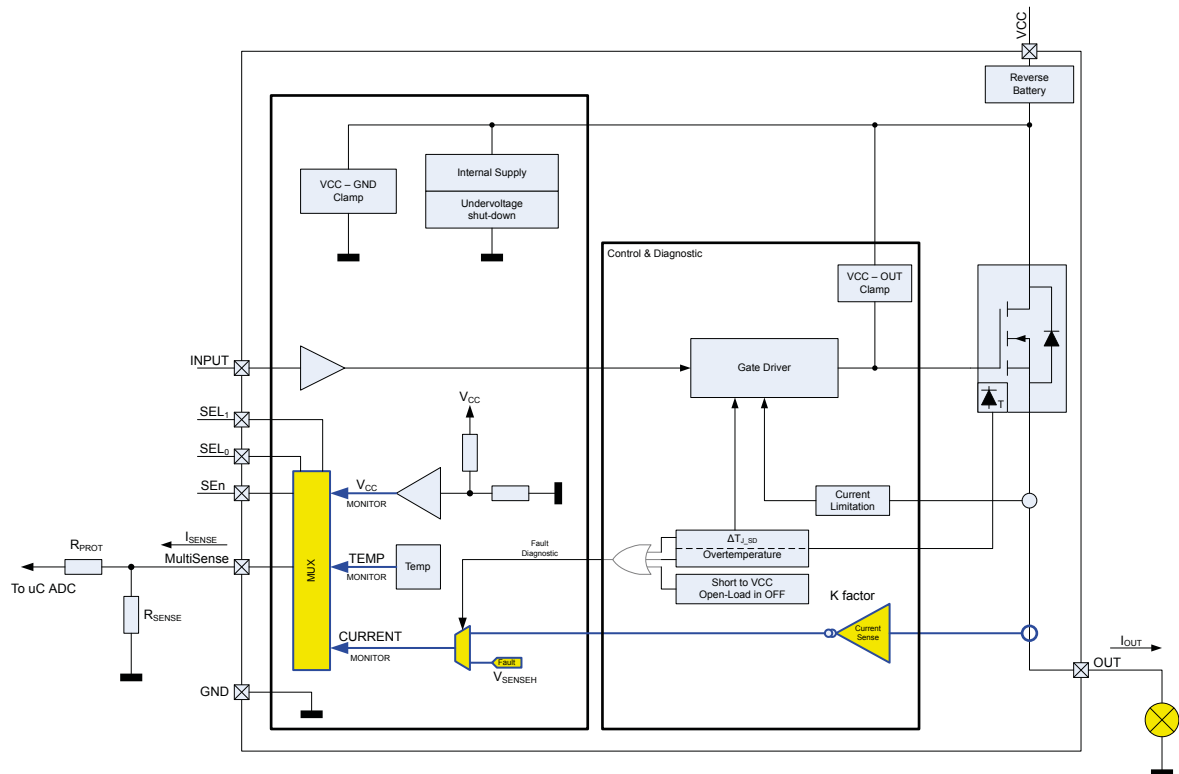
4.4 MultiSense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage proportional to V_{CC}
- T_{CASE} : voltage proportional to chip temperature

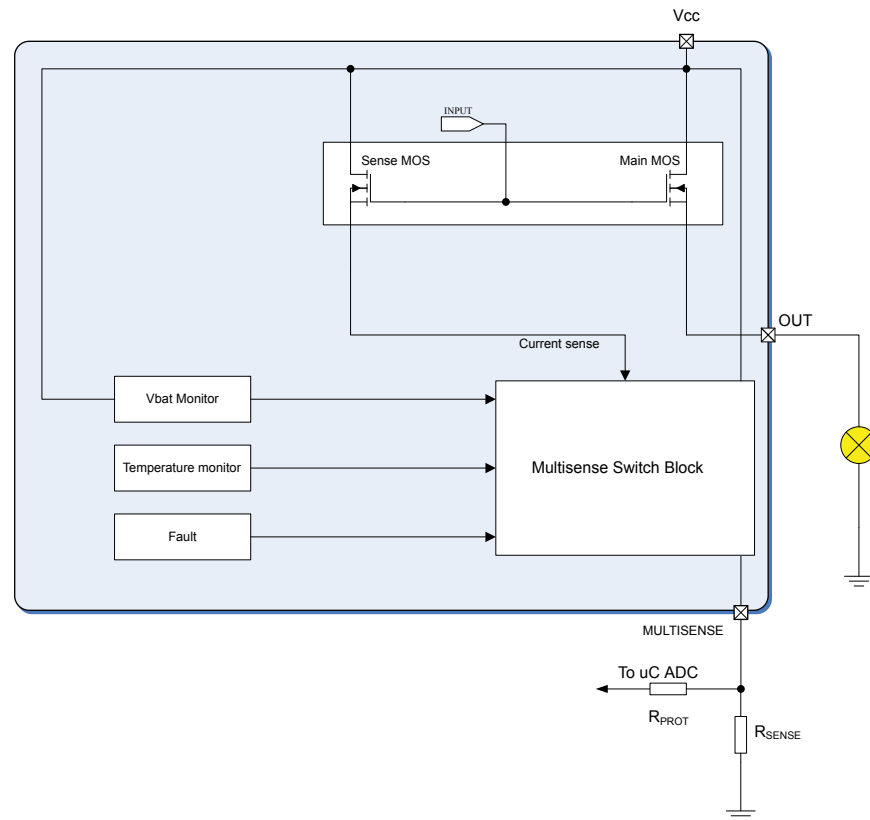
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 36. MultiSense and diagnostic – block diagram



4.4.1 Principle of MultiSense signal generation

Figure 37. MultiSense block diagram



GAPGCFT01040

Current monitor

When current mode is selected via MultiSense, this output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from MultiSense pin in current output mode
- I_{OUT} is the current flowing through output

Figure 39. Open-load / short to V_{CC} condition

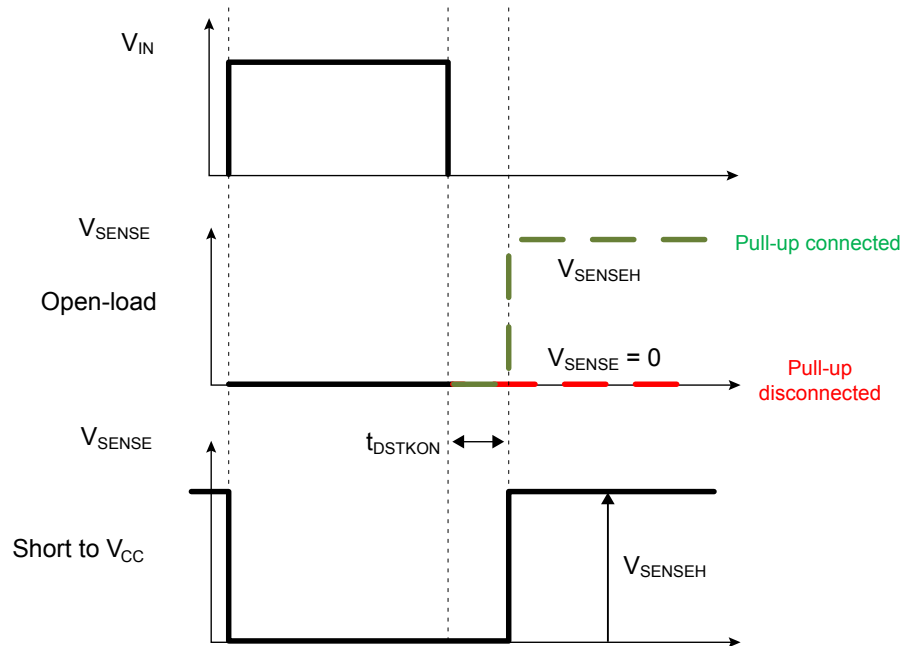


Table 15. MultiSense pin levels in off-state

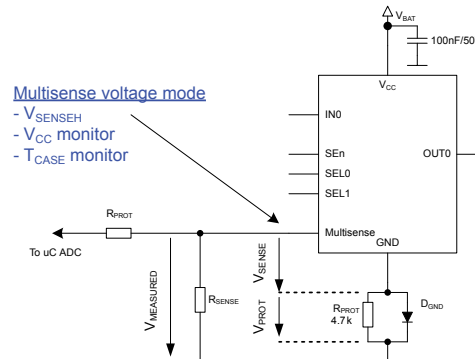
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
Short to V _{CC}	$V_{OUT} > V_{OL}$	0	H
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 T_{CASE} and V_{CC} monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection (optional) is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 1 shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 40. GND voltage shift



GADG0407191139LM

V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 8$.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$$

where $dV_{SENSE_TC} / dT \sim$ typically -5.5 mV/K (for temperature range $(-40$ °C to 150 °C)).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

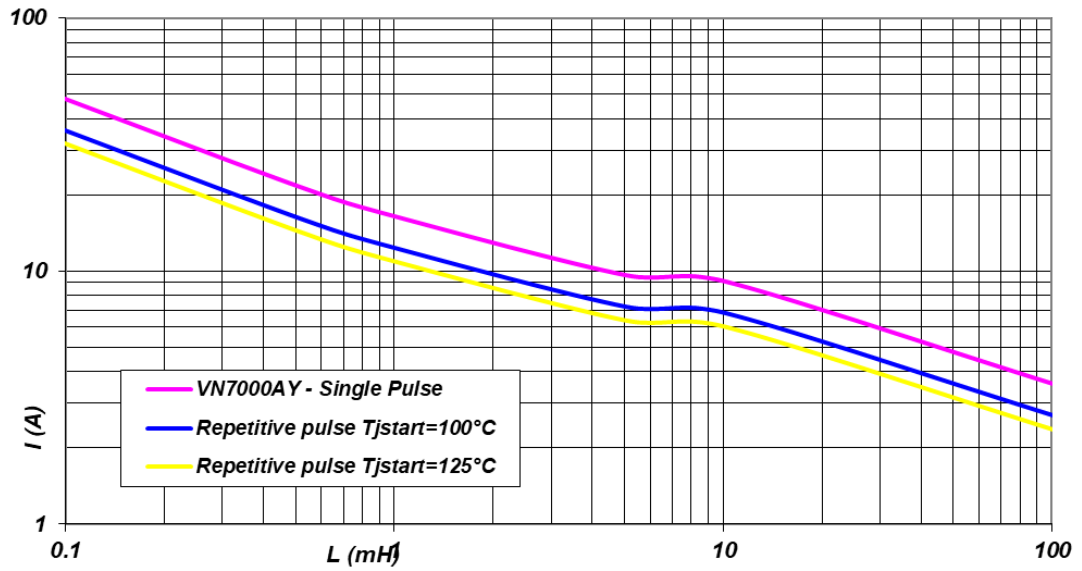
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off)min} @ 4V}$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 41. Maximum turn off current versus inductance



6 Package and PCB thermal data

6.1 PowerSSO-36 thermal data

Figure 42. PowerSSO-36 PC board

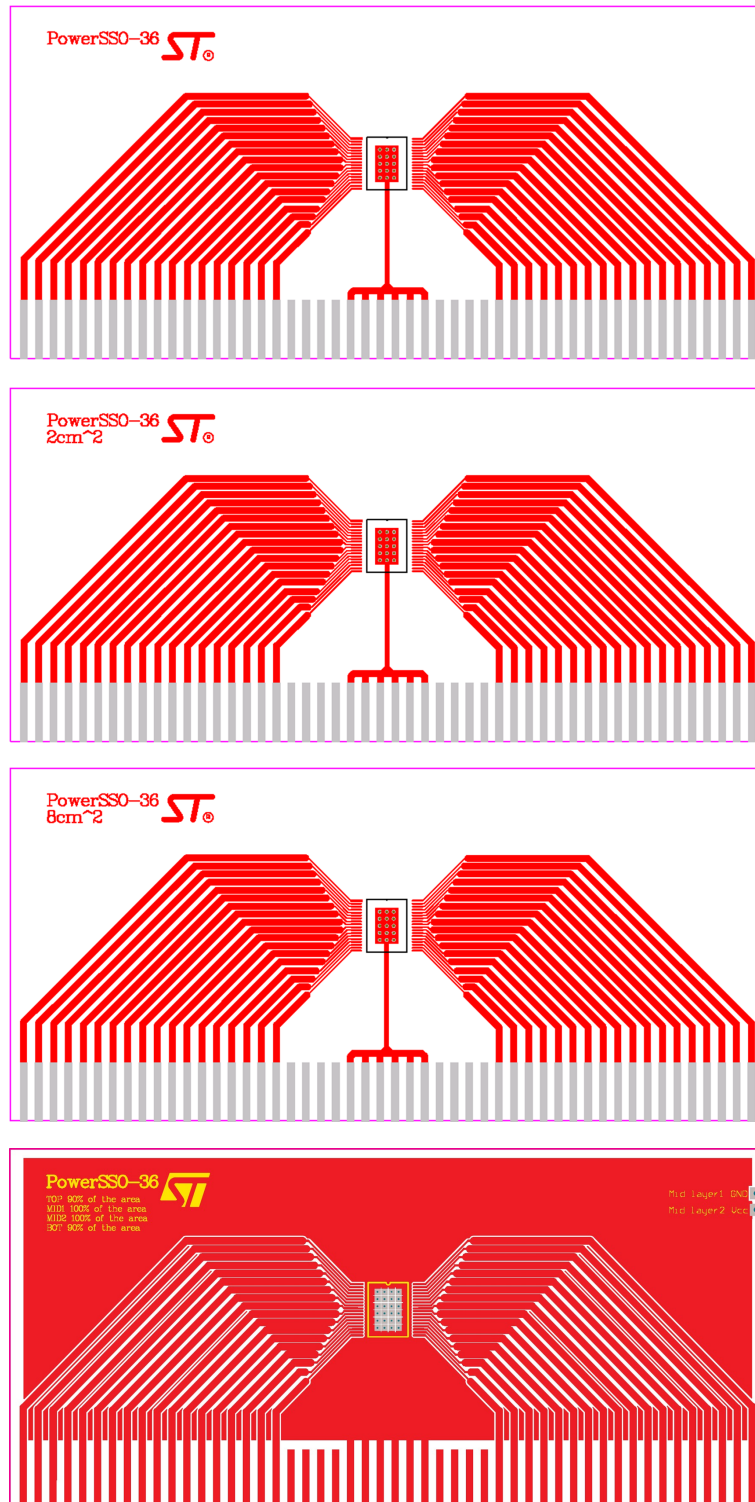
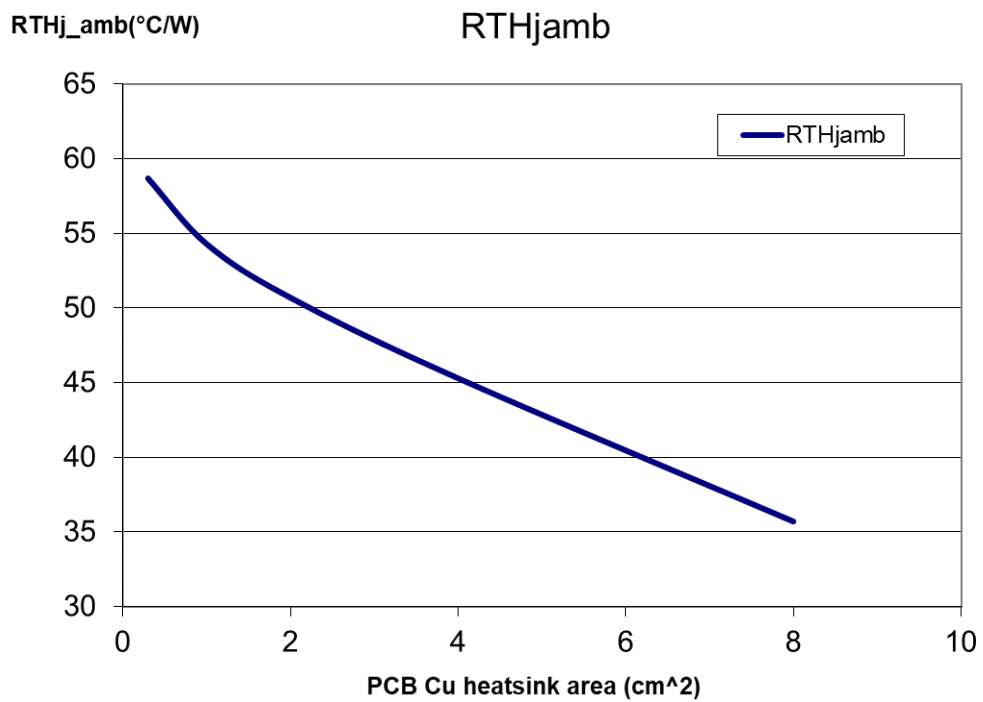


Table 16. PCB properties

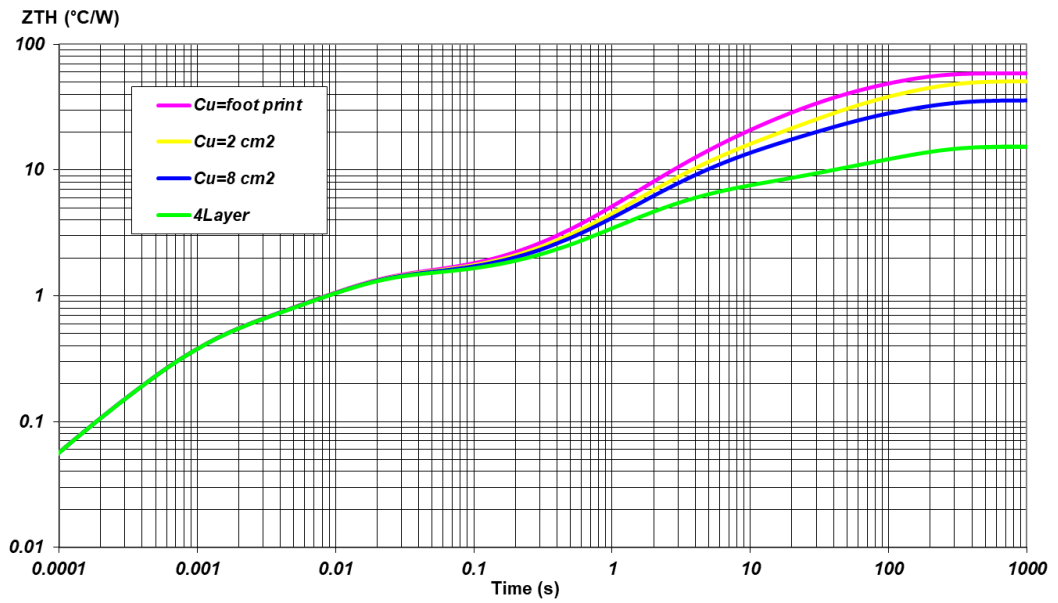
Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	4.1 mm x 6.5 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 43. $R_{thj-amb}$ vs PCB copper area in open box free air conditions



$R_{thj-amb}$ on 4Layer PCB: 15.3°C/W

Figure 44. Power SSO-36 thermal impedance junction ambient single pulse



Equation: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 45. Thermal fitting model

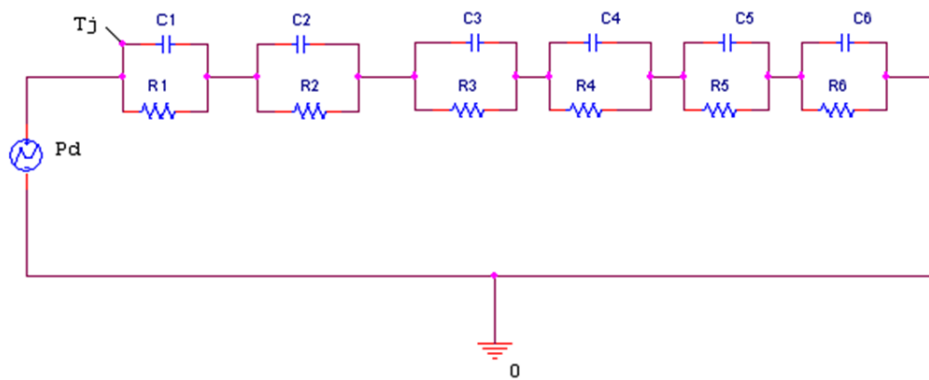


Table 17. Thermal parameters

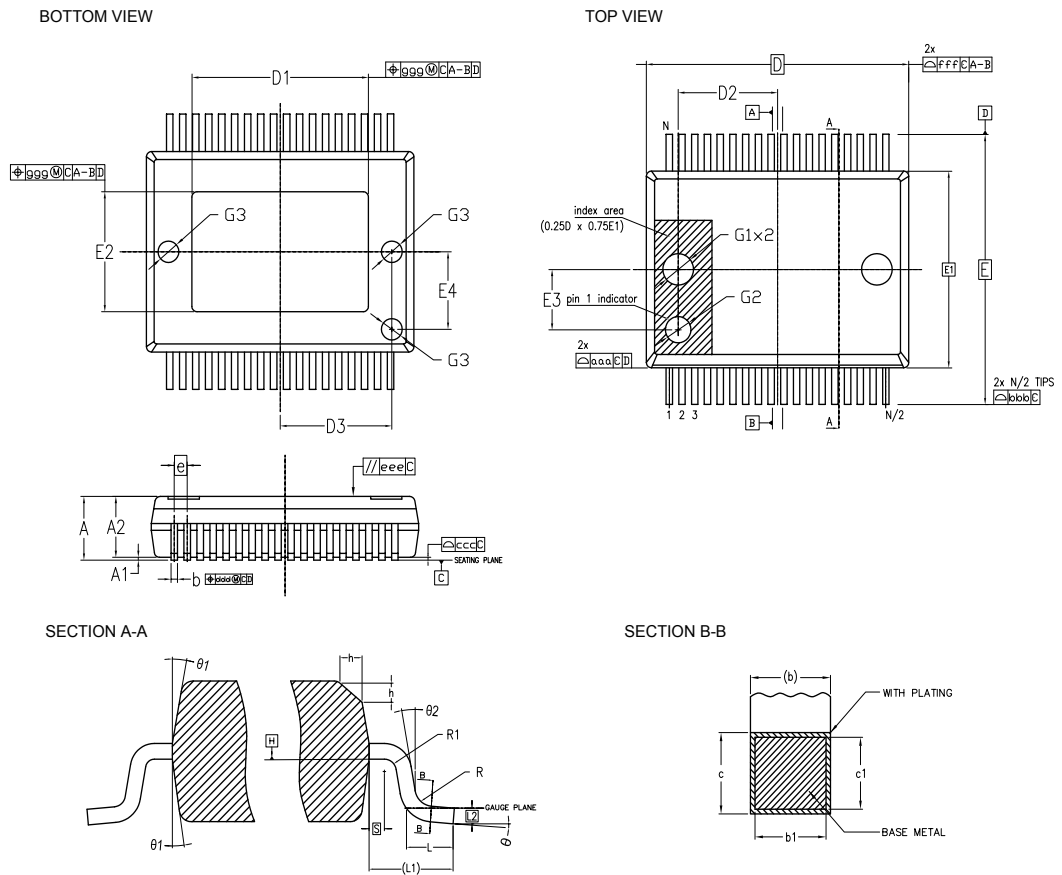
Area/island (cm ²)	FP	2	8	4L
R1 (°C/W)	0.4	-	-	-
R2 (°C/W)	1	-	-	-
R3 (°C/W)	3.4	3.4	3.4	2.2
R4 (°C/W)	6	6	6	2.8
R5 (°C/W)	18	14	10	2
R6 (°C/W)	30	26	15	7
C1 (W * s/°C)	0.002	-	-	-
C2 (W * s/°C)	0.01	-	-	-
C3 (W * s/°C)	0.3	0.6	0.6	0.6
C4 (W * s/°C)	0.8	0.8	0.9	1.2
C5 (W * s/°C)	1	2	3	10
C5 (W * s/°C)	3	5	9	18

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-36 package information

Figure 46. PowerSSO-36 package outline



GAPG2508150825CFT

Table 18. PowerSSO-36 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	5°		10°
Θ2	0°		
A	2.15		2.45
A1	0.00		0.10
A2	2.15		2.35
b	0.18		0.32
b1	0.13	0.25	0.30
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.90		7.50
D2		3.65	
D3		4.30	
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.30		5.20
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40 REF		
L2	0.25 BSC		
N	36		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
fff		0.20	
ggg		0.15	

7.2 PowerSSO-36 packing information

Figure 47. PowerSSO-36 reel 13"

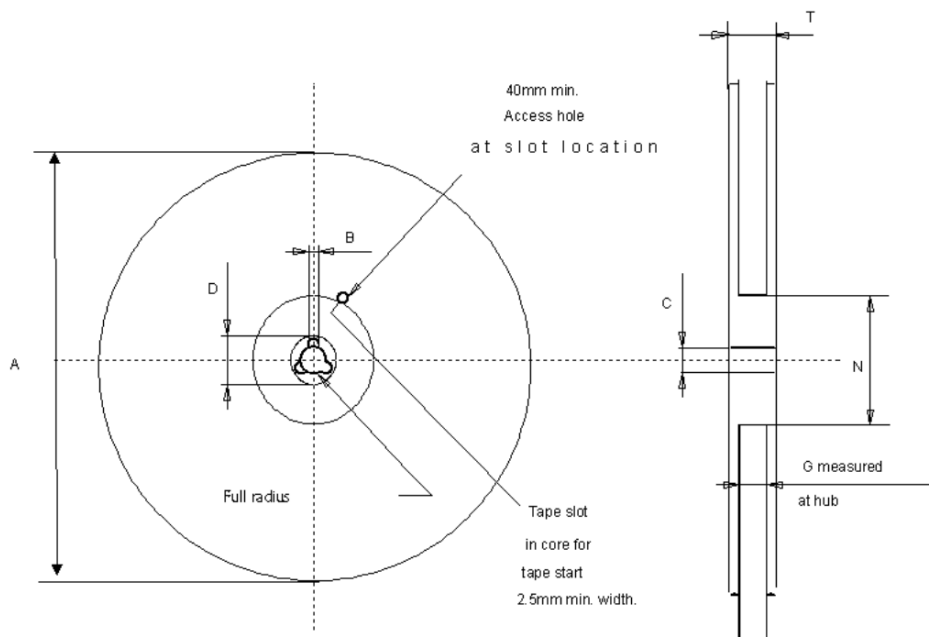
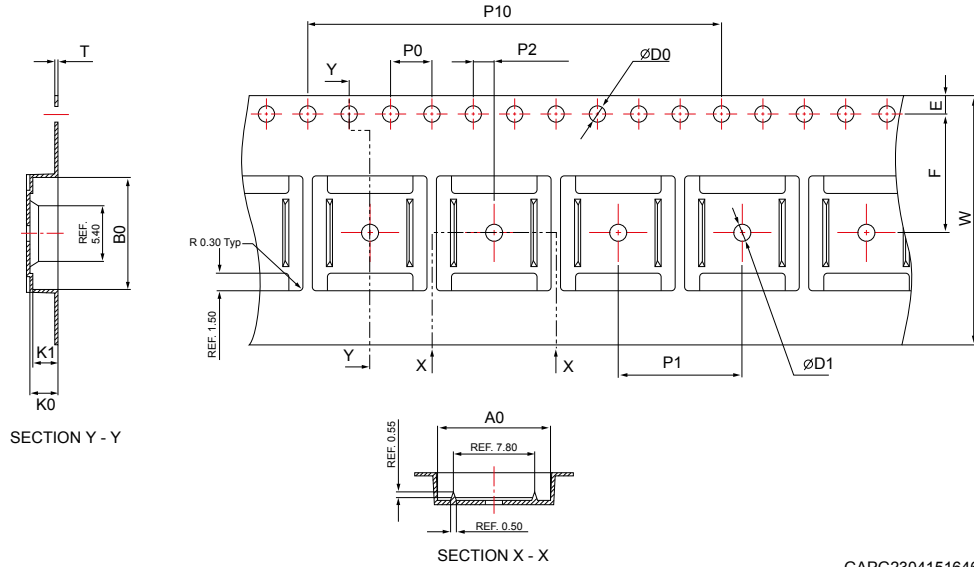


Table 19. Reel dimensions

Description	Value ⁽¹⁾
Base quantity	1000
Bulk quantity	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

1. All dimensions are in mm.

Figure 48. PowerSSO-36 carrier tape



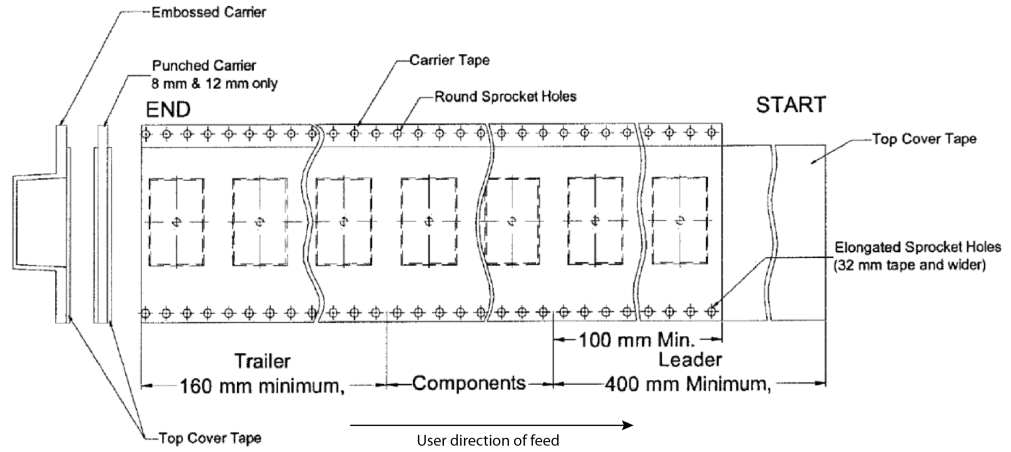
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Table 20. PowerSSO-36 carrier tape dimensions

Description	Value ⁽¹⁾
A ₀	10.90 ± 0.10
B ₀	10.80 ± 0.10
K ₀	2.75 ± 0.10
K ₁	2.45 ± 0.10
D ₀	1.50 (+0.10 / -0)
D ₁	1.60 ± 0.10
P ₀	4.00 ± 0.10
P ₁	12.00 ± 0.10
P ₂	2.00 ± 0.10
P ₁₀	40.00 ± 0.20
E	1.75 ± 0.10
F	11.50 ± 0.10
W	24.00 ± 0.30
T	0.30 ± 0.05

1. All dimensions are in mm.

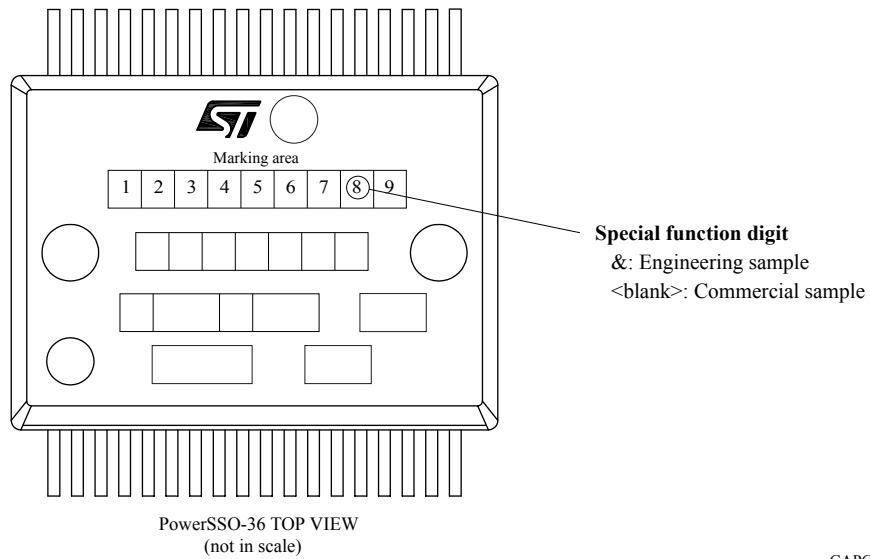
Figure 49. PowerSSO-36 schematic drawing of leader and trailer tape



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7.3 PowerSSO-36 marking information

Figure 50. PowerSSO-36 marking information



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Note: *Engineering Samples: Parts marked as “&” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.*
Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 21. Document revision history

Date	Revision	Changes
22-Feb-2016	1	Initial release.
10-Oct-2016	2	<p><i>Section "Features"</i></p> <ul style="list-style-type: none"> changed "Shutdown current" parameter name to "Current limitation" and value to 190 A changed $V_{USD_Cranking}$ value removed feature "Automotive qualified" changed I_{STBY} Max. value to 20 μA <p><i>Section "Description"</i></p> <ul style="list-style-type: none"> updated text <p><i>Table 1: "Pin functions"</i></p> <ul style="list-style-type: none"> updated FaultRST pin description <p><i>Table 3: "Absolute maximum ratings"</i></p> <ul style="list-style-type: none"> updated V_{CC}, V_{CCPK} and I_{SENSE} <p><i>Table 4: "Thermal data"</i></p> <ul style="list-style-type: none"> $R_{thj-board}$ parameter changed to $R_{thj-case}$ <p><i>Table 5: "Electrical characteristics during cranking"</i></p> <ul style="list-style-type: none"> updated $V_{USD_Cranking}$ and V_{USD} Max. values updated R_{ON_L}, R_{ON_H} and T_{TSD} Test conditions updated V_{clamp} <p><i>Table 6: "Power section"</i></p> <ul style="list-style-type: none"> changed I_{STBY} Max. value to 20 μA changed $I_{L(off)}$ Max. value to 20 μA <p><i>Table 7: "Switching"</i></p> <ul style="list-style-type: none"> added junction temperature to delay time and voltage slope Parameter descriptions updated T_{SKEW} values <p><i>Table 9: "Protections"</i></p> <ul style="list-style-type: none"> Changed I_{SD} parameter to I_{LIMH} added parameters I_{LIML} and ΔT_{J_SD} updated V_{SENSE_SAT}, I_{SENSE_SAT} and I_{OUT_SAT} junction temperature test conditions updated MultiSense timings (Multiplexer transition times) I_{OUT} test conditions <p>Reworked <i>Table 11: "Truth table"</i></p> <p><i>Table 12: "MultiSense multiplexer addressing"</i></p> <ul style="list-style-type: none"> added footnote to OFF-state diag. column heading <p>Reworked <i>Section 3: "Protections"</i></p> <p><i>Section 4.4.2: "TCASE and VCC monitor"</i></p> <ul style="list-style-type: none"> updated V_{SENSE} equation in V_{CC} monitor section
12-Jan-2017	3	<p>Added "Automotive qualified" cover page feature</p> <p><i>Figure 2. Configuration diagram (top view)</i></p> <ul style="list-style-type: none"> updated pins 26 to 30 <p><i>Table 6. Power section</i></p> <ul style="list-style-type: none"> removed $R_{ON_REV_H}$ changed $R_{ON_REV_L}$ symbol to R_{ON_REV} and updated parameter description added $I_{S(ON)}$ test condition: $V_{R_mode} = 0$ V added $I_{GND(ON)}$ test condition: $V_{R_mode} = 0$ V

Date	Revision	Changes
12-Jan-2017	3 (continued)	<p><i>Table 7. Switching (R_mode = Low)</i></p> <ul style="list-style-type: none"> Updated title (was "Switching") <p><i>Table 8. Switching (R_mode = High)</i></p> <p>Added</p> <ul style="list-style-type: none"> updated I_{LIMH} Min., Typ. and Max. values updated I_{LIML} Typ. values updated ΔT_{J_SD} and t_{LATCH_RST} test conditions <p><i>Table 11. MultiSense</i></p> <ul style="list-style-type: none"> updated V_{SENSE_SAT} test conditions
28-Mar-2018	4	<p><i>Table 6. Power section</i></p> <ul style="list-style-type: none"> Inserted max value "12" for R_{ON_H} parameter Inserted max value "3" for R_{ON_L} parameter <p><i>Table 7. Switching (R_mode = Low)</i></p> <ul style="list-style-type: none"> updated Typ. values <p><i>Table 8. Switching (R_mode = High)</i></p> <ul style="list-style-type: none"> updated Typ. values <p><i>Table 11. MultiSense</i></p> <ul style="list-style-type: none"> updated Min. Typ. and Max. values <p><i>Table 13. MultiSense multiplexer addressing</i></p> <ul style="list-style-type: none"> Updated I_{SENSE} with V_{SENSE}.
28-Jan-2019	5	<p>Updated features in cover page.</p> <p>Updated:</p> <ul style="list-style-type: none"> Figure 3. Current and voltage conventions Table 3. Absolute maximum ratings Table 6. Power section Table 7. Switching (R_mode = Low) Table 8. Switching (R_mode = High) Table 9. Logic inputs Table 10. Protections Table 11. MultiSense <p>Minor text changes.</p>
01-Aug-2019	6	<p>Updated features and description in cover page.</p> <p>Updated:</p> <ul style="list-style-type: none"> Figure 1. Block diagram Figure 2. Configuration diagram (top view) Figure 3. Current and voltage conventions Figure 10. Multisense timings (chip temperature and V_{CC} sense mode) Figure 34. Application diagram Figure 35. Simplified internal structure Figure 36. MultiSense and diagnostic – block diagram Figure 38. Analog HSD – open-load detection in off-state Figure 40. GND voltage shift Table 1. Pin functions Table 2. Suggested connections for unused and not connected pins Table 3. Absolute maximum ratings Table 6. Power section Table 7. Switching (R_mode = Low) Table 9. Logic inputs

Date	Revision	Changes
01-Aug-2019	6 (continued)	<ul style="list-style-type: none"> • Table 10. Protections • Table 11. MultiSense • Table 12. Truth table • Table 13. MultiSense multiplexer addressing • Section 6.1 PowerSSO-36 thermal data Minor text changes.
14-Jan-2020	7	Updated features in cover page. Updated: <ul style="list-style-type: none"> • Table 2. Suggested connections for unused and not connected pins • Table 3. Absolute maximum ratings • Table 4. Thermal data • Table 6. Power section • Table 7. Switching ($R_{mode} = Low$) • Table 14. ISO 7637-2 - electrical transient conduction along supply line • Table 11. MultiSense • Section 6.1 PowerSSO-36 thermal data Added: <ul style="list-style-type: none"> • Figure 4. IOOUT/ISENSE vs. IOOUT - High $R_{DS(on)}$ mode • Figure 5. Current sense precision vs. IOOUT - High $R_{DS(on)}$ mode • Figure 6. IOOUT/ISENSE vs. IOOUT - Low $R_{DS(on)}$ mode • Figure 7. Current sense precision vs. IOOUT - Low $R_{DS(on)}$ mode • Section 2.4 Waveforms • Section 2.5 Electrical characteristics curves • Section 5 Maximum demagnetization energy ($V_{CC} = 16 V$) Minor text changes.

Contents

1	Block diagram and pin description	3
2	Electrical specification	5
2.1	Absolute maximum ratings	5
2.2	Thermal data	6
2.3	Main electrical characteristics	6
2.4	Waveforms	19
2.5	Electrical characteristics curves	19
3	Protections	24
3.1	Power limitation	24
3.2	Thermal shutdown	24
3.3	Current limitation	24
3.4	Negative voltage clamp	24
4	Application information	25
4.1	GND protection network against reverse battery	25
4.2	Immunity against transient electrical disturbances	26
4.3	MCU I/Os protection	26
4.4	Multisense - analog current sense	26
4.4.1	Principle of MultiSense signal generation	27
4.4.2	T _{CASE} and V _{CC} monitor	30
4.4.3	Short to VCC and OFF-state open-load detection	31
5	Maximum demagnetization energy (VCC = 16 V)	32
6	Package and PCB thermal data	33
6.1	PowerSSO-36 thermal data	33
7	Package information	37
7.1	PowerSSO-36 package information	37
7.2	PowerSSO-36 packing information	39
7.3	PowerSSO-36 marking information	41
	Revision history	42

List of tables

Table 1.	Pin functions	3
Table 2.	Suggested connections for unused and not connected pins	4
Table 3.	Absolute maximum ratings	5
Table 4.	Thermal data	6
Table 5.	Electrical characteristics during cranking	6
Table 6.	Power section	7
Table 7.	Switching (R_mode = Low)	7
Table 8.	Switching (R_mode = High)	8
Table 9.	Logic inputs	9
Table 10.	Protections	10
Table 11.	MultiSense	10
Table 12.	Truth table	17
Table 13.	MultiSense multiplexer addressing	18
Table 14.	ISO 7637-2 - electrical transient conduction along supply line	26
Table 15.	MultiSense pin levels in off-state	30
Table 16.	PCB properties	34
Table 17.	Thermal parameters	36
Table 18.	PowerSSO-36 mechanical data	38
Table 19.	Reel dimensions	39
Table 20.	PowerSSO-36 carrier tape dimensions	40
Table 21.	Document revision history	42

List of figures

Figure 1.	Block diagram	3
Figure 2.	Configuration diagram (top view).	4
Figure 3.	Current and voltage conventions.	5
Figure 4.	IOUT/ISENSE vs. IOUT - High $R_{DS(ON)}$ mode	13
Figure 5.	Current sense precision vs. IOUT - High $R_{DS(ON)}$ mode	14
Figure 6.	IOUT/ISENSE vs. IOUT - Low $R_{DS(ON)}$ mode	14
Figure 7.	Current sense precision vs. IOUT - Low $R_{DS(ON)}$ mode	15
Figure 8.	Switching time and Pulse skew	15
Figure 9.	MultiSense timings (current sense mode).	16
Figure 10.	Multisense timings (chip temperature and V_{CC} sense mode).	16
Figure 11.	T_{DSTKON}	17
Figure 12.	Latch functionality - behavior in hard short circuit condition ($T_{AMB} \ll T_{TSD}$)	19
Figure 13.	Latch functionality - behavior in hard short circuit condition.	19
Figure 14.	OFF-state output current	20
Figure 15.	Standby current	20
Figure 16.	$I_{GND(ON)}$ vs. I_{out}	20
Figure 17.	Logic input high level voltage	20
Figure 18.	Logic input low level voltage	20
Figure 19.	High level logic input current.	20
Figure 20.	Low level logic input current	21
Figure 21.	Logic input hysteresis voltage	21
Figure 22.	Undervoltage shutdown	21
Figure 23.	On-state resistance vs. T_{case}	21
Figure 24.	On-state resistance vs. V_{CC}	21
Figure 25.	Turn-on voltage slope	21
Figure 26.	Turn-off voltage slope	22
Figure 27.	W_{on} vs. T_{case}	22
Figure 28.	W_{off} vs. T_{case}	22
Figure 29.	I_{LIMH} vs. T_{case}	22
Figure 30.	Turn-off output voltage clamp	22
Figure 31.	OFF-state open-load voltage detection threshold	22
Figure 32.	V_s clamp vs. T_{case}	23
Figure 33.	V_{senseh} vs. T_{case}	23
Figure 34.	Application diagram.	25
Figure 35.	Simplified internal structure	25
Figure 36.	MultiSense and diagnostic – block diagram	27
Figure 37.	MultiSense block diagram	28
Figure 38.	Analog HSD – open-load detection in off-state	29
Figure 39.	Open-load / short to V_{CC} condition	30
Figure 40.	GND voltage shift	31
Figure 41.	Maximum turn off current versus inductance.	32
Figure 42.	PowerSSO-36 PC board	33
Figure 43.	$R_{thj-amb}$ vs PCB copper area in open box free air conditions	34
Figure 44.	Power SSO-36 thermal impedance junction ambient single pulse	35
Figure 45.	Thermal fitting model.	35
Figure 46.	PowerSSO-36 package outline	37
Figure 47.	PowerSSO-36 reel 13"	39
Figure 48.	PowerSSO-36 carrier tape	40
Figure 49.	PowerSSO-36 schematic drawing of leader and trailer tape	41
Figure 50.	PowerSSO-36 marking information	41

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