ASA65R550E, ASU65R550E, ASD65R550E, ASE65R550E

MOSFET Silicon N-Channel MOS

1. Applications

Boost PFC switch,single-ended flyback or two-transistor forward topologies.
PD Adaptor,LCD & PDP TV and LED lighting.

2. Features

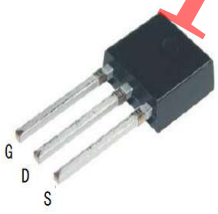
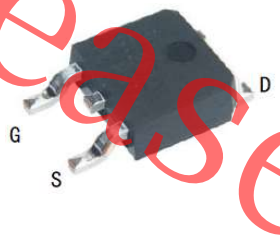
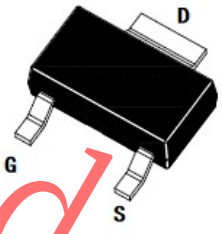
Low drain-source on-resistance: RDS(ON) = 0.50Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.8 to 4.2 V

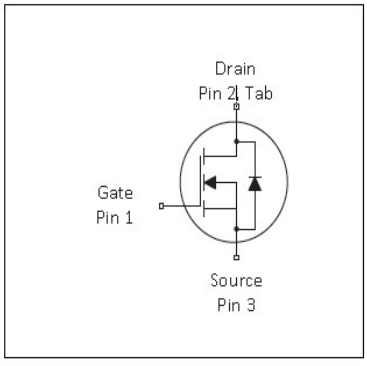
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @$T_{j,max}$	700	V
$R_{DS(on),max}$	550	m Ω
$Q_{g,typ}$	8.0	nC
$I_{D,pulse}$	24	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA65R550E	TO220F	ASA65R550E
ASU65R550E	TO251	ASU65R550E
ASD65R550E	TO252	ASD65R550E
ASE65R550E	SOT223	ASE65R550E

TO220F	TO251	TO252	SOT223
			



1 Maximum ratings

at T_j= 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuousdraincurrent[1]	I_D		-	8	A	T_C=25°C
Pulseddraincurrent[2]	$I_{D,pulse}$	-	-	24	A	T_C=25°C
Avalancheenergy,singlepulse	E_{AS}	-	-	624	mJ	Tc=25°C,VDD=50V,L = 10mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	7	A	Tc=25°C,VDD=50V,L = 10mH, RG=25Ω
MOSFETdv/dtruggedness	dv/dt	-	-	15	V/ns	V_{DS}=0...400V
Gate sourcevoltage (static)	V_{GS}	-20	-	20	V	static;
Gate sourcevoltage (dynamic)	V_{GS}	-30	-	30	V	AC(f>1Hz)
Power dissipation (TO220F)	P_{tot}	-	-	28	W	T_C=25°C
Power dissipation (TO252&TO251)	P_{tot}	-	-	63	W	T_C=25°C
Power dissipation (SOT223)	P_{tot}	-	-	7	W	T_C=25°C
Storagetemperature	T_{stg}	-55	-	150	°C	
Operatingjunctiontemperature	T_j	-55	-	150	°C	
Reversediode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V,I_{SD}<=48A,T_j=25°C seetable8

[1] LimitedbyT$_{j,max}$.MaximumDutyCycleD=0.50
[2] Pulsewidtht$_p$ limitedbyT$_{j,max}$
[3] IdenticallowsideandhighsideswitchwithidenticalR$_G$

2 Thermal characteristics

Table 3 Thermalcharacteristics (TO220 FullPAK)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

Thermalcharacteristics (TO251 and TO252)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Thermalcharacteristics (SOT223)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction -solder point	R_{thJC}	-	-	18	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	160	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C,unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-sourcebreakdownvoltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V,I_D=10mA
Gate thresholdvoltage	$V_{(GS)th}$	2.8		4.2	V	V_{DS}=V_{GS},I_D=250uA
Zerogate voltage draincurrent	I_{DSS}	-	-	100	nA	V_{DS}=650V,V_{GS}=0V,T_j=25°C
Gate-sourceleakagecurrent	I_{GSS}	-	-	100	nA	V_{GS}=30V,V_{DS}=0V
Drain-sourceon-stateresistance	$R_{DS(on)}$	-	0.50	0.55	Ω	V_{GS}=10V,I_D=4A,T_j=25°C
Gate resistance	R_G	-	25	-		f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Inputcapacitance	C_{iss}	-	599	-	pF	V_{GS}=0V,V_{DS}=50V,f=10kHz
Output capacitance	C_{oss}	-	76	-	pF	V_{GS}=0V,V_{DS}=50V,f=10kHz
Reverse transfer capacitance	C_{rss}	-	3.55	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-ondelaytime	$t_{d(on)}$	-	26.8	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=3A, R_G=6.8Ω;see table 9
Risetime	t_r	-	24.8	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=3A, R_G=6.8Ω;see table 9
Turn-offdelaytime	$t_{d(off)}$	-	127.6	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=3A, R_G=6.8Ω;see table 9
Falltime	t_f	-	21.2	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=3A, R_G=6.8Ω;see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate tosourcecharge	Q_{gs}	-	2.6	-	nC	V_{DD}=400V, I_D=3A, V_{GS}=0 to 10V
Gate todraincharge	Q_{gd}	-	1.7	-	nC	V_{DD}=400V, I_D=3A, V_{GS}=0 to 10V
Gate chargetotal	Q_g	-	8.0	-	nC	V_{DD}=400V, I_D=3A, V_{GS}=0 to 10V
Gate plateauvoltage	$V_{plateau}$	-	6.6	-	V	V_{DD}=400V, I_D=3A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diodeforwardvoltage	V_{SD}	-	0.76	-	V	V_{GS}=0V,I_F=1A,T_j=25°C
Reverserecoverytime	t_{rr}	-	174	-	ns	V_R=400V, I_F=3 A, di_F/dt=100A/μs; see table 8
Reverserecoverycharge	Q_{rr}	-	1.2	-	uC	V_R=400V, I_F=3 A, di_F/dt=100A/μs; see table 8
Peakreverserecoverycurrent	I_{rrm}	-	13.5	-	A	V_R=400V, I_F=3 A, di_F/dt=100A/μs; see table 8

4 Electrical characteristics diagram

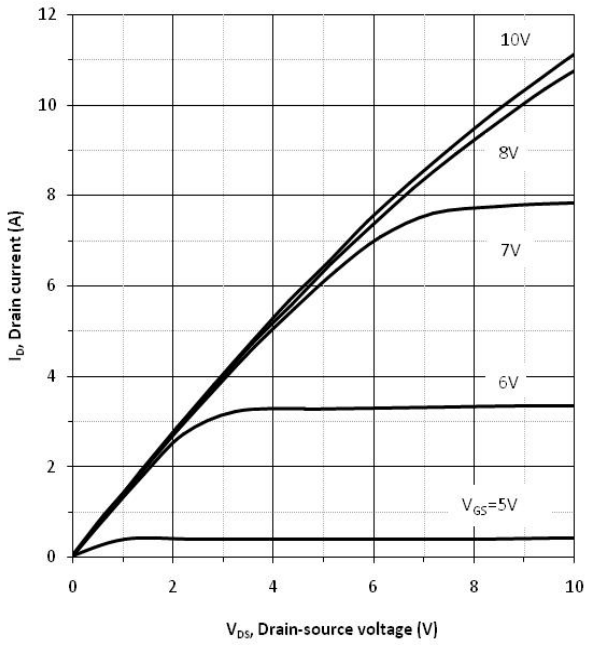
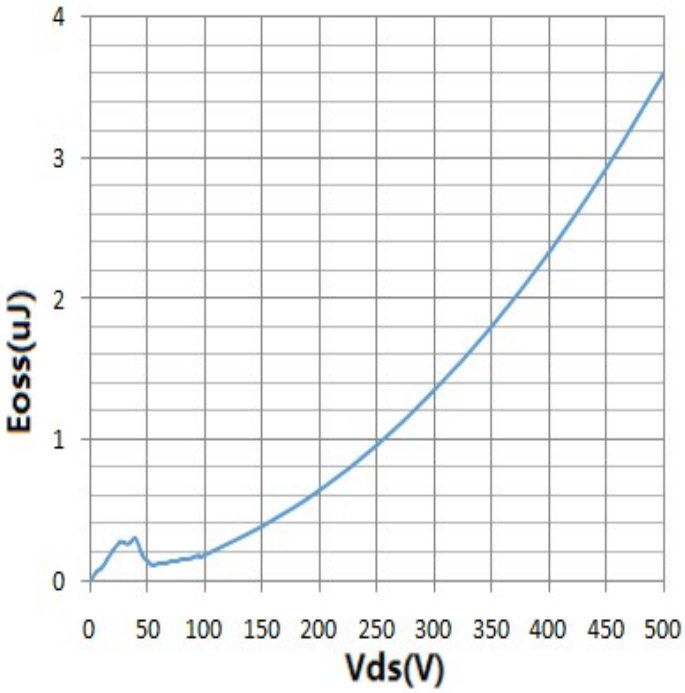
Diagram 1: Typ. output characteristics	Diagram 2: Typ. Coss stored energy
	
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}	*Eoss=f(VDS)*

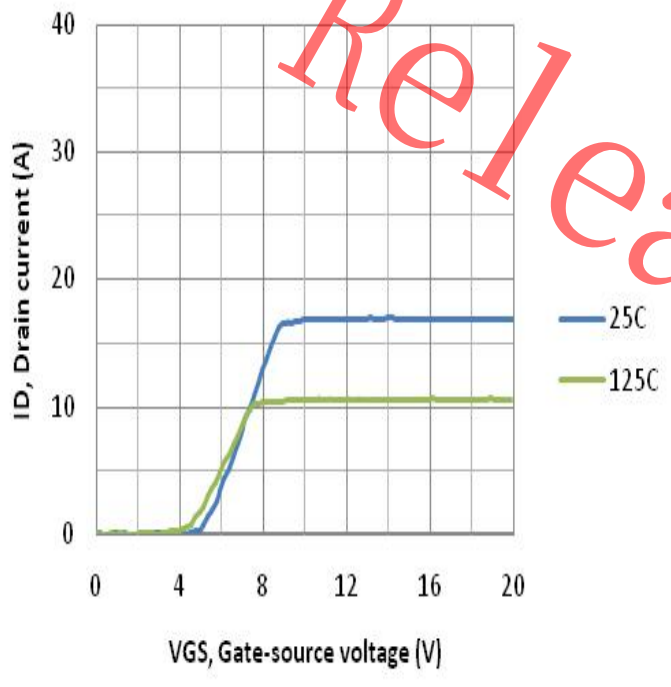
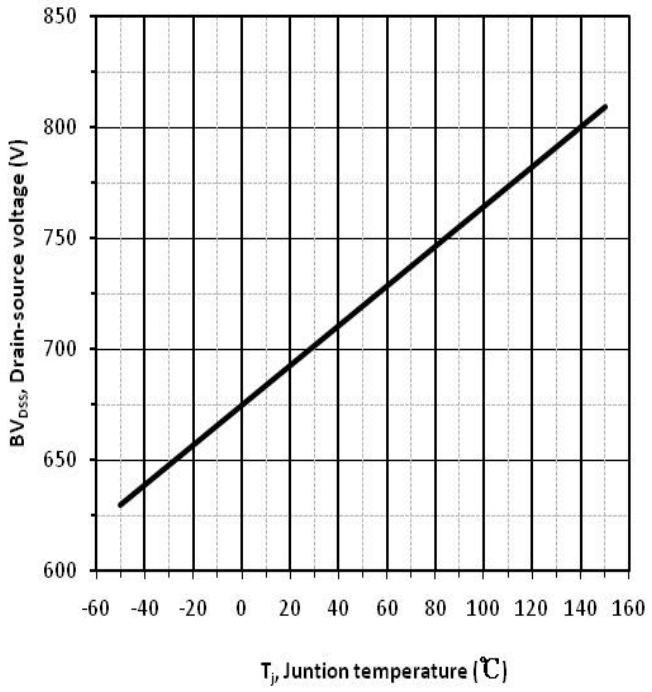
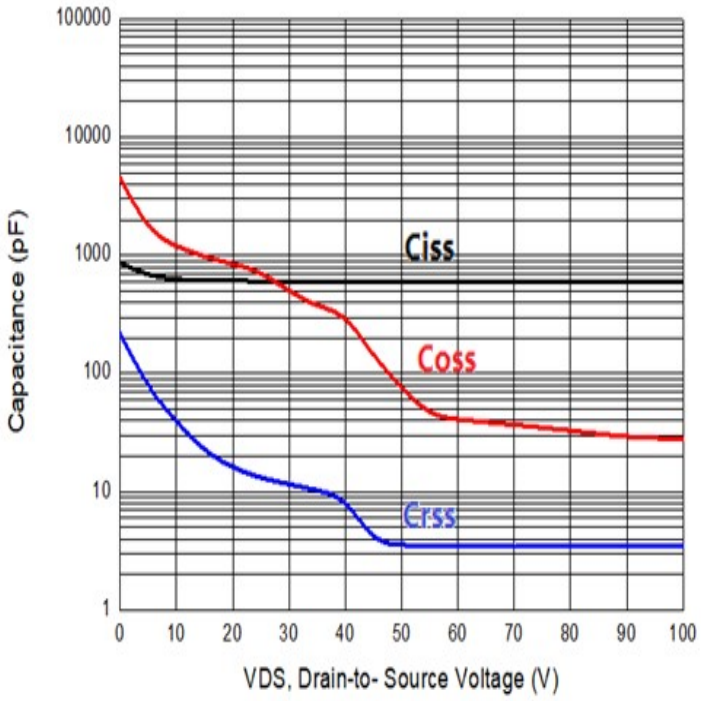
Diagram 3: Typ. transfer characteristics	Diagram 4: Typ. gate charge
	
I_D=f(V_{GS});parameter: T_j	V_{GS}=f(Q_{gate});I_D=3A pulsed; parameter: V_{DD}

Diagram 5: Drain-source breakdown voltage	Diagram 6: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j);I_D=10mA	C=f(V_{DS});V_{GS}=0V; f=10 kHz

5 Test Circuits

Table 8 Diodecharacteristics

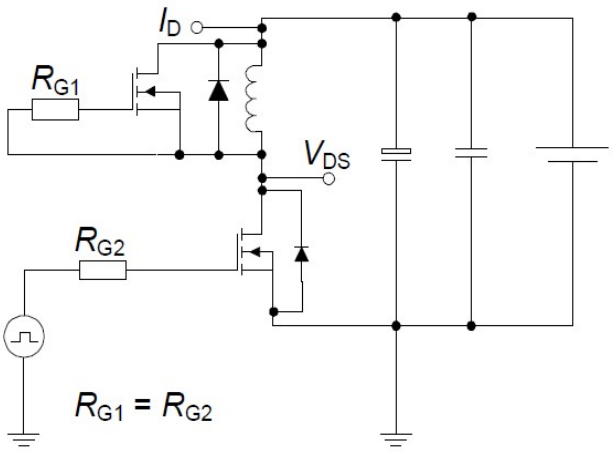
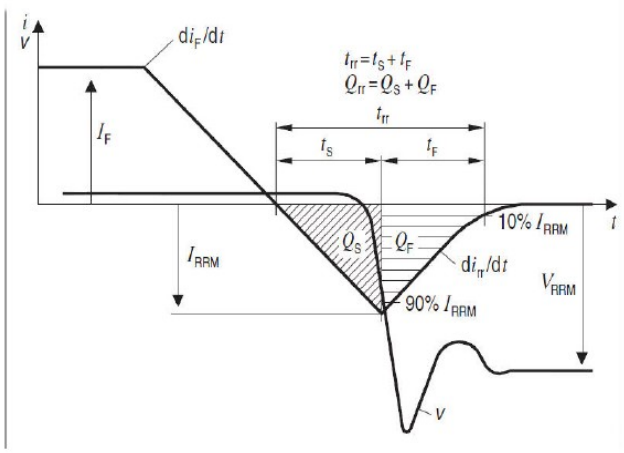
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switchingtimes

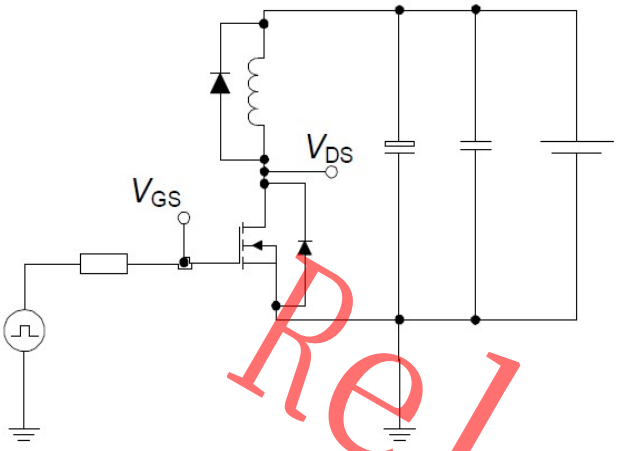
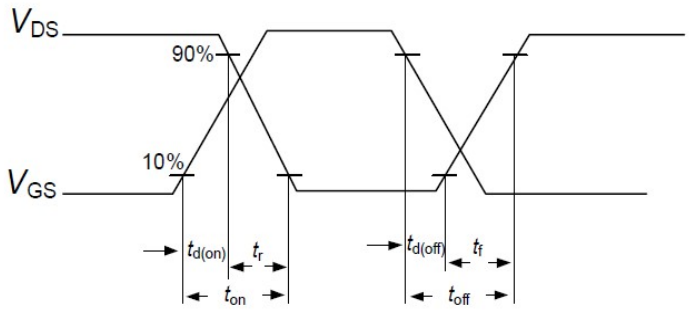
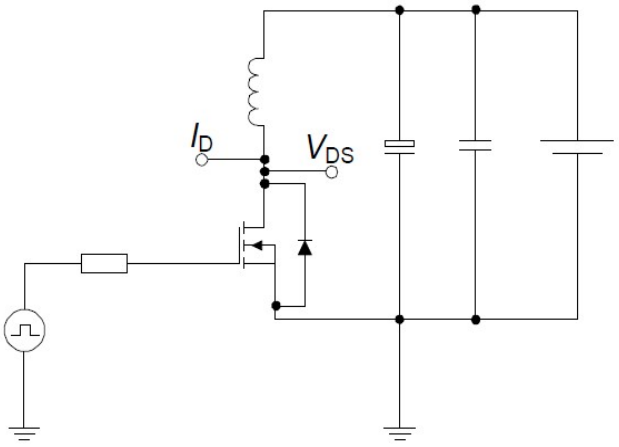
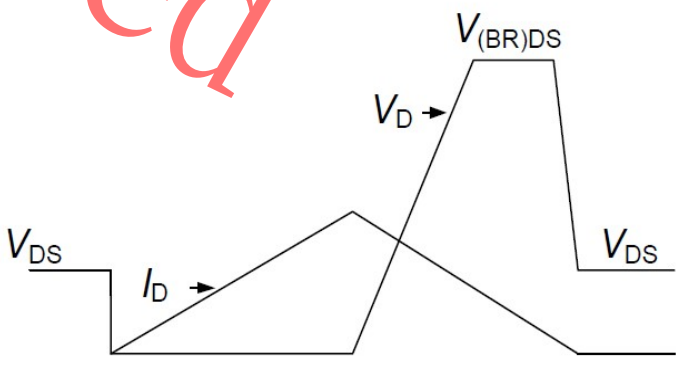
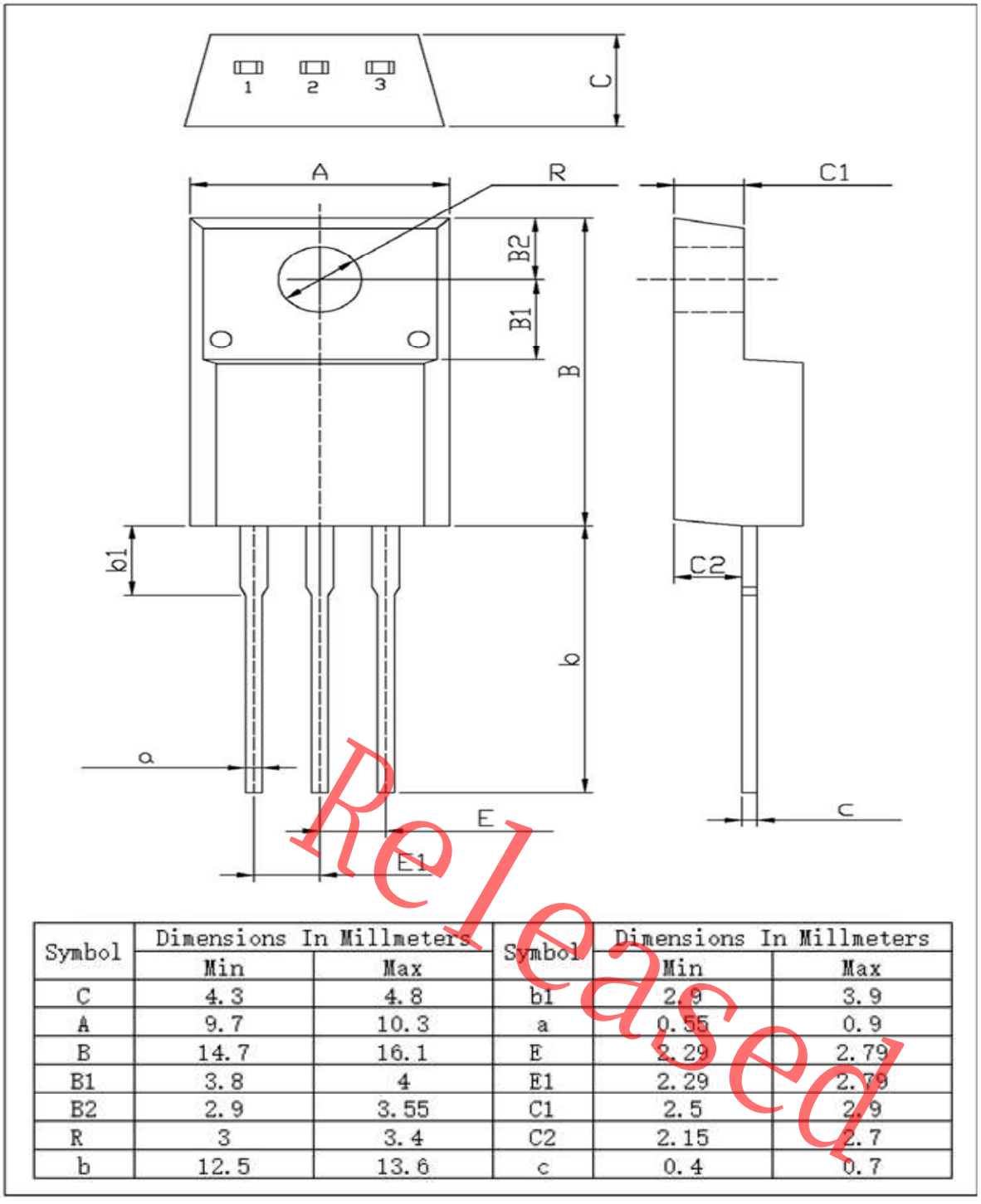
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductiveload

Unclamped inductive load test circuit	Unclamped inductive waveform
	

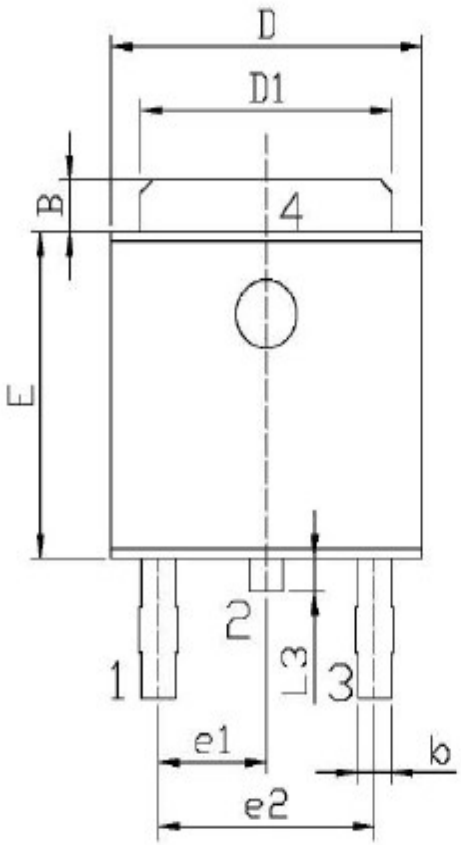
6 Package Outlines

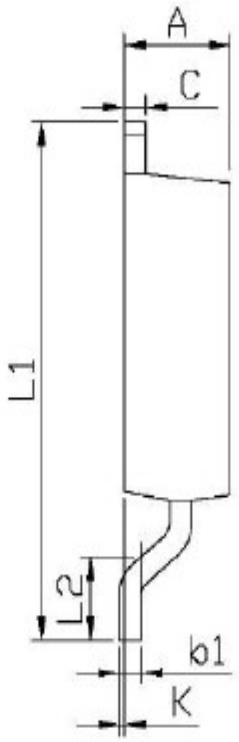
TO-220F 单位：mm



Symbol	Dimensions In Millmeters		Symbol	Dimensions In Millmeters	
	Min	Max		Min	Max
C	4.3	4.8	b1	2.9	3.9
A	9.7	10.3	a	0.55	0.9
B	14.7	16.1	E	2.29	2.79
B1	3.8	4	E1	2.29	2.79
B2	2.9	3.55	C1	2.5	2.9
R	3	3.4	C2	2.15	2.7
b	12.5	13.6	c	0.4	0.7

Figure1：OutlinePG-TO220F

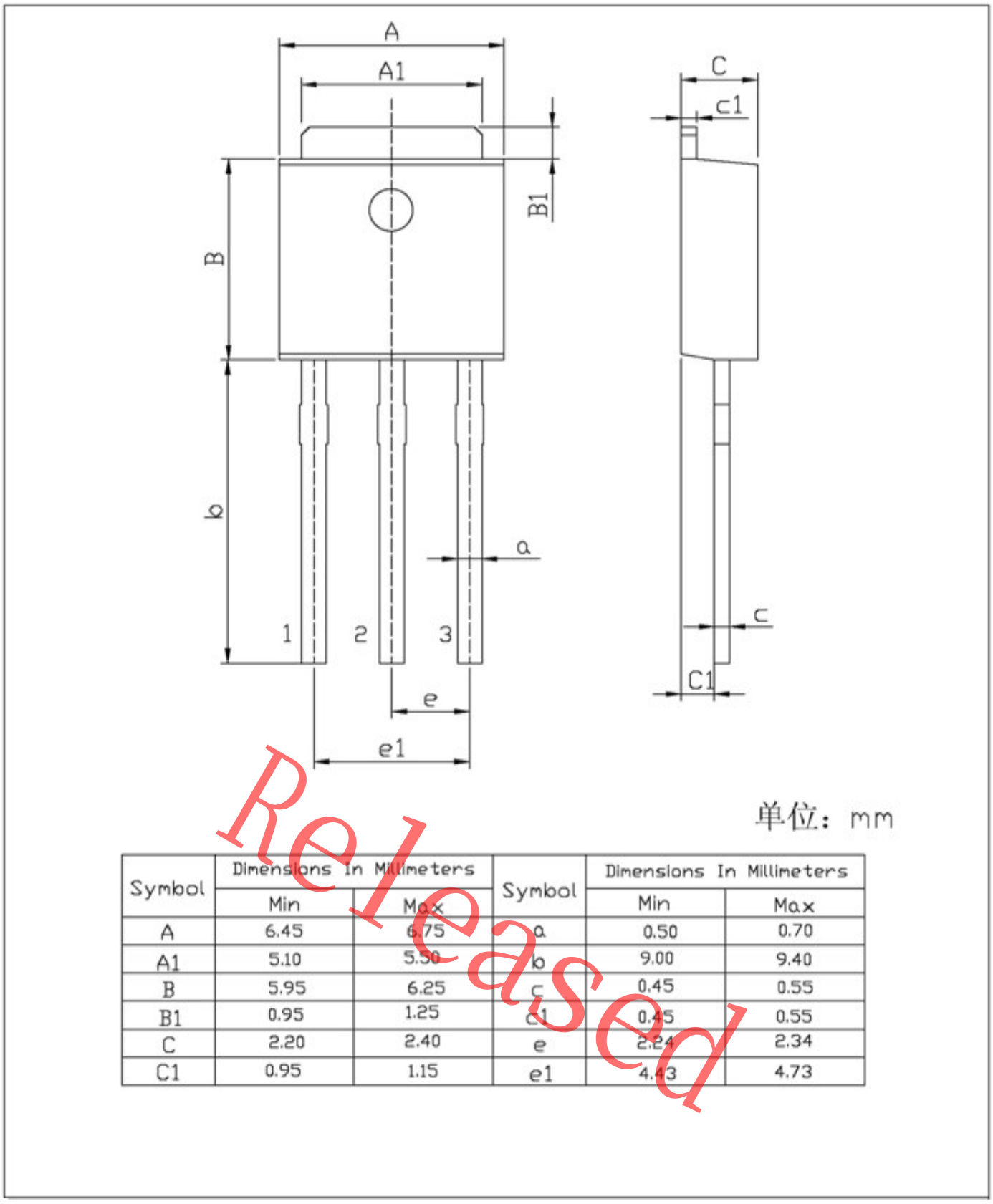




单位：mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	2.20	2.40	E	5.95	6.25
B	0.95	1.25	e1	2.24	2.34
b	0.50	0.70	e2	4.43	4.73
b1	0.45	0.55	L1	9.45	9.95
C	0.45	0.55	L2	1.25	1.75
D	6.45	6.75	L3	0.60	0.90
D1	5.10	5.50	K	0.00	0.10

Figure2：OutlinePG-TO252

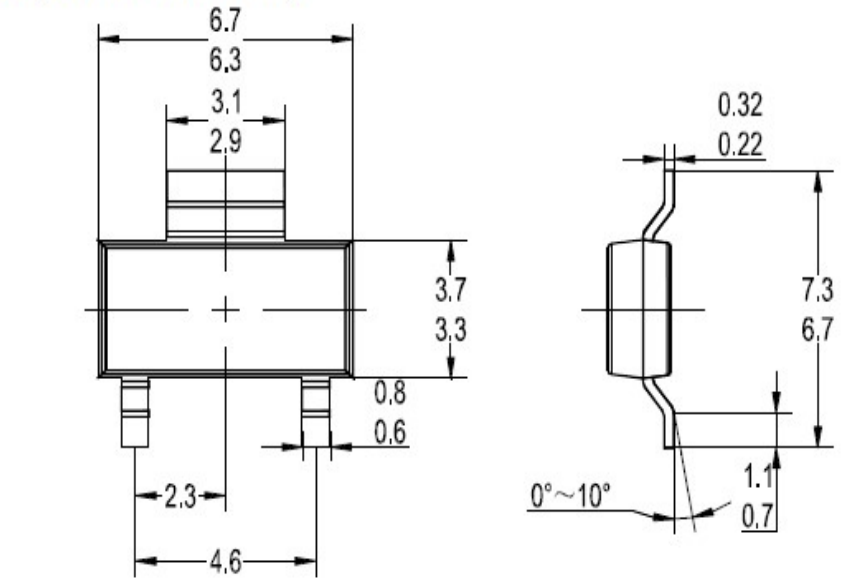


单位：mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	6.45	6.75	a	0.50	0.70
A1	5.10	5.50	b	9.00	9.40
B	5.95	6.25	c	0.45	0.55
B1	0.95	1.25	c1	0.45	0.55
C	2.20	2.40	e	2.24	2.34
C1	0.95	1.15	e1	4.43	4.73

Figure3：OutlinePG-TO251

PACKAGE OUTLINE (Dimensions in mm) SOT-223-2



Recommended Soldering Footprint

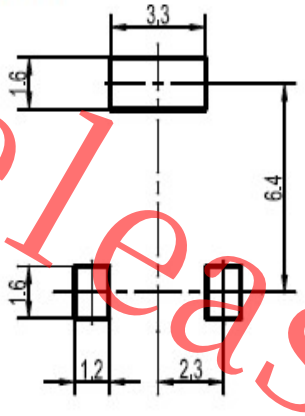


Figure3：OutlinePG-SOT223

Revision History

Revision	Date	Subjects (majorchangessince lastrevision)
0.1	2019-04-11	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc
1.1	2020-03-30	Add Electrical characteristics Curve
1.2	2020-04-18	Add avalanche energy test condition, avalanche current data and test condition
1.3	2021-02-03	Add part “ASE65R550E”