

DESCRIPTION

The 8810 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package

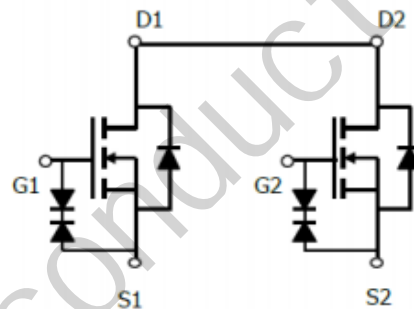
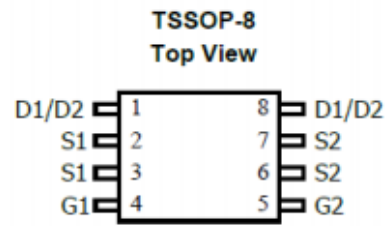
FEATURE

- ◆ 20V/7.0A, $R_{DS(ON)}=12m\Omega$ (typ.) @ $V_{GS}=4.5V$
- ◆ 20V/5.5A, $R_{DS(ON)}=15m\Omega$ (typ.) @ $V_{GS}=2.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ This is a Full RoHS compliance
- ◆ ESD Rating:2000V HBM
- ◆ TSSOP8 package design

APPLICATIONS

- ◆ Power Management in Note Book
- ◆ Portable Equipment
- ◆ Battery Powered System

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 10	V
I_D	Continuous Drain Current ($T_A=25^\circ C$)	$V_{GS}=10V$	7.0	A
	Continuous Drain Current ($T_A=75^\circ C$)		6.0	A
I_{DM}	Pulsed Drain Current		30	A
I_S	Continuous Source Current (Diode Conduction)		1	A
P_D	Power Dissipation	$T_A=25^\circ C$	1.5	W
		$T_A=75^\circ C$	1.0	
T_J	Operation Junction Temperature		150	$^\circ C$
T_{STG}	Storage Temperature Range		-55~+150	$^\circ C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ **THERMAL DATA**

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5		$^{\circ}\text{C}/\text{W}$

■ **ELECTRICAL CHARACTERISTICS**($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4	0.75	1.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 8\text{V}$			± 10	μA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0$			1	μA
		$V_{DS}=20\text{V}, V_{GS}=0$ $T_J=55^{\circ}\text{C}$			5	
$I_{D(ON)}$	On-State Drain Current	$V_{DS}\geq 5\text{V}, V_{GS}=4.5\text{V}$	7			A
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=4.5\text{V}, I_D=7\text{A}$	10	12.5	19	m Ω
		$V_{GS}=4.0\text{V}, I_D=7\text{A}$	11	13.5	19	
		$V_{GS}=3.1\text{V}, I_D=6.5\text{A}$	12	14	20	
		$V_{GS}=2.5\text{V}, I_D=5.5\text{A}$	13	16	22	
		$V_{GS}=1.8\text{V}, I_D=5\text{A}$	14	18	28	
G_{fs}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=7\text{A}$		31		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=1.0\text{A}, V_{GS}=0\text{V}$		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=10\text{V}$ $V_{GS}=4.5\text{V}$ $I_D=7.0\text{A}$		16		nC
Q_{gs}	Gate-Source Charge			1.7		
Q_{gd}	Gate-Drain Charge			6.8		
C_{iss}	Input Capacitance	$V_{DS}=10\text{V}$ $V_{GS}=0\text{V}$ $f=1\text{MHz}$		1120		pF
C_{oss}	Output Capacitance			1950		
C_{riss}	Reverse Transfer Capacitance			155		
$T_{d(on)}$	Turn-On Time	$V_{DS}=10\text{V}$ $I_D=7.0\text{A}$		7.2		nS
T_r				11		
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=5\text{V}$ $R_G=3.3\Omega$		64		
T_f				32		

Note: 1. Pulse test: pulse width $\leq 300\mu\text{S}$, duty cycle $\leq 2\%$

2.Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS** (25°C Unless Note)

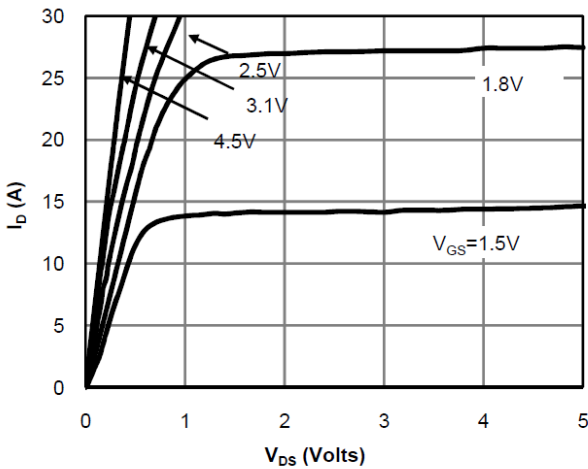


Fig 1: On-Region Characteristics (Note E)

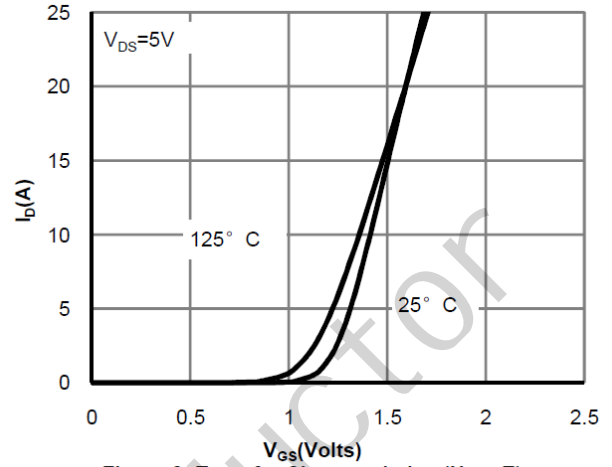


Figure 2: Transfer Characteristics (Note E)

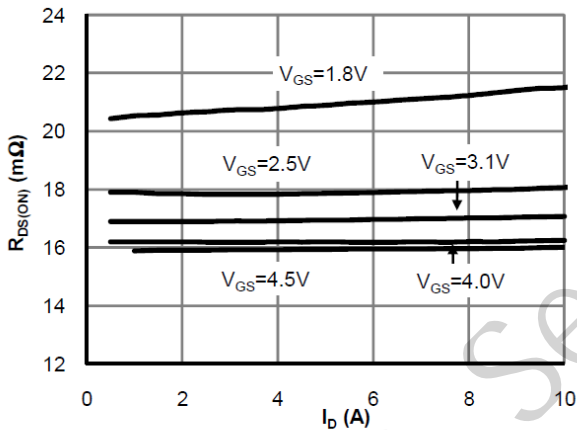


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

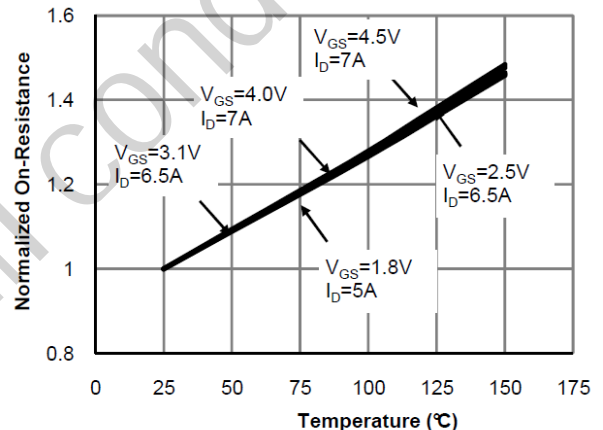


Figure 4: On-Resistance vs. Junction Temperature (Note E)

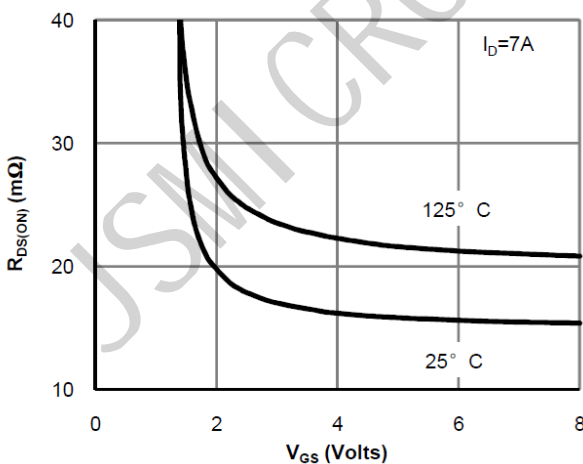


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

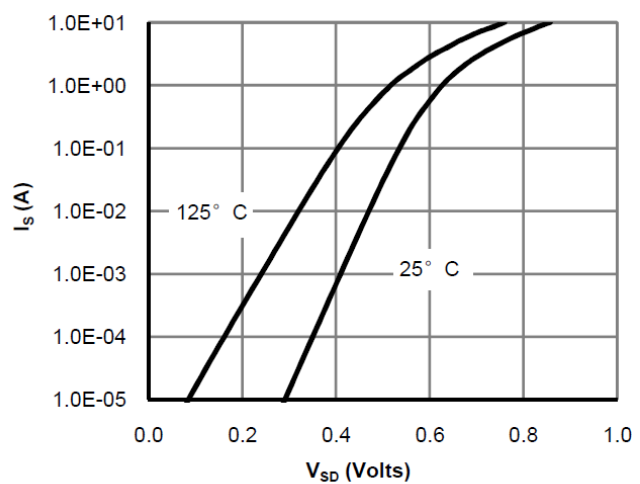


Figure 6: Body-Diode Characteristics (Note E)

■ **TYPICAL CHARACTERISTICS** (continuous)

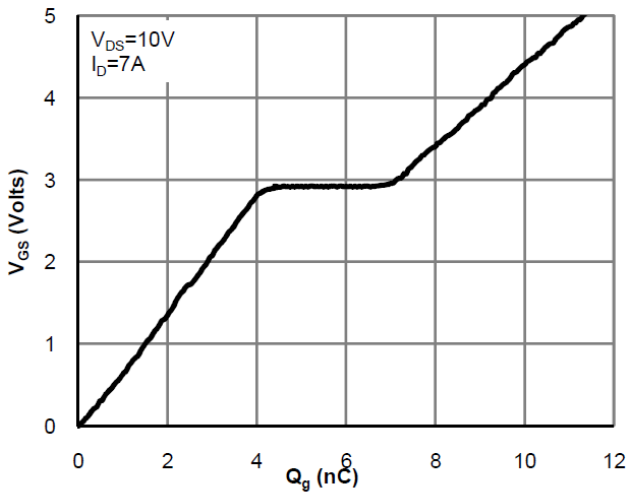


Figure 7: Gate-Charge Characteristics

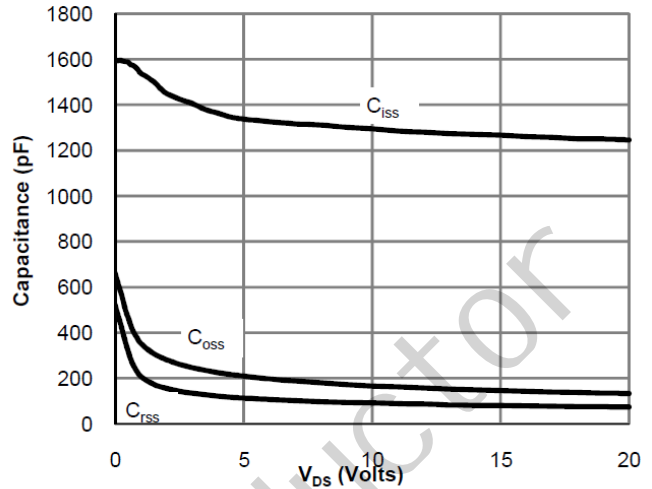


Figure 8: Capacitance Characteristics

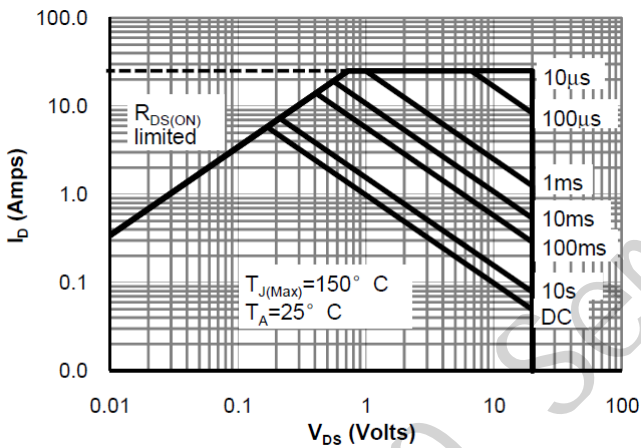


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

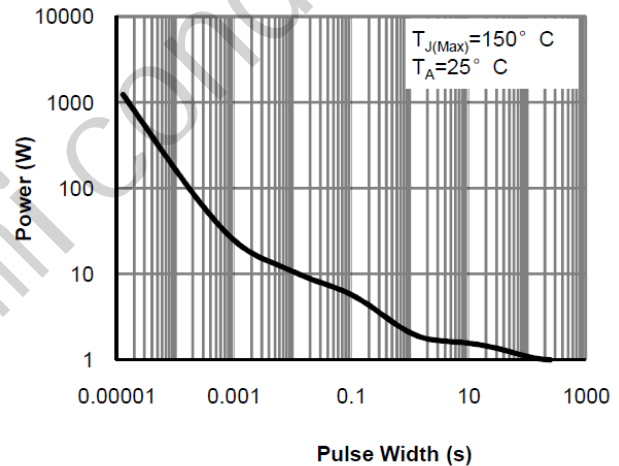


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

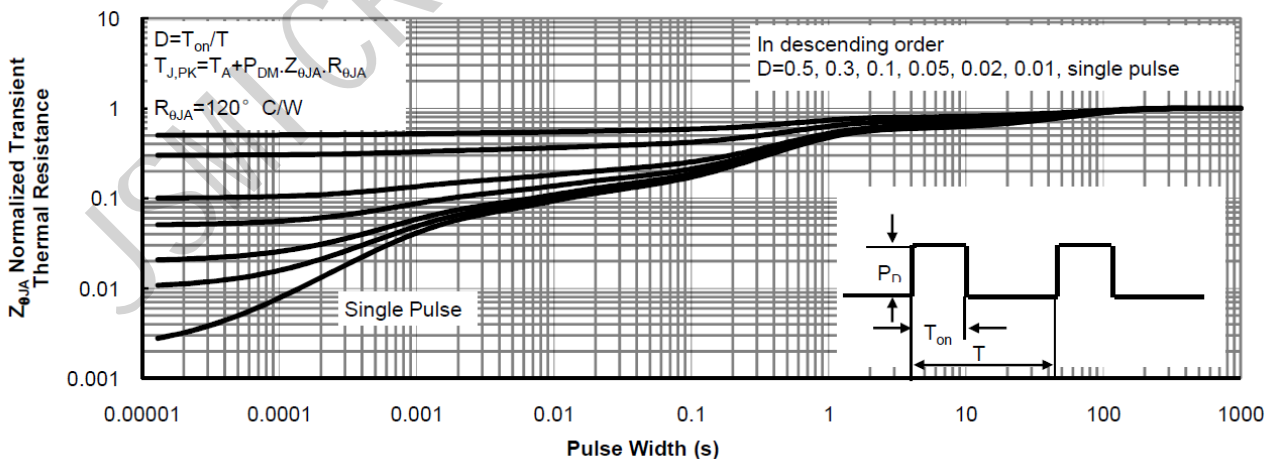
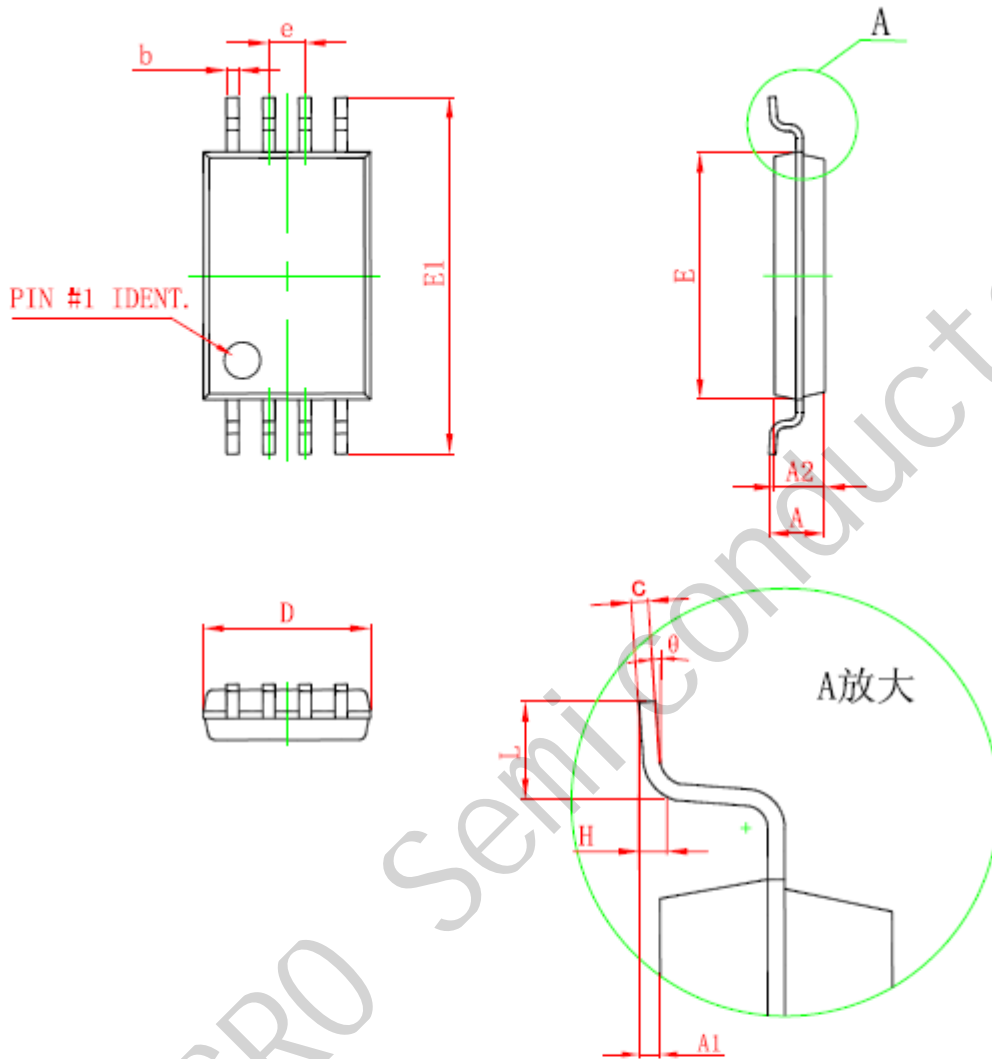


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

■ TSSOP8L PACKAGE OUTLINE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°