Precision, Low Noise, CMOS, Rail-to-Rail, Input/ Output Operational Amplifiers

The HT8605, HT8606, and HT8608[1] are single, dual, and quad rail-to-rail input and output, single-supply amplifiers. They feature very low offset voltage, low input voltage and current noise, and wide signal bandwidth. They use the Analog Devices, Inc. patented DigiTrim® trimming technique, which achieves superior precision without laser trimming.

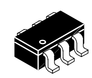
The combination of low offsets, low noise, very low input bias currents, and high speed makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for these amplifiers include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

FEATURES

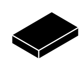
Low offset voltage: 65 µV maximum
Low input bias currents: 1 pA maximum
Low noise: 8 nV/√Hz
Wide bandwidth: 10 MHz
High open-loop gain: 1000 V/mV
Unity gain stable
Single-supply operation: 2.7 V to 5.5 V
5-ball WLCSP for single (HT8605) and 8-ball WLCSP for dual (HT8606)

APPLICATIONS

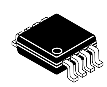
Photodiode amplification
Battery-powered instrumentation
Multipole filters
Sensors
Barcode scanners
Audio



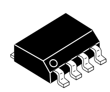
SOT23-5 T SUFFIX
HT8605ARTZ
HT8605BRTZ



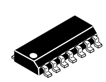
DFN−8* D SUFFIX
HT8606ARDZ



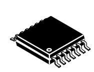
MSOP−8 M SUFFIX
HT8606ARMZ



SOP−8 R SUFFIX
HT8605ARZ
HT8606ARZ



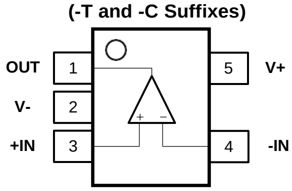
SOP−14 R SUFFIX
HT8608ARZ



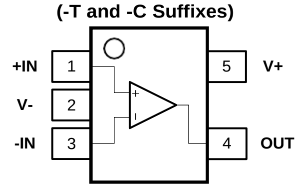
TSSOP−14 T SUFFIX
HT8608ARTZ

Pin Configuration (Top View)

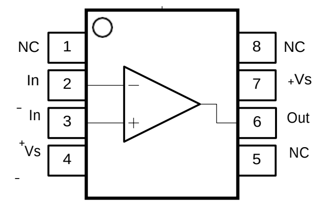
HT8605A
SOT23-5/SC70-5
(-T and -C Suffixes)



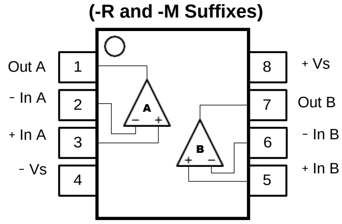
HT8605B
SOT23-5/SC70-5
(-T and -C Suffixes)



HT8605A
8-Pin SOIC
(-R Suffix)

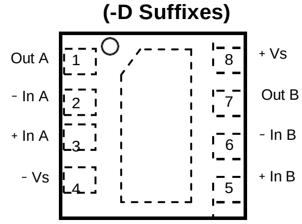


HT8606A
8-Pin SOIC/MSOP
(-R and -M Suffixes)

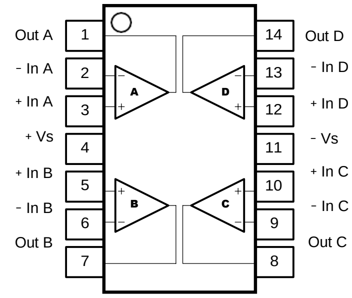


HT8606A

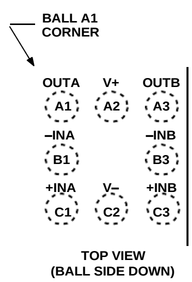
8-Pin DFN
(-D Suffixes)



HT8608A
14-Pin SOIC/TSSOP
(-R and -T Suffixes)



HT8606A
8-Pin LCSP8
(G Suffixes)



5 V ELECTRICAL SPECIFICATIONS

V_S = 5 V, V_{CM} = V_S/2, T_A = 25 ℃, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
HT8605/HT8606 (Except WLCSP)		V_S = 3.5 V, V_{CM} = 3 V		20	65	μV
HT8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	μV
HT8605/HT8606/HT8608		V_S = 5 V, V_{CM} = 0 V to 5 V		80	300	μV
		−40°C < T_A < +125°C			750	μV
Input Bias Current	I_B			0.2	1	pA
HT8605/HT8606		−40°C < T_A < +85°C			50	pA
HT8605/HT8606		−40°C < T_A < +125°C			250	pA
HT8608		−40°C < T_A < +85°C			100	pA
HT8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	85	100		dB
		−40°C < T_A < +125°C	75	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	300	1000		V/mV
Offset Voltage Drift						
HT8605/HT8606	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4.5	μV/°C
HT8608	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	μV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.96	4.98		V
		I_L = 10 mA	4.7	4.79		V
		−40°C < T_A < +125°C	4.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		20	40	mV
		I_L = 10 mA		170	210	mV
		−40°C < T_A < +125°C			290	mV
Output Current	I_{OUT}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
HT8605/HT8606		V_S = 2.7 V to 5.5 V	80	95		dB
HT8605/HT8606 WLCSP		V_S = 2.7 V to 5.5 V	75	92		dB
HT8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1	1.2	mA
		−40°C < T_A < +125°C			1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/μs
Settling Time	t_S	To 0.01%, 0 V to 2 V step, A_V = 1		<1		μs
Unity Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			65		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	μV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

2.7 V ELECTRICAL SPECIFICATIONS

V_S = 2.7 V, V_{CM} = V_S/2, T_A = 25 ℃, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
HT8605/HT8606 (Except WLCSP)		V_S = 3.5 V, V_{CM} = 3 V		20	65	μV
HT8608		V_S = 3.5 V, V_{CM} = 2.7 V		20	75	μV
HT8605/HT8606/HT8608		V_S = 2.7 V, V_{CM} = 0 V to 2.7 V		80	300	μV
		−40°C < T_A < +125°C			750	μV
Input Bias Current	I_B			0.2	1	pA
HT8605/HT8606		−40°C < T_A < +85°C			50	pA
HT8605/HT8606		−40°C < T_A < +125°C			250	pA
HT8608		−40°C < T_A < +85°C			100	pA
HT8608		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	80	95		dB
		−40°C < T_A < +125°C	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.2 V	110	350		V/mV
Offset Voltage Drift						
HT8605/HT8606	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4.5	μV/°C
HT8608	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	μV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.6	2.66		V
		−40°C < T_A < +125°C	2.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	40	mV
		−40°C < T_A < +125°C			50	mV
Output Current	I_{OUT}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
HT8605/HT8606		V_S = 2.7 V to 5.5 V	80	95		dB
HT8605/HT8606 WLCSP		V_S = 2.7 V to 5.5 V	75	92		dB
HT8608		V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1.15	1.4	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/μs
Settling Time	t_S	To 0.01%, 0 V to 1 V step, A_V = 1		<0.5		μs
Unity Gain Bandwidth Product	GBP			9		MHz
Phase Margin	Φ_M			50		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	μV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	6 V
Output Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	
All Packages	−65°C to +150°C
Operating Temperature Range	
All Packages	−40°C to +125°C
Junction Temperature Range	
All Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

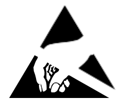
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Ball WLCSP (CB)	170		°C/W
5-Lead SOT-23 (RJ)	240	92	°C/W
8-Ball WLCSP (CB)	115		°C/W
8-Lead MSOP (RM)	206	44	°C/W
8-Lead SOIC_N (R)	157	56	°C/W
14-Lead SOIC_N (R)	105	36	°C/W
14-Lead TSSOP (RU)	148	23	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

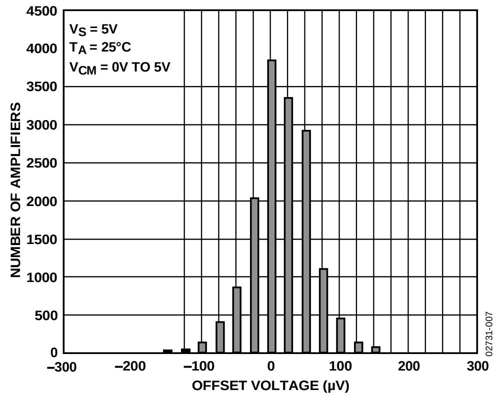


Figure 7. Input Offset Voltage Distribution

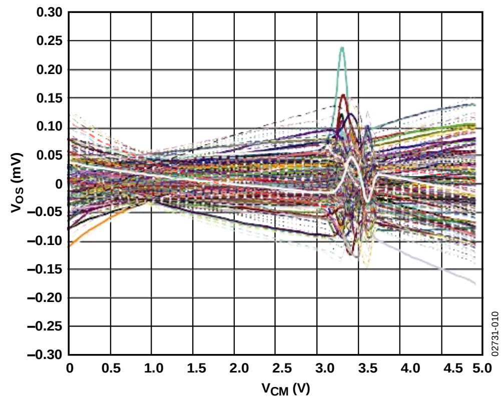


Figure 10. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

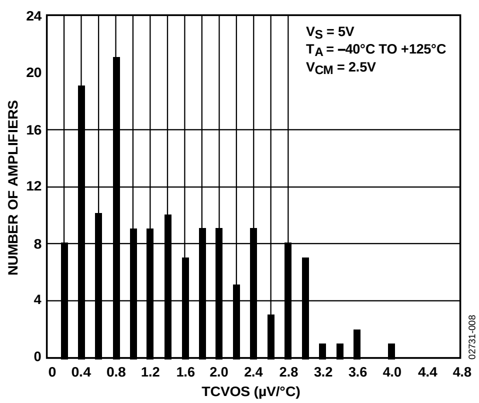


Figure 8. HT8608 Input Offset Voltage Drift Distribution

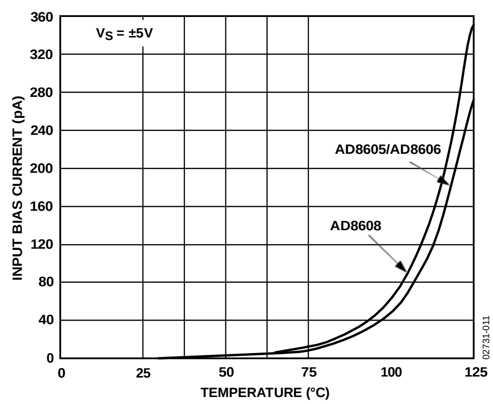


Figure 11. Input Bias Current vs. Temperature

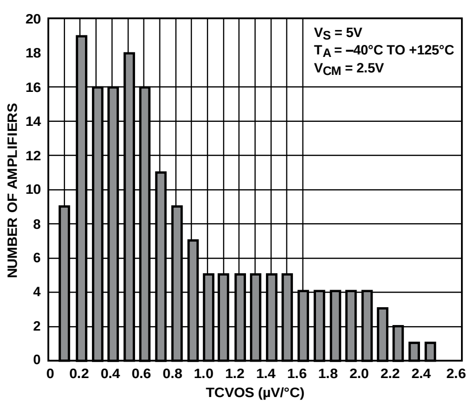


Figure 9. HT8605/HT8606 Input Offset Voltage Drift Distribution

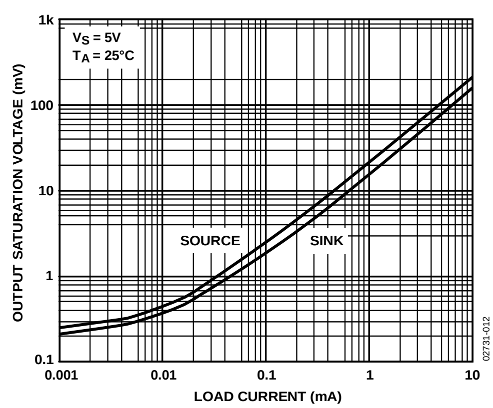


Figure 12. Output Saturation Voltage vs. Load Current

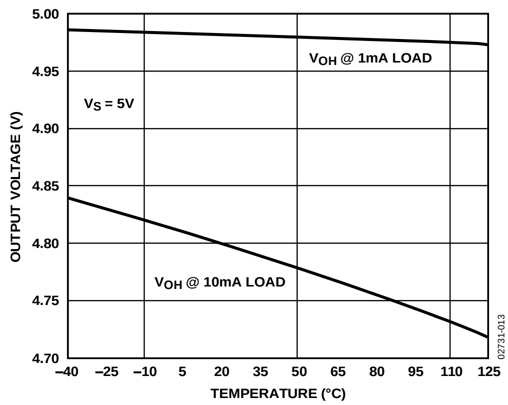


Figure 13. Output Voltage Swing High vs. Temperature

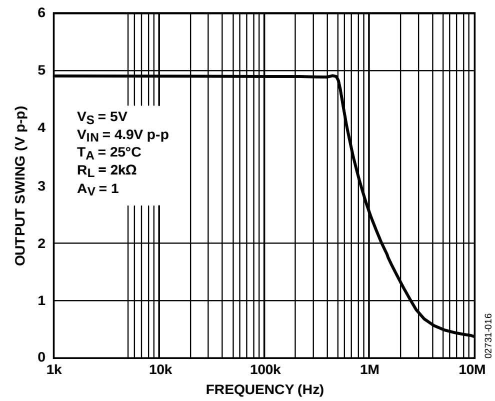


Figure 16. Closed-Loop Output Voltage Swing (FPBW)

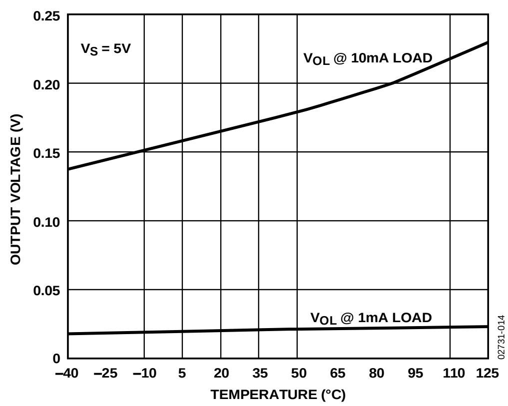


Figure 14. Output Voltage Swing Low vs. Temperature

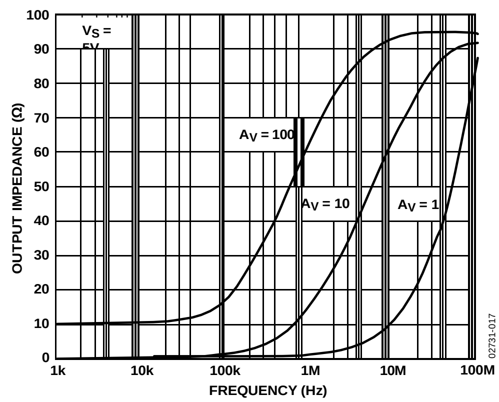


Figure 17. Output Impedance vs. Frequency

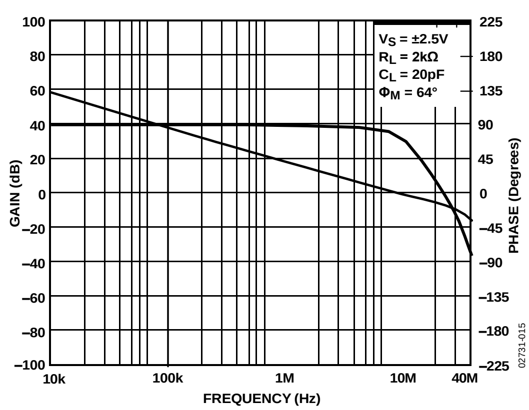


Figure 15. Open-Loop Gain and Phase vs. Frequency

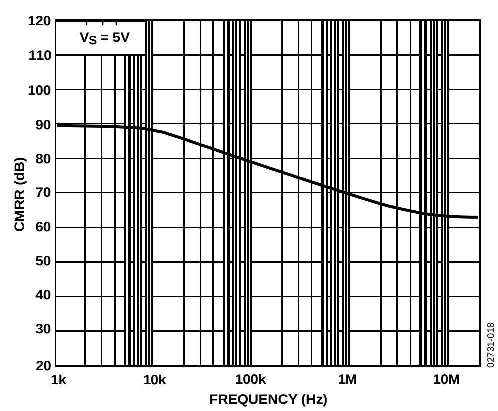


Figure 18. Common-Mode Rejection Ratio (CMRR) vs. Frequency

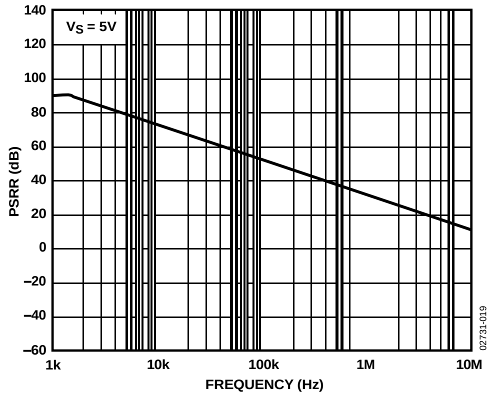


Figure 19. PSRR vs. Frequency

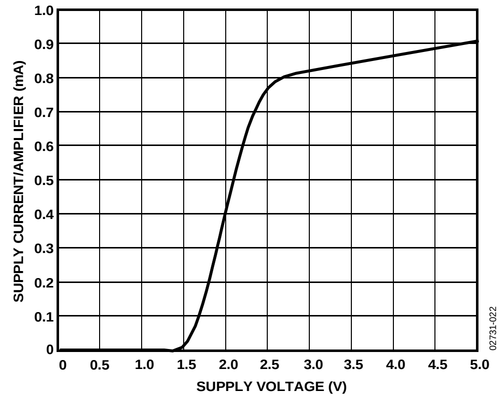


Figure 22. Supply Current/Amplifier vs. Supply Voltage

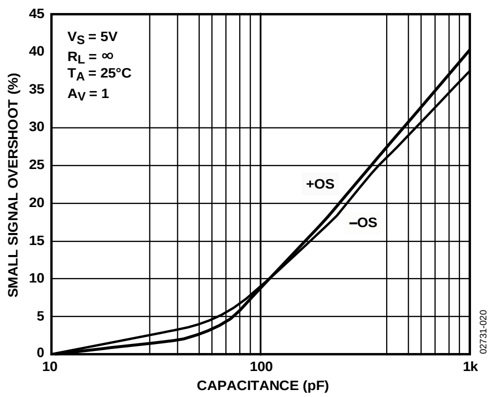


Figure 20. Small Signal Overshoot vs. Load Capacitance

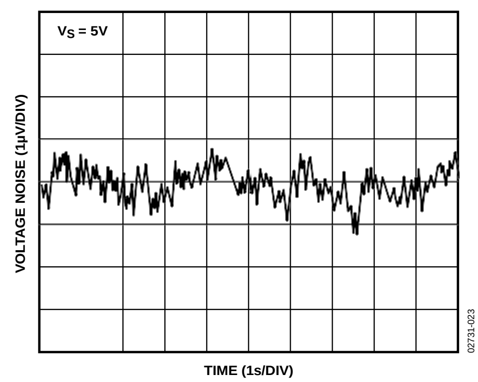


Figure 23. 0.1 Hz to 10 Hz Input Voltage Noise

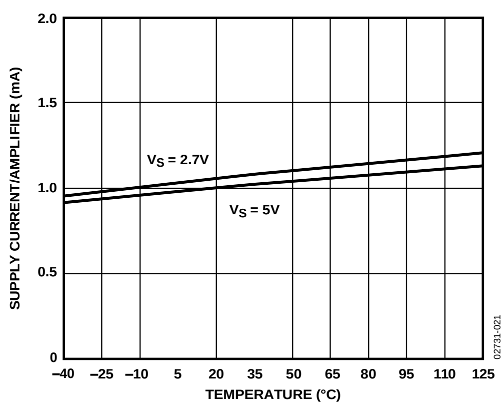


Figure 21. Supply Current/Amplifier vs. Temperature

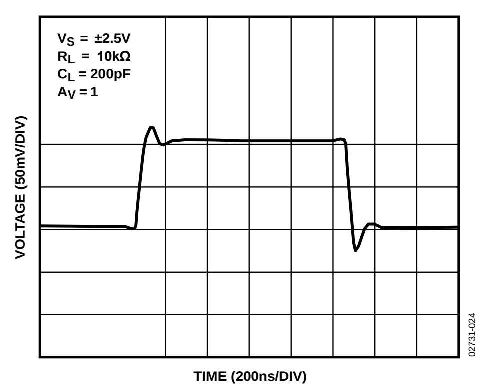


Figure 24. Small Signal Transient Response

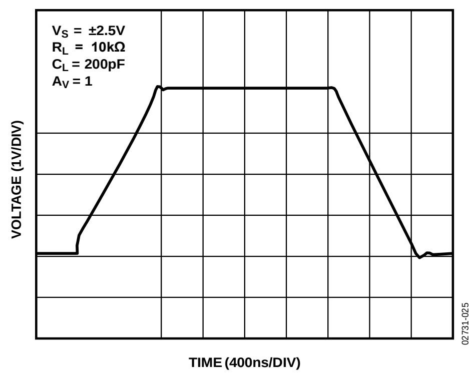


Figure 25. Large Signal Transient Response

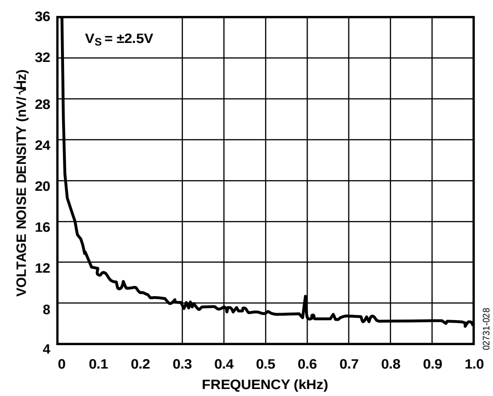


Figure 28. Voltage Noise Density vs. Frequency

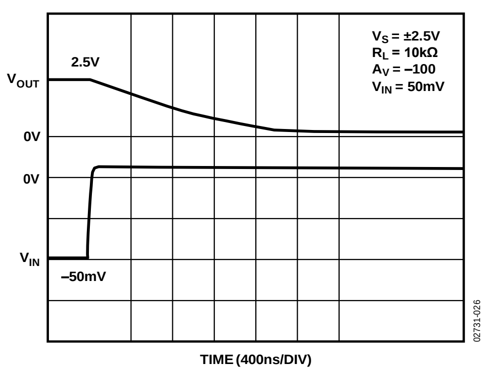


Figure 26. Positive Overload Recovery

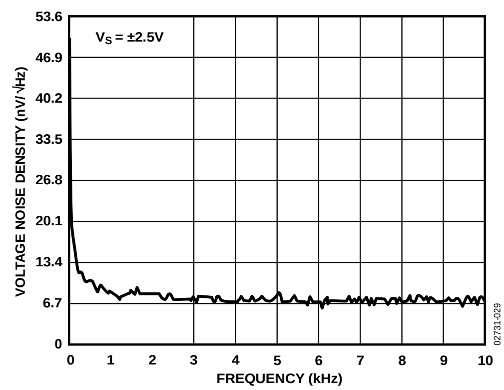


Figure 29. Voltage Noise Density vs. Frequency

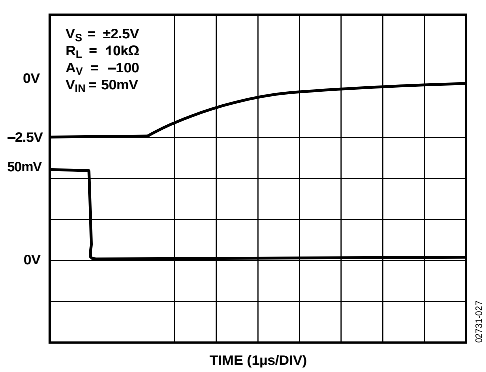


Figure 27. Negative Overload Recovery

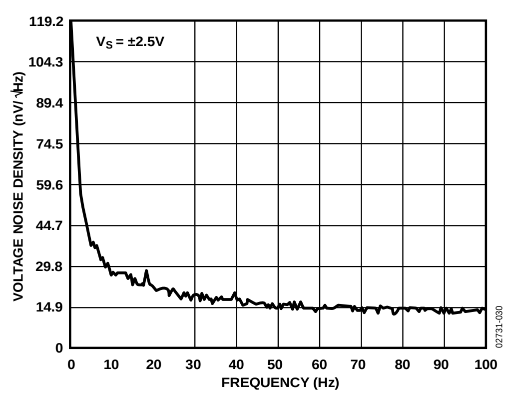


Figure 30. Voltage Noise Density vs. Frequency

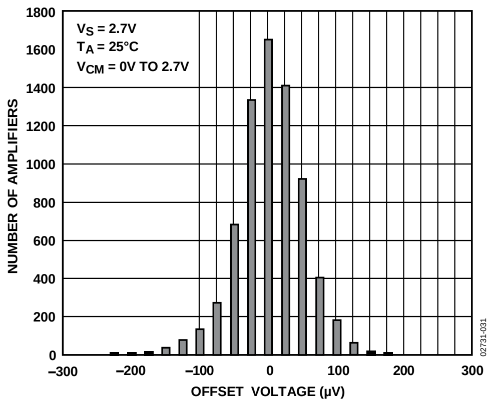


Figure 31. Input Offset Voltage Distribution

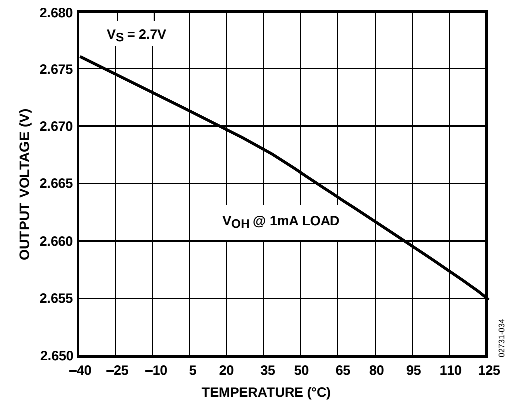


Figure 34. Output Voltage Swing High vs. Temperature

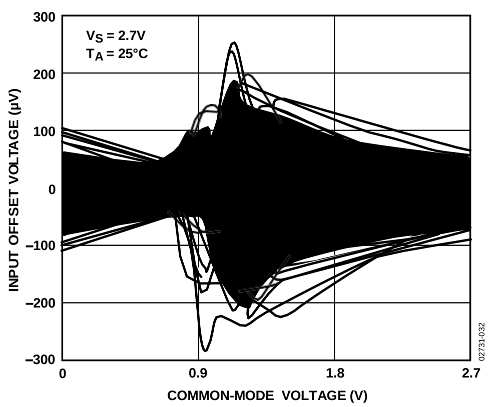


Figure 32. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

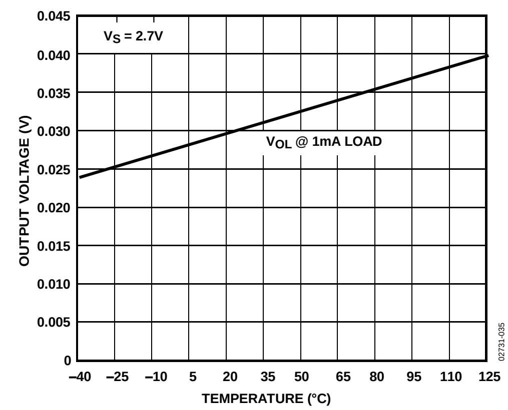


Figure 35. Output Voltage Swing Low vs. Temperature

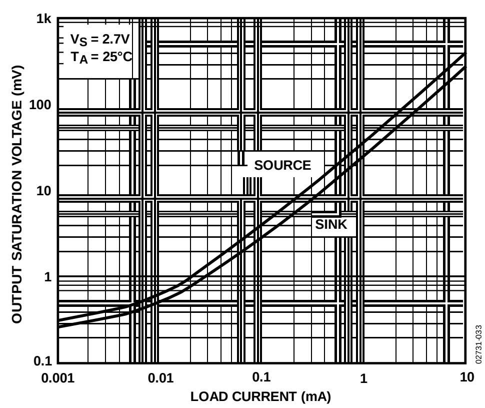


Figure 33. Output Saturation Voltage vs. Load Current

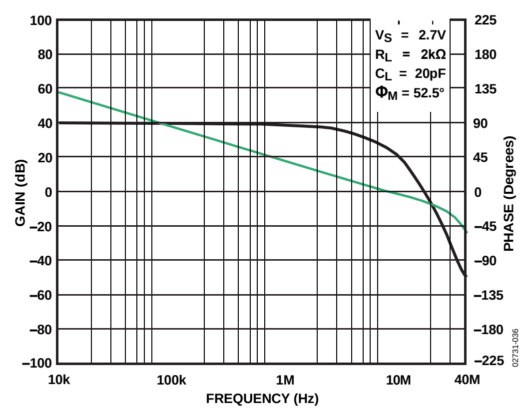


Figure 36. Open-Loop Gain and Phase vs. Frequency

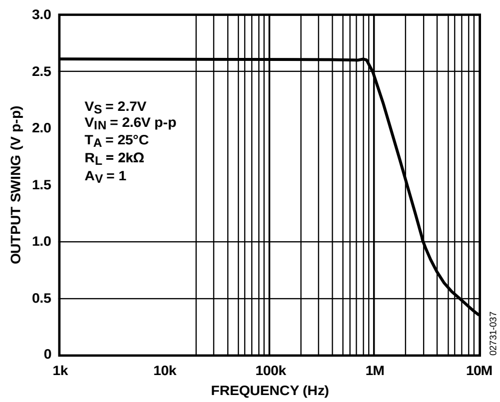


Figure 37. Closed-Loop Output Voltage Swing vs. Frequency (FPBW)

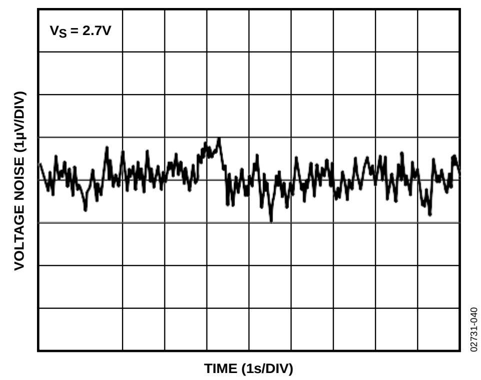


Figure 40. 0.1 Hz to 10 Hz Input Voltage Noise

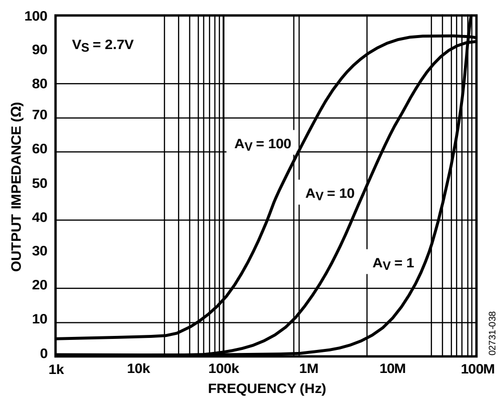


Figure 38. Output Impedance vs. Frequency

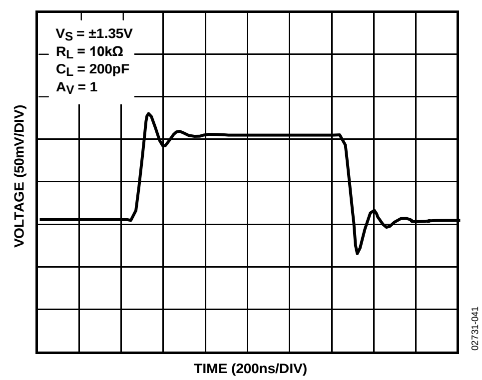


Figure 41. Small Signal Transient Response

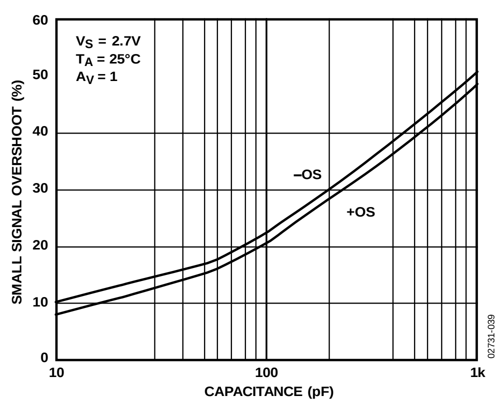


Figure 39. Small Signal Overshoot vs. Load Capacitance

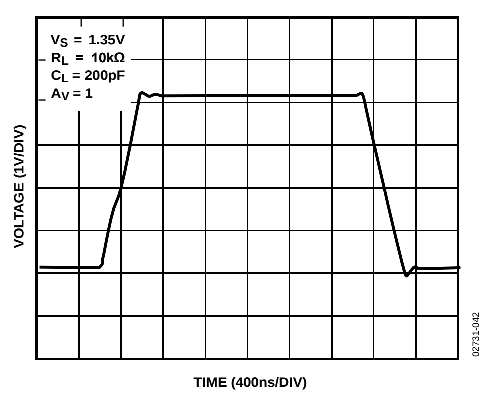


Figure 42. Large Signal Transient Response

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change in polarity at the output of the amplifier when a voltage that exceeds the maximum input common-mode voltage drives the input.

Phase reversal can cause permanent damage to the amplifier; it can also cause system lockups in feedback loops. The HT8605 does not exhibit phase reversal even for inputs exceeding the supply voltage by more than 2 V.

MAXIMUM POWER DISSIPATION

Power dissipated in an IC causes the die temperature to increase, which can affect the behavior of the IC and the application circuit performance.

The absolute maximum junction temperature of the HT8605/ HT8606/HT8608 is 150℃. Exceeding this temperature could damage or destroy the device.

The maximum power dissipation of the amplifier is calculated according to

$$P_{DISS} = \frac{T_J - T_A}{\theta_{JA}}$$

where:

T_J is the junction temperature.
T_A is the ambient temperature.
θ_{JA} is the junction-to-ambient thermal resistance.

Figure 44 compares the maximum power dissipation with temperature for the various HT860x family packages.

INPUT OVERVOLTAGE PROTECTION

The HT8605 has internal protective circuitry. However, if the voltage applied at either input exceeds the supplies by more than 2.5 V, external resistors should be placed in series with the inputs. The resistor values can be determined by

$$\frac{V_{IN} - V_S}{R_S + 200\Omega} \leq 5\text{mA}$$

The remarkable low input offset current of the HT8605 (<1 pA) allows the use of larger value resistors. With a 10 kΩ resistor at the input, the output voltage has less than 10 nV of error voltage. A 10 kΩ resistor has less than 13 nV/√Hz of thermal noise at room temperature.

THD + NOISE

Total harmonic distortion is the ratio of the input signal in V rms to the total harmonics in V rms throughout the spectrum. Harmonic distortion adds errors to precision measurements and adds unpleasant sonic artifacts to audio systems.

The HT8605 has a low total harmonic distortion. Figure 45 shows that the HT8605 has less than 0.005% or −86 dB of THD + N over the entire audio frequency range. The HT8605 is configured in positive unity gain, which is the worst case, and with a load of 10 kΩ.

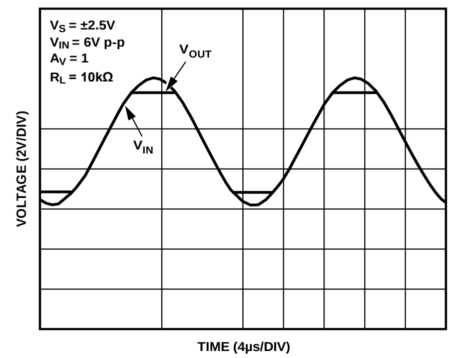


Figure 43. No Phase Reversal

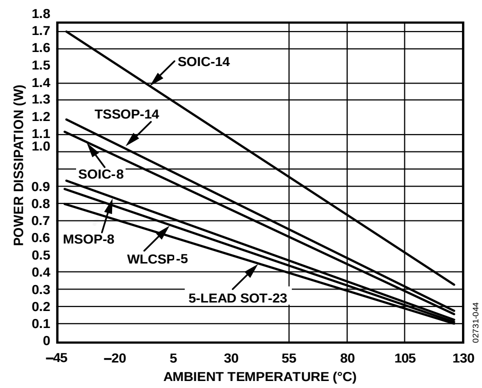


Figure 44. Maximum Power Dissipation vs. Ambient Temperature

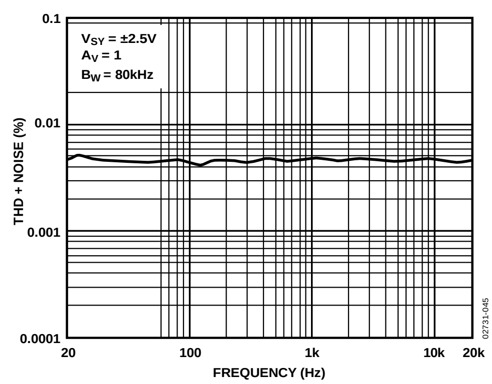


Figure 45. THD + Noise vs. Frequency

TOTAL NOISE INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the HT8605 make it the ideal amplifier for circuits with substantial input source resistance, such as photodiodes. Input offset voltage increases by less than 0.5 nV per 1 kΩ of source resistance at room temperature and increases to 10 nV at 85 ℃. The total noise density of the circuit is

$$e_{n,\ TOTAL} = \sqrt{e_n{}^2 + (i_n R_S)^2 + 4kTR_S}$$

where:

e_n is the input voltage noise density of the HT8605.
i_n is the input current noise density of the HT8605.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + ℃).

For example, with R_S = 10 kΩ, the total voltage noise density is roughly 15 nV/√Hz.

For R_S < 3.9 kΩ, e_n dominates and $e_{n,\ TOTAL} \approx e_n$.

The current noise of the HT8605 is so low that its total density does not become a significant term unless R_S is greater than 6 MΩ.

The total equivalent rms noise over a specific bandwidth is expressed as

$$E_n = (e_{n,\ TOTAL})\sqrt{BW}$$

where BW is the bandwidth in hertz.

Note that the previous analysis is valid for frequencies greater than 100 Hz and assumes relatively flat noise, above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

CHANNEL SEPARATION

Channel separation, or inverse crosstalk, is a measure of the signal feed from one amplifier (channel) to another on the same IC.

The HT8606 has a channel separation of greater than −160 dB up to frequencies of 1 MHz, allowing the two amplifiers to amplify ac signals independently in most applications.

CAPACITIVE LOAD DRIVE

The HT860x can drive large capacitive loads without oscillation. Figure 47 shows the output of the HT8606 in response to a 200 mV input signal. In this case, the amplifier is configured in positive unity gain, worst case for stability, while driving a 1000 pF load at its output. Driving larger capacitive loads in unity gain can require the use of additional circuitry.

A snubber network, shown in Figure 48, helps reduce the signal overshoot to a minimum and maintain stability. Although this circuit does not recover the loss of bandwidth induced by large capacitive loads, it greatly reduces the overshoot and ringing. This method does not reduce the maximum output swing of the amplifier.

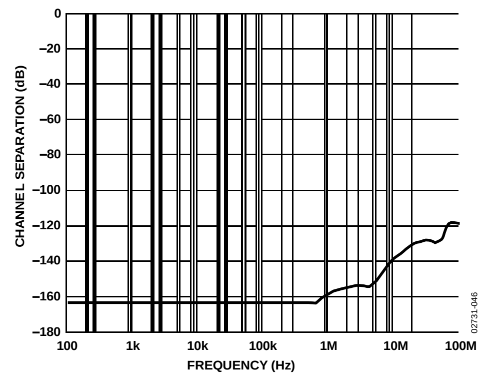


Figure 46. Channel Separation vs. Frequency

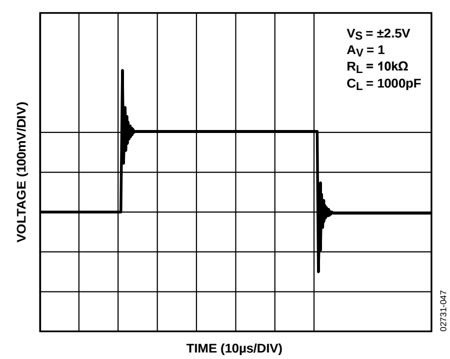


Figure 47. HT8606 Capacitive Load Drive Without Snubber

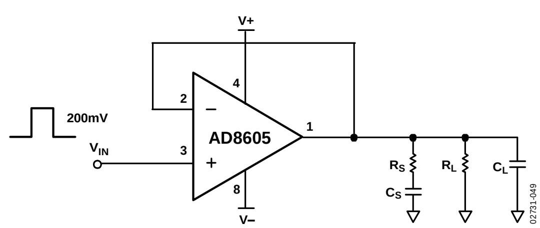


Figure 48. Snubber Network Configuration

Figure 49 shows a scope of the output at the snubber circuit. The overshoot is reduced from over 70% to less than 5%, and the ringing is eliminated by the snubber. Optimum values for R_S and C_S are determined experimentally.

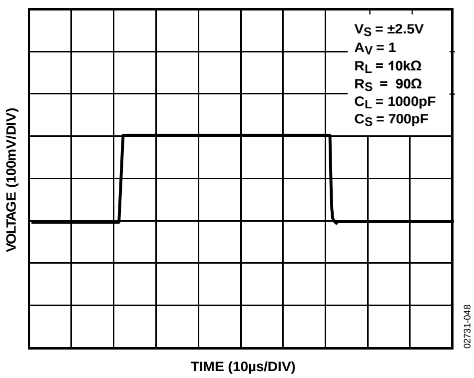


Figure 49. Capacitive Load Drive with Snubber

Table 5 summarizes a few optimum values for capacitive loads.

Table 5.

C_L (pF)	R_S (Ω)	C_S (pF)
500	100	1000
1000	70	1000
2000	60	800

An alternate technique is to insert a series resistor inside the feedback loop at the output of the amplifier. Typically, the value of this resistor is approximately 100 Ω. This method also reduces overshoot and ringing but causes a reduction in the maximum output swing.

LIGHT SENSITIVITY

The HT8605ACB (WLCSP package option) is essentially a silicon die with additional postfabrication dielectric and intermetallic processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of the HT8605ACB mounted on standard PCB material reveals that only the input bias current (I_B) parameter is impacted when the package is illuminated directly by high intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1 mW/cm^2) ambient light. Figure 50 shows that I_B increases with increasing wavelength and intensity of incident light; I_B can reach levels as high as 4500 pA at a light intensity of 3 mW/cm^2 and a wavelength of 850 nm. The light intensities shown in Figure 50 are not normal for most applications, that is, even though direct sunlight can have intensities of 50 mW/cm^2, office ambient light can be as low as 0.1 mW/cm^2.

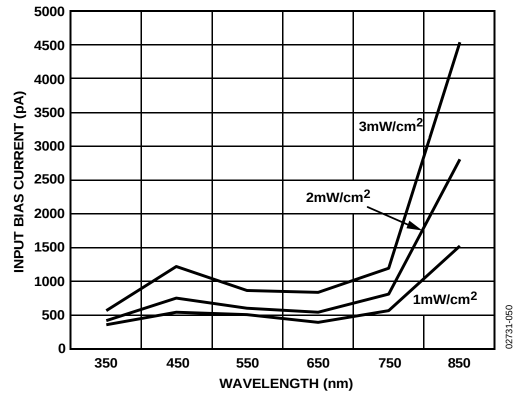


Figure 50. HT8605ACB Input Bias Current Response to Direct Illumination of Varying Intensity and Wavelength

When the WLCSP package is assembled on the board with the bump side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased I_B. No performance degradation occurs due to illumination of the backside (substrate) of the HT8605ACB. The HT8605ACB is particularly sensitive to incident light with wavelengths in the near infrared range (NIR, 700 nm to 1000 nm). Photons in this waveband have a longer wavelength and lower energy than photons in the visible (400 nm to 700 nm) and near ultraviolet (NUV, 200 nm to 400 nm) bands; therefore, they can penetrate more deeply into the active silicon. Incident light with wavelengths greater than 1100 nm has no photoelectric effect on the HT8605ACB because silicon is transparent to wavelengths in this range. The spectral content of conventional light sources varies. Sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; fluorescent lamps have significant peaks in the visible but not the NUV or NIR bands.

Efforts have been made at a product level to reduce the effect of ambient light; the under bump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump side) of the die. However, if an application encounters any light sensitivity with the HT8605ACB, shielding the bump side of the WLCSP package with opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica-filled liquid epoxies that are used in flip-chip underfill techniques.

WLCSP ASSEMBLY CONSIDERATIONS

For detailed information on the WLCSP PCB assembly and reliability, see Application Note AN-617, *MicroCSP™ Wafer Level Chip Scale Package*.

PHOTODIODE PREAMPLIFIER APPLICATIONS

The low offset voltage and input current of the HT8605 make it an excellent choice for photodiode applications. In addition, the low voltage and current noise make the amplifier ideal for application circuits with high sensitivity.

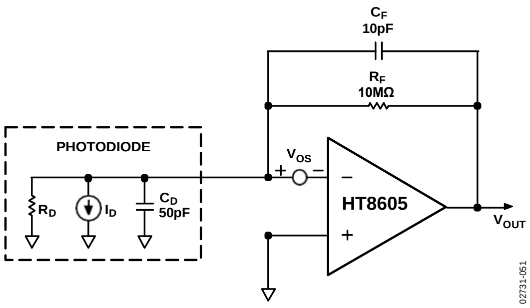


Figure 51. Equivalent Circuit for Photodiode Preamp

The input bias current of the amplifier contributes an error term that is proportional to the value of R_F.

The offset voltage causes a dark current induced by the shunt resistance of the Diode R_D. These error terms are combined at the output of the amplifier. The error voltage is written as

$$E_O = V_{OS}\left(1+\frac{R_F}{R_D}\right)+R_F I_B$$

Typically, R_F is smaller than R_D, thus R_F/R_D can be ignored.

At room temperature, the HT8605 has an input bias current of 0.2 pA and an offset voltage of 100 µV. Typical values of R_D are in the range of 1 GΩ.

For the circuit shown in Figure 51, the output error voltage is approximately 100 µV at room temperature, increasing to about 1 mV at 85 ℃.

The maximum achievable signal bandwidth is

$$f_{MAX} = \sqrt{\frac{f_t}{2\pi R_F C_F}}$$

where f_t is the unity gain frequency of the amplifier.

AUDIO AND PDA APPLICATIONS

The low distortion and wide dynamic range of the HT860x make it a great choice for audio and PDA applications, including microphone amplification and line output buffering.

Figure 52 shows a typical application circuit for headphone/ line-out amplification.

R1 and R2 are used to bias the input voltage at half the supply, which maximizes the signal bandwidth range. C1 and C2 are used to ac couple the input signal. C1, R1, and R2 form a high-pass filter whose corner frequency is 1/[2π(R1||R2)C1]. The high output current of the HT8606 allows it to drive heavy

resistive loads.

The circuit in Figure 52 is tested to drive a 16 Ω headphone. The THD + N is maintained at approximately −60 dB throughout the audio range.

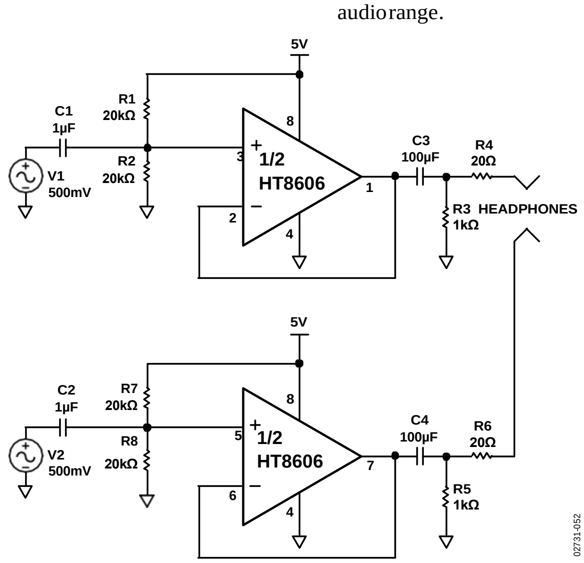


Figure 52. Single-Supply Headphone/Speaker Amplifier

INSTRUMENTATION AMPLIFIERS

The low offset voltage and low noise of the HT8605 make it an ideal amplifier for instrumentation applications.

Difference amplifiers are widely used in high accuracy circuits to improve the common-mode rejection ratio. Figure 53 shows a simple difference amplifier. Figure 54 shows the common-mode rejection for a unity gain configuration and for a gain of 10.

Making (R4/R3) = (R2/R1) and choosing 0.01% tolerance yields a CMRR of 74 dB and minimizes the gain error at the output.

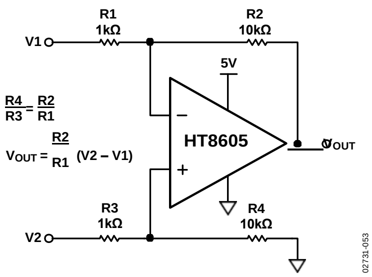


Figure 53. Difference Amplifier, A_V = 10

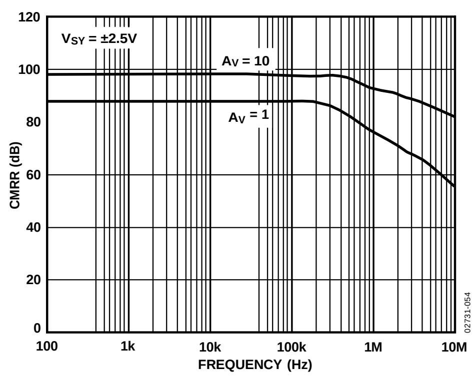


Figure 54. Difference Amplifier CMRR vs. Frequency

DAC CONVERSION

The low input bias current and offset voltage of the HT8605 make it an excellent choice for buffering the output of a current output DAC.

Figure 55 shows a typical implementation of the HT8605 at the output of a 12-bit DAC.

The DAC8143 output current is converted to a voltage by the feedback resistor. The equivalent resistance at the output of the DAC varies with the input code, as does the output capacitance.

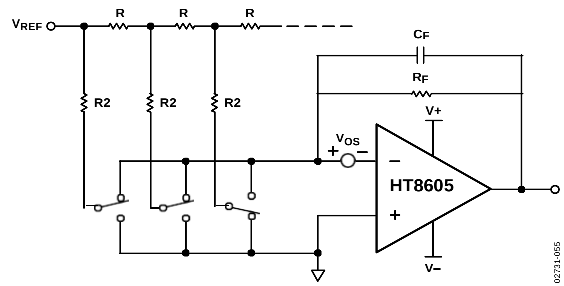


Figure 55. Simplified Circuit of the DAC8143 with HT8605 Output Buffer

To optimize the performance of the DAC, insert a capacitor in the feedback loop of the HT8605 to compensate the amplifier for the pole introduced by the output capacitance of the DAC. Typical values for C_F range from 10 pF to 30 pF; it can be adjusted for the best frequency response. The total error at the output of the op amp can be computed by

$$E_O = V_{OS}\left(1+\frac{R_F}{Req}\right)$$

where *Req* is the equivalent resistance seen at the output of the DAC. As previously mentioned, Req is code dependent and varies with the input. A typical value for Req is 15 kΩ. Choosing a feedback resistor of 10 kΩ yields an error of less than 200 µV.

Figure 56 shows the implementation of a dual-stage buffer at the output of a DAC. The first stage is used as a buffer. Capacitor C1 with Req creates a low-pass filter, and thus, provides phase lead to compensate for frequency response. The second stage of the HT8606 is used to provide voltage gain at the output of the buffer.

Grounding the positive input terminals in both stages reduces errors due to the common-mode output voltage. Choosing R1, R2, and R3 to match within 0.01% yields a CMRR of 74 dB and maintains minimum gain error in the circuit.

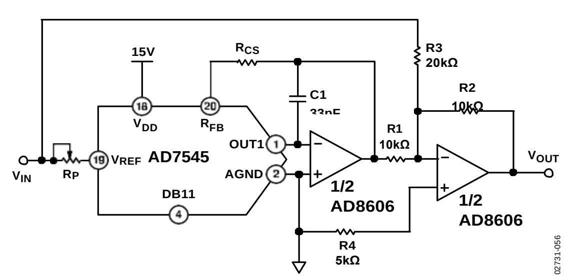
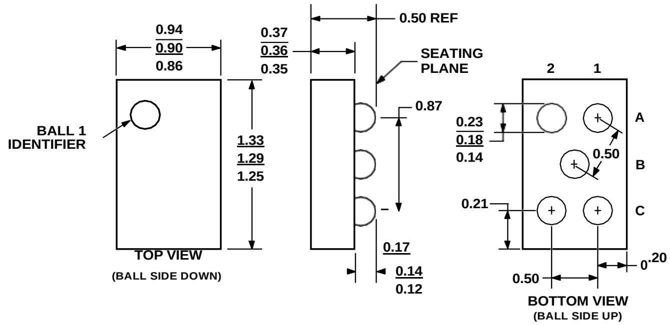
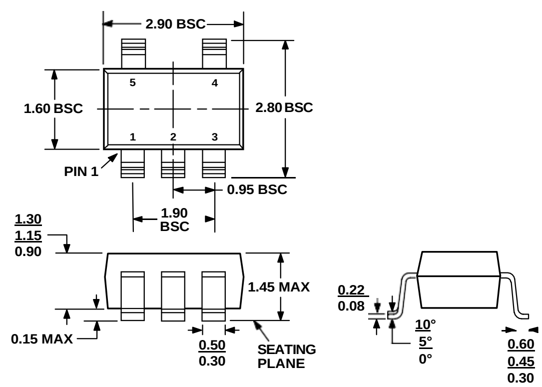
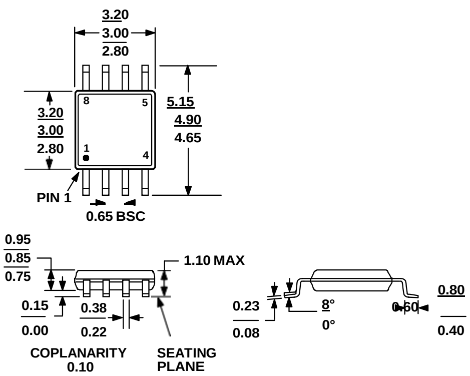


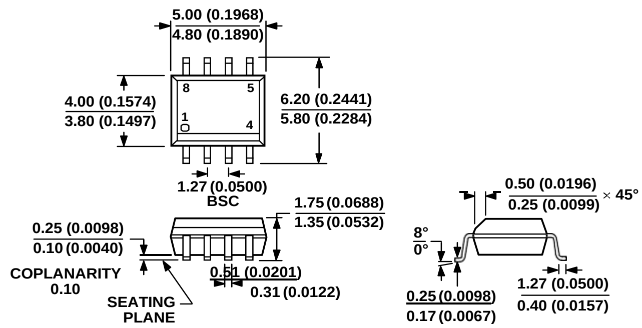
Figure 56. Bipolar Operation

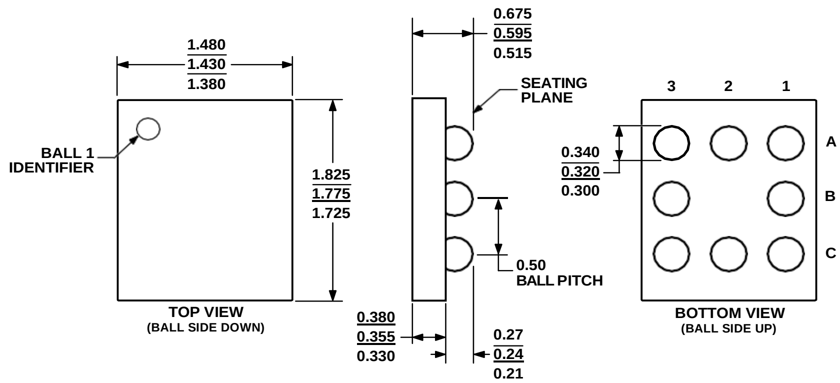
OUTLINE DIMENSIONS

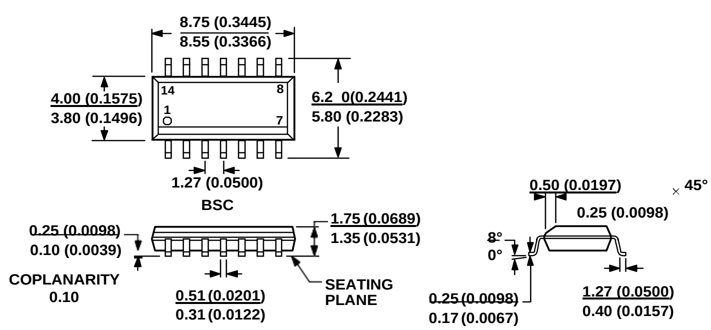


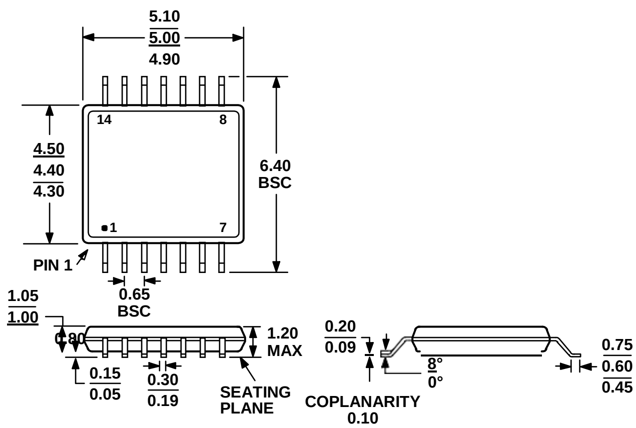





5.00 (0.1968)
4.80 (0.1890)
4.00 (0.1574)
3.80 (0.1497)
6.20 (0.2441)
5.80 (0.2284)
1.27 (0.0500)
BSC
0.25 (0.0098)
0.10 (0.0040)
COPLANARITY
0.10
SEATING
PLANE
0.51 (0.0201)
0.31 (0.0122)
1.75 (0.0688)
1.35 (0.0532)
0.50 (0.0196)
0.25 (0.0099)
× 45°
8°
0°
0.25 (0.0098)
0.17 (0.0067)
1.27 (0.0500)
0.40 (0.0157)


1.480
1.430
1.380
BALL 1
IDENTIFIER
1.825
1.775
1.725
TOP VIEW
(BALL SIDE DOWN)
0.675
0.595
0.515
SEATING
PLANE
0.340
0.320
0.300
0.50
BALL PITCH
0.380
0.355
0.330
0.27
0.24
0.21
3
2
1
A
B
C
BOTTOM VIEW
(BALL SIDE UP)


8.75 (0.3445)
8.55 (0.3366)
4.00 (0.1575)
3.80 (0.1496)
6.2 0(0.2441)
5.80 (0.2283)
1.27 (0.0500)
BSC
0.25 (0.0098)
0.10 (0.0039)
COPLANARITY
0.10
0.51 (0.0201)
0.31 (0.0122)
1.75 (0.0689)
1.35 (0.0531)
SEATING
PLANE
0.50 (0.0197)
× 45°
0.25 (0.0098)
8°
0°
0.25 (0.0098)
0.17 (0.0067)
1.27 (0.0500)
0.40 (0.0157)


5.10
5.00
4.90
14
8
4.50
4.40
4.30
6.40
BSC
1
7
PIN 1
0.65
BSC
1.05
1.00
0.80
1.20
MAX
0.20
0.09
0.75
0.60
0.45
8°
0°
0.15
0.05
0.30
0.19
SEATING
PLANE
COPLANARITY
0.10