

36V, 1.2MHz Dual Operational Amplifier

1 FEATURES

- **Unity-Gain Bandwidth: 1.2MHz**
- **Low Input Offset Voltage: $\pm 2.5\text{mV}$ (Max at 25°C)**
- **Quiescent Current: 1.3mA**
- **Common-Mode Input Voltage Range Include Ground**
- **Supply Range: 3V to 36V**
- **SPECIFIED UP TO +125°C**
- **Micro SIZE PACKAGES: SOIC-8(SOP8), MSOP-8 and TSSOP-8**

2 APPLICATIONS

- **SENSORS**
- **PHOTODIODE AMPLIFICATION**
- **ACTIVE FILTER**
- **TEST EQUIPMENT**
- **DRIVING A/D CONVERTERS**

3 DESCRIPTIONS

The LM2904 device offer high voltage (36V) operation and low input offset voltage, as well as excellent speed/power consumption ratio, providing an excellent bandwidth (1.2MHz) and slew rate of $0.5\text{V}/\mu\text{s}$. The op-amp is unity gain stable and feature an low input bias current.

The input can operate normally within of the negative power rail to 1.5V below of the positive power rail. The LM2904 operational amplifiers is specified at the full temperature range of -40°C to $+125^{\circ}\text{C}$ under single power supplies of 3V to 36V or dual power supplies of $\pm 1.5\text{V}$ to $\pm 18\text{V}$.

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE(NOM)
LM2904	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
	TSSOP-8	3.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

1 FEATURES	1
2 APPLICATIONS	1
3 DESCRIPTIONS	1
4 Revision History	3
5 PACKAGE/ORDERING INFORMATION ⁽¹⁾	4
6 Pin Configuration and Functions (Top View)	5
7 SPECIFICATIONS	6
7.1 Absolute Maximum Ratings	6
7.2 ESD Ratings	6
7.3 Recommended Operating Conditions	6
7.4 ELECTRICAL CHARACTERISTICS	7
7.5 TYPICAL CHARACTERISTICS	9
8 Detailed Description	11
8.1 Overview	11
8.2 Functional Block Diagram	11
8.3 Feature Description	11
8.3.1 Unity-Gain Bandwidth	11
8.3.2 Slew Rate	11
8.3.3 Input Common Mode Range	11
8.4 Device Functional Modes	11
9 Application and Implementation	12
9.1 Application Information	12
9.2 Typical Application	12
9.2.1 Design Requirements	12
9.2.2 Detailed Design Procedure	12
10 Power Supply Recommendations	13
11 LAYOUT	13
11.1 Layout Guidelines	13
11.2 Layout Example	14
12 PACKAGE OUTLINE DIMENSIONS	15
13 TAPE AND REEL INFORMATION	18

4 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2023/06/20	Preliminary version completed
A.1	2023/09/01	Initial version completed
A.2	2023/11/07	Update ESD Ratings

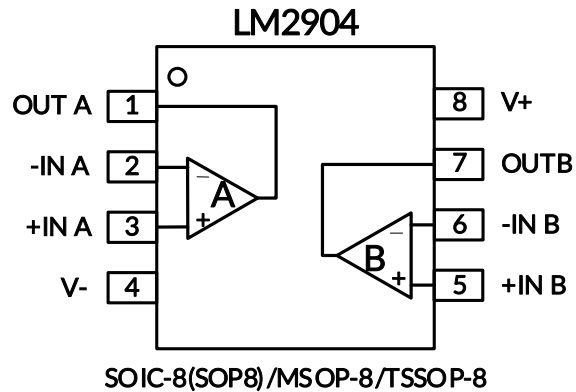
5 PACKAGE/ORDERING INFORMATION ⁽¹⁾

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking ⁽²⁾	Package Qty
LM2904XK-G	SOIC-8(SOP8)	8	2	-40°C ~125°C	LM2904	Tape and Reel,4000
LM2904XM-G	MSOP-8	8	2	-40°C ~125°C	LM2904	Tape and Reel,4000
LM2904XQ-G	TSSOP-8	8	2	-40°C ~125°C	LM2904	Tape and Reel,4000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O ⁽¹⁾	DESCRIPTION
	SOIC-8(SOP8)/MSOP-8/TSSOP-8		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply or ground (for single supply operation)
V+	8	-	Positive (highest) power supply

(1) I = Input, O = Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
Voltage	Supply, $V_S = (V+) - (V-)$			40	V
	Signal input pin ⁽²⁾		$(V-) - 0.3$	$(V+) + 0.3$	
	Signal output pin ⁽³⁾		$(V-) - 0.3$	$(V+) + 0.3$	
	Differential input voltage		$(V-) - (V+)$	$(V+) - (V-)$	
Current	Output short-circuits ⁽⁴⁾		Continuous		
θ_{JA}	Package thermal impedance ⁽⁵⁾	SOIC-8(SOP8)		110	°C/W
		MSOP-8		170	
		TSSOP-8		240	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J ⁽⁶⁾		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ± 10 mA or less.

(4) Short-circuit to ground, one amplifier per package.

(5) The package thermal impedance is calculated in accordance with JEDEC-51.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS001-2017	± 500	V
		Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2018	± 1000	
		Machine Model (MM), JESD22-A115C (2010)	± 100	



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	Single-supply	3		36	V
	Dual-supply	± 1.5		± 18	

7.4 ELECTRICAL CHARACTERISTICS

(At $T_A = +25^\circ\text{C}$, $V_S = 3\text{V}$ to 36V , $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, $V_{CM} = V_S/2$, Full ⁽⁹⁾ = -40°C to $+125^\circ\text{C}$, unless otherwise noted.) ⁽¹⁾

PARAMETER		CONDITIONS	T _J	LM2904			UNIT
				MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	
POWER SUPPLY							
V _S	Operating Voltage Range		25°C	3		36	V
I _Q	Quiescent Current	V _S =±2.5V, I _O =0mA	25°C		1.3	1.5	mA
			Full			1.8	
		V _S =±18V, I _O =0mA	25°C		1.75	2.0	
			Full			2.4	
PSRR	Power-Supply Rejection Ratio	V _S =±2.5V to ±18V	25°C	90	100		dB
			Full	80			
INPUT							
V _{OS}	Input Offset Voltage	V _{CM} = V _S /2	25°C	-2.5	±1	2.5	mV
			Full	-6		6	
V _{OS} T _C	Input Offset Voltage Average Drift	V _{CM} = V _S /2	Full		±8		μV/°C
I _B	Input Bias Current ^{(4) (5)}	V _{CM} = V _S /2	25°C		±15	±35	nA
			Full			±50	
I _{OS}	Input Offset Current ⁽⁵⁾	V _{CM} = V _S /2	25°C		±0.5	±4	nA
			Full			±5	
V _{CM}	Common-Mode Voltage Range	V _S = 3V to 36V	25°C	(V-)		(V+)-1.5	V
		V _S = 5V to 36V	Full	(V-)		(V+)-2	
CMRR	Common-Mode Rejection Ratio	V _S = ±18V, V _{CM} =(V-) to (V+)-1.5V	25°C	80	100		dB
		V _S = ±18V, V _{CM} =(V-) to (V+)-2V	Full	70			
OUTPUT							
A _{OL}	Open-Loop Voltage Gain	R _L =10KΩ, V _S = ±18V, V _O =-16.5V to 16.5V	25°C	102	110		dB
			Full	70			
V _{OH}	Output Swing	I _{OUT} =50uA	25°C		1.27	1.4	V
		I _{OUT} =1mA	25°C		1.32	1.45	
		I _{OUT} =5mA	25°C		1.41	1.6	
V _{OL}		I _{OUT} =50uA	25°C		55	120	mV
		I _{OUT} =1mA	25°C		0.77	1	V
I _{SC}	Short-Circuit Current ^{(6) (7)}	V _S =±10V, V _O =0V, I _{SOURCE}	25°C	50	60		mA
		V _S =±10V, V _O =0V, I _{SINK}		12	20		
FREQUENCY RESPONSE							
SR	Slew Rate ⁽⁸⁾	V _S =±2.5V, G=+1, C _L =100pF	25°C		0.5		V/μs
GBW	Gain-Bandwidth Product	V _S =±2.5V, G=+11, V _{pp} =50mV	25°C		1.2		MHz
		V _S =±18V, G=+11, V _{pp} =50mV	25°C		1.4		
t _s	Settling Time,0.01%	V _S =±2.5V, G=+1, C _L =100nF, Step=2V	25°C		4		μs

t_{OR}	Overload Recovery Time	$V_{IN} \cdot \text{Gain} \geq V_S, V_S = \pm 2.5V, V_{pp} = 1V, G = 11$	25°C		4		μs
Φ_m	Phase Margin ⁽⁵⁾	$V_S = \pm 2.5V, G = +1, C_L = 50pF$	25°C		52		°
C_{LOAD}	Capacitive Load Drive		25°C		100		pF
NOISE							
E_n	Input Voltage Noise	$f = 0.1Hz \text{ to } 10Hz, V_S = \pm 2.5V$	25°C		0.91		μV_{pp}
e_n	Input Voltage Noise Density ⁽⁵⁾	$f = 1KHz$	25°C		38		nV/\sqrt{Hz}

NOTE:

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
- (4) Positive current corresponds to current flowing into the device.
- (5) This parameter is ensured by design and/or characterization and is not tested in production.
- (6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
- (7) Short circuit test is a momentary test.
- (8) Number specified is the slower of positive and negative slew rates.
- (9) Specified by characterization only.

7.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, unless otherwise noted.

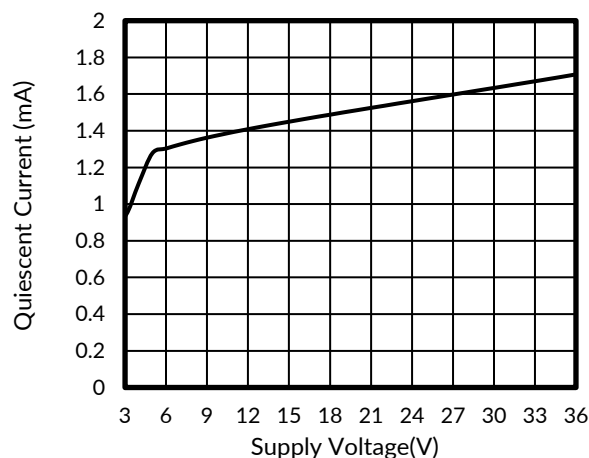


Figure 1. Supply Voltage vs Quiescent Current

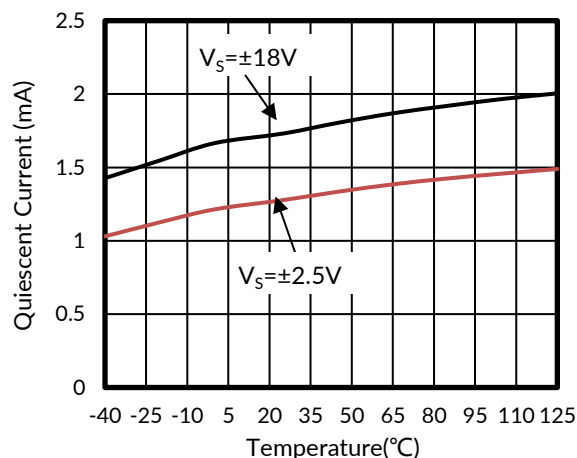


Figure 2. Quiescent Current vs Temperature

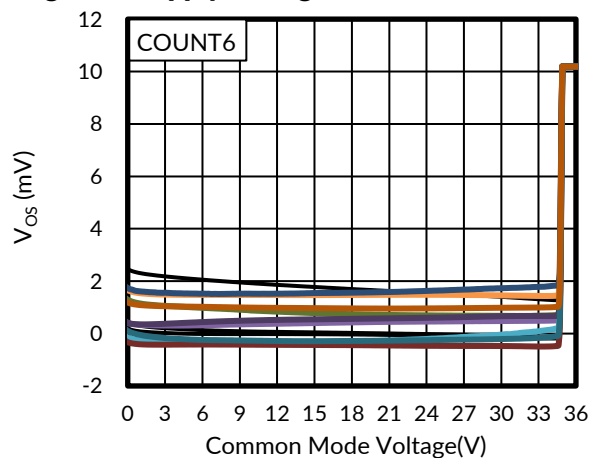


Figure 3. Offset Voltage vs Common Mode Voltage

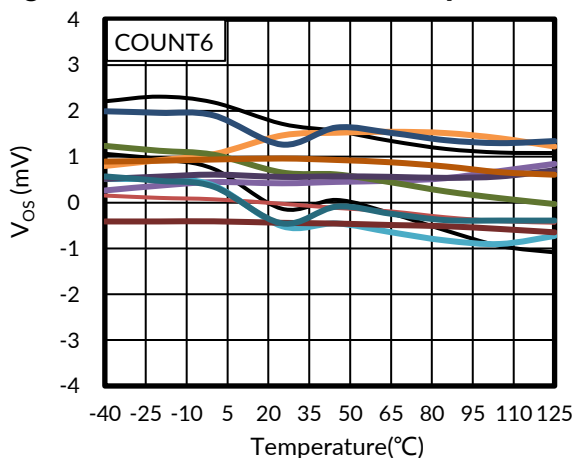


Figure 4. Offset Voltage vs Temperature

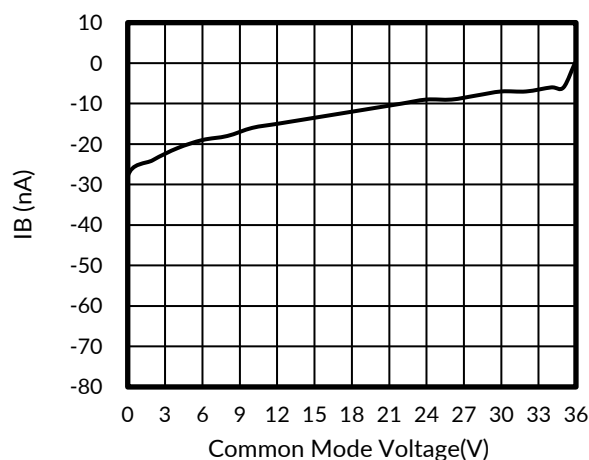


Figure 5. Input Bias Current vs Common Mode Voltage

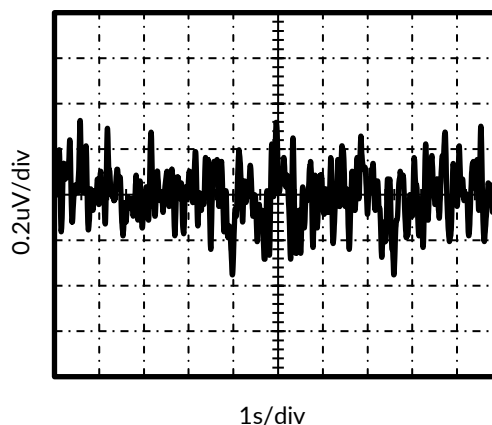


Figure 6. 0.1Hz to 10Hz Input Voltage Noise

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, unless otherwise noted.

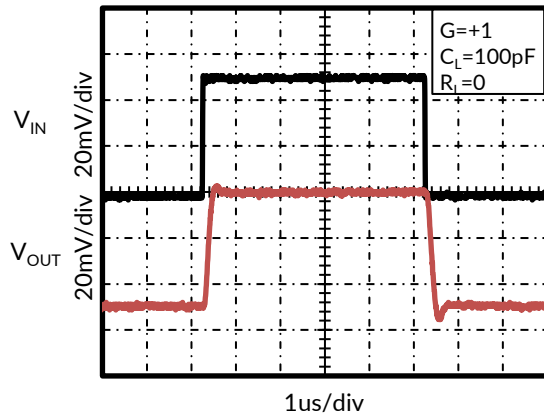


Figure 7. 50mV Small-Signal Step Response

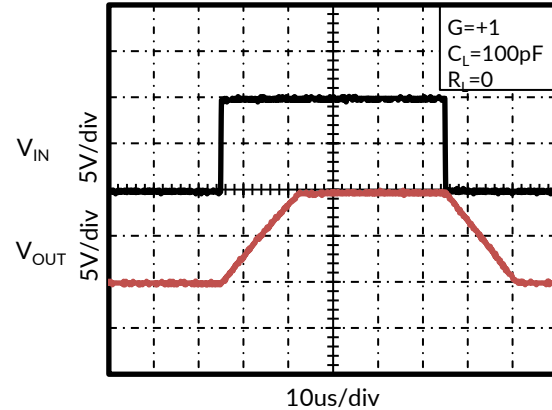


Figure 8. 10V Large-Signal Step Response

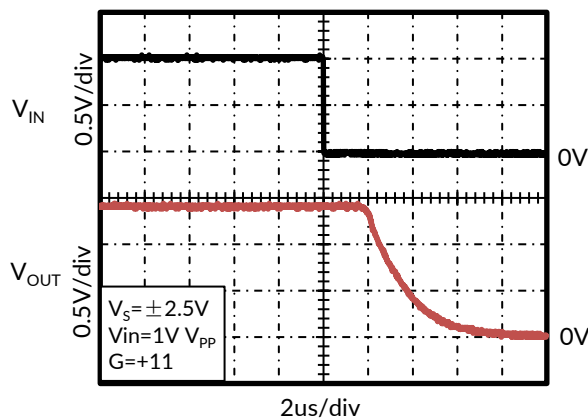


Figure 9. Positive Overload Recovery

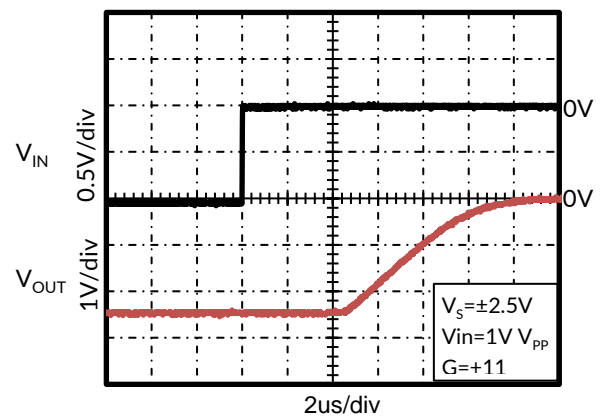


Figure 10. Negative Overload Recovery

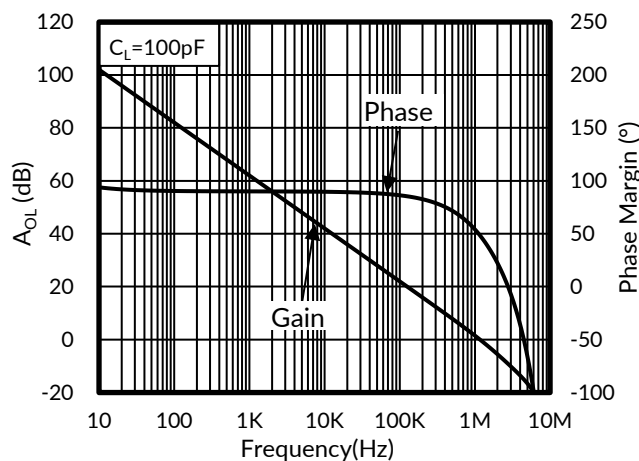


Figure 11. Open-Loop Gain and Phase Margin vs Frequency

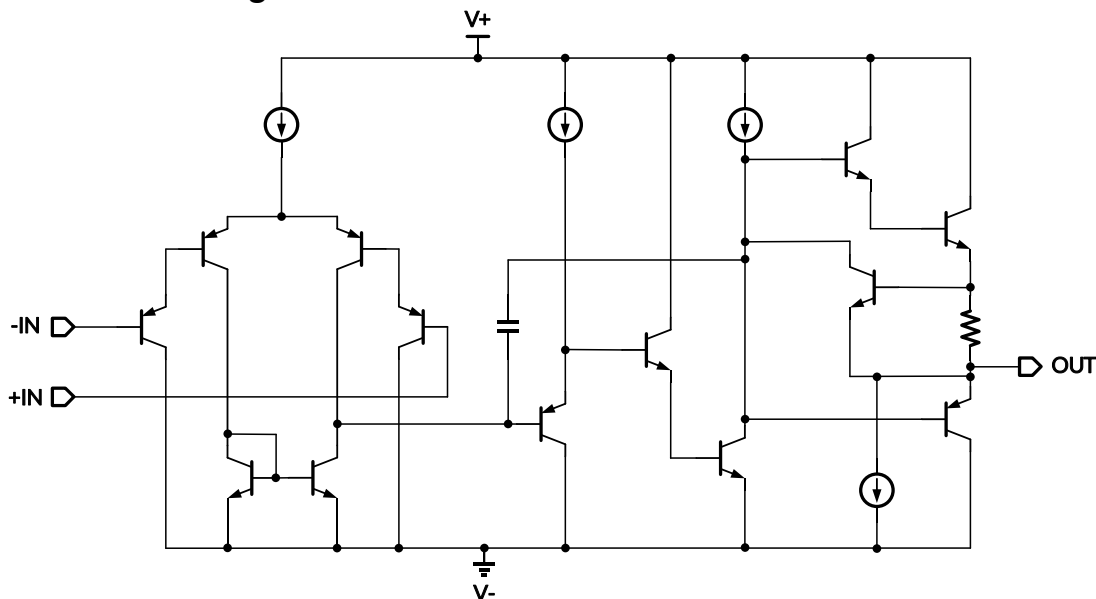
8 Detailed Description

8.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in Recommended Operating Conditions and V_S is at least 1.5V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5V supply used in digital systems and easily can provide the required interface electronics without additional $\pm 5V$ supplies.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2MHz unity-gain bandwidth.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5V/ μ s slew rate.

8.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_S - 1.5V$ ($V_S - 2V$ across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3V below V_- then input current should be limited to 1mA and the output phase is undefined.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

9 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

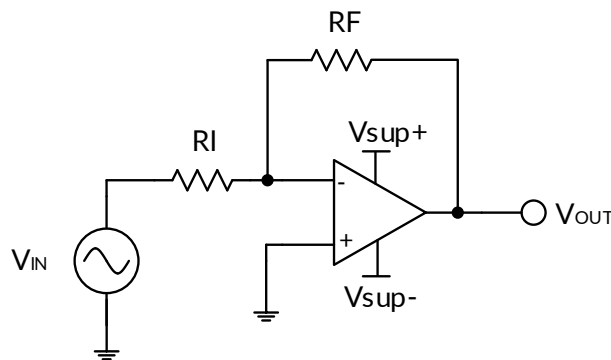


Figure 12. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of $\pm 0.5V$ to $\pm 1.8V$. Setting the supply at $\pm 12V$ is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamperes range. This ensures the part does not draw too much current. This example uses $10k\Omega$ for R_I which means $36k\Omega$ is used for R_F . This was determined by Equation 3.

$$A_v = - \frac{R_F}{R_I} \quad (3)$$

10 Power Supply Recommendations

CAUTION: Supply voltages larger than specified in the recommended operating region can permanently damage the device.

Place 0.1 μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see LAYOUT.

11 LAYOUT

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 14, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

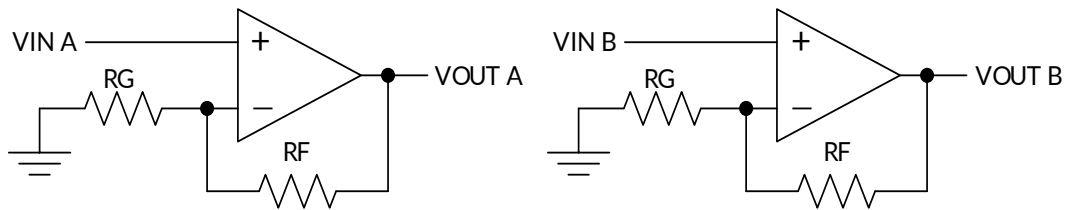


Figure 13. Schematic Representation

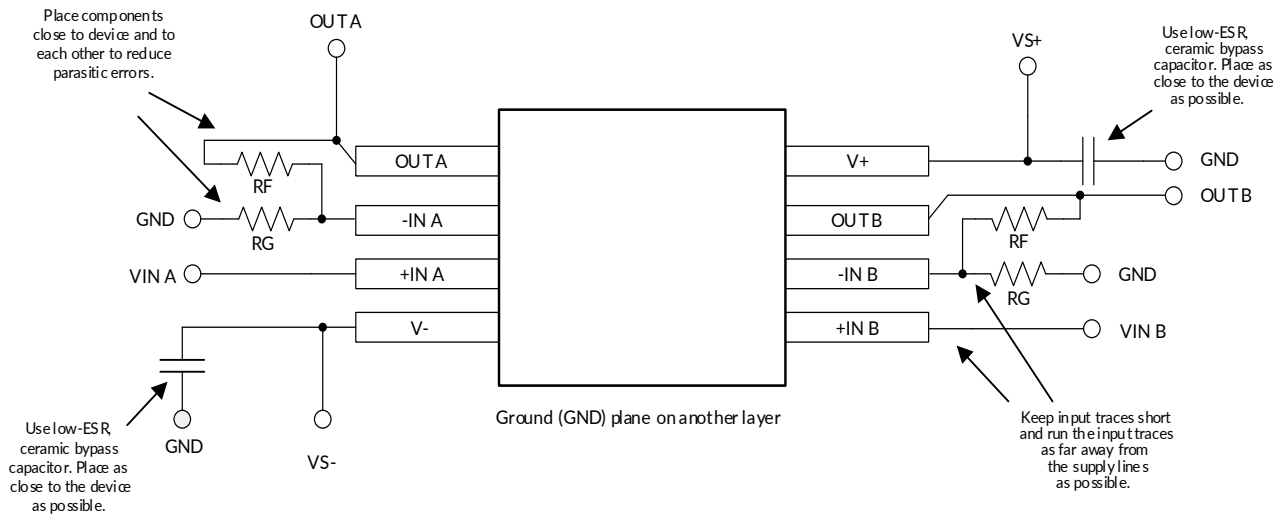
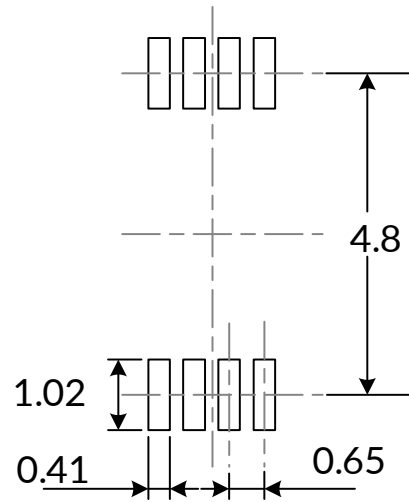
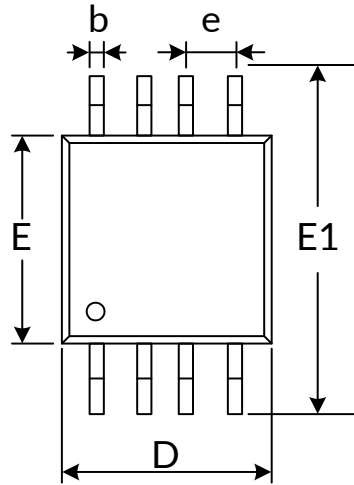


Figure 14. Layout Recommendation

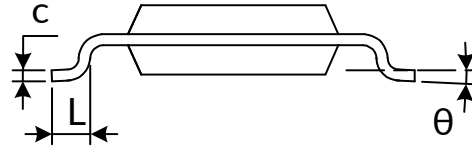
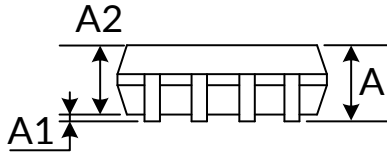
NOTE: Layout Recommendations have been shown for dual op-amp only, follow similar precautions for Single and four.

12 PACKAGE OUTLINE DIMENSIONS

MSOP-8 ⁽³⁾



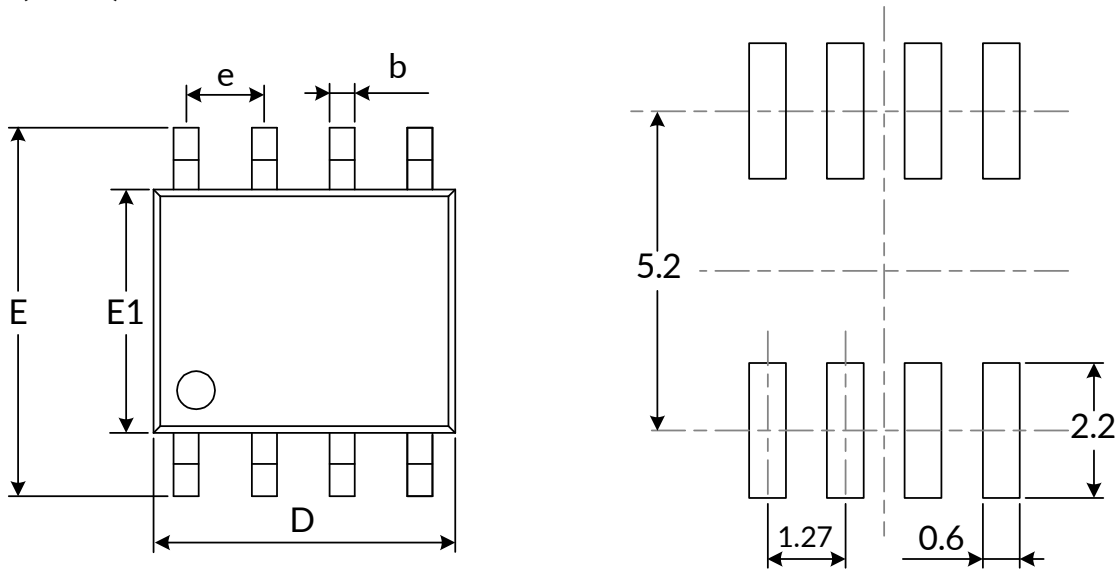
RECOMMENDED LAND PATTERN (Unit: mm)



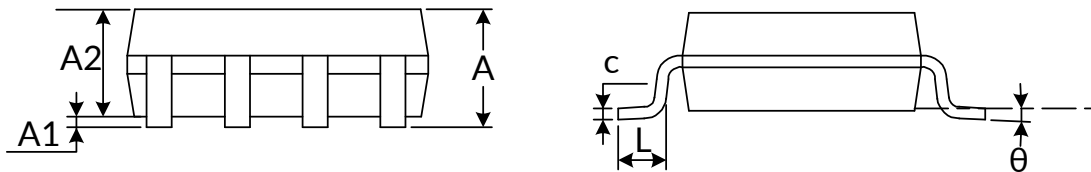
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D ⁽¹⁾	2.900	3.100	0.114	0.122
e	0.650(BSC) ⁽²⁾		0.026(BSC) ⁽²⁾	
E ⁽¹⁾	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

SOIC-8(SOP8) ⁽³⁾


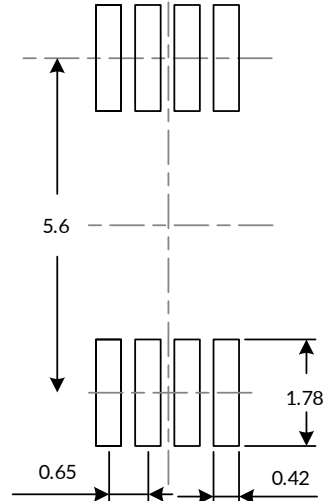
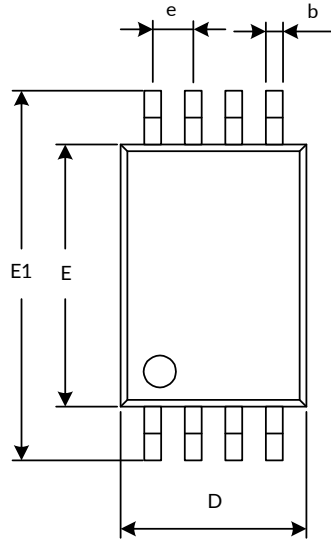
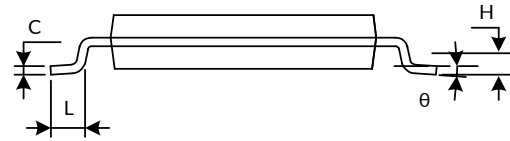
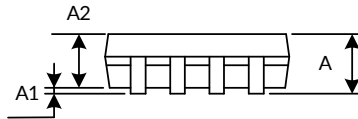
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D ⁽¹⁾	4.800	5.000	0.189	0.197
e	1.270(BSC) ⁽²⁾		0.050(BSC) ⁽²⁾	
E	5.800	6.200	0.228	0.244
E1 ⁽¹⁾	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP-8⁽³⁾

RECOMMENDED LAND PATTERN (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D ⁽¹⁾	2.900	3.100	0.114	0.122
E ⁽¹⁾	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 (BSC) ⁽²⁾		0.026 (BSC) ⁽²⁾	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

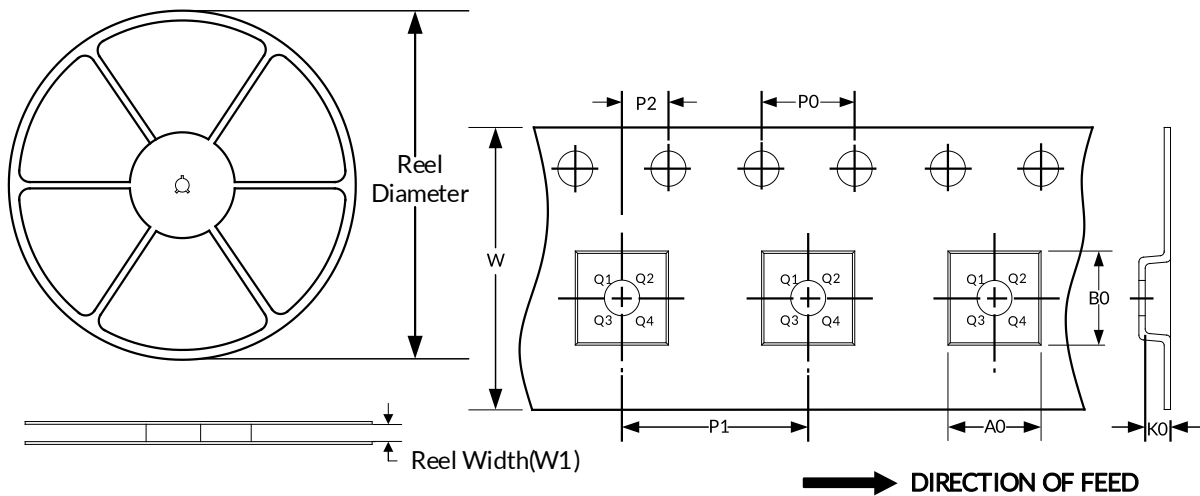
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8(SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TSSOP-8	13"	12.4	6.90	3.45	1.65	4.0	8.0	2.0	12.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

IMPORTANT NOTICE AND DISCLAIMER

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.