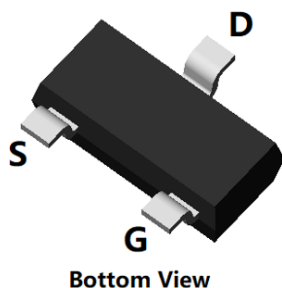
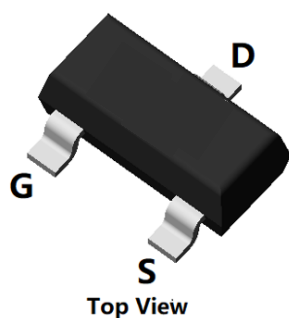
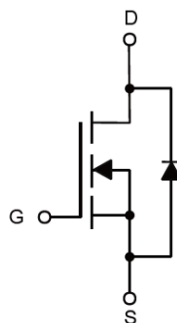


BSS138

N-Channel Enhancement Mode Field Effect Transistor



SOT-23



Product Summary

• V_{DS}	50V
• I_D	340mA
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<2.5ohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<3.0ohm

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	50	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^{\circ}C$ @ Steady State	I_D	340	mA
	$T_A=70^{\circ}C$ @ Steady State		272	
Pulsed Drain Current ^A		I_{DM}	1.5	A
Total Power Dissipation @ $T_A=25^{\circ}C$		P_D	350	mW
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	357	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
BSS138	F2	SS.	3000	30000	120000	7" reel

BSS138

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	50			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =50V,V _{GS} =0V			0.5	μA
Gate-Body Leakage Current	I _{GSS1}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
	I _{GSS2}	V _{GS} = ±10V, V _{DS} =0V			±50	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.8	1.2	1.6	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =300mA		1.1	2.5	Ω
		V _{GS} = 4.5V, I _D =200mA		1.2	3.0	
Diode Forward Voltage	V _{SD}	I _S =300mA,V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				340	mA
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V,f=1MHZ		28.5		pF
Output Capacitance	C _{oss}			2.7		
Reverse Transfer Capacitance	C _{rss}			1.78		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =25V,I _D =0.3A		1.7		nC
Gate-Source Charge	Q _{gs}			0.4		
Gate-Drain Charge	Q _{gd}			0.24		
Reverse Recovery Charge	Q _{rr}	I _F =0.3A, di/dt=-100A/us		2.65		
Reverse Recovery Time	t _{rr}			12.2		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V,V _{DD} =25V, I _D =300mA, R _{GEN} =6Ω		2.6		ns
Turn-on Rise Time	t _r			18.8		
Turn-off Delay Time	t _{D(off)}			9.7		
Turn-off fall Time	t _f			47		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

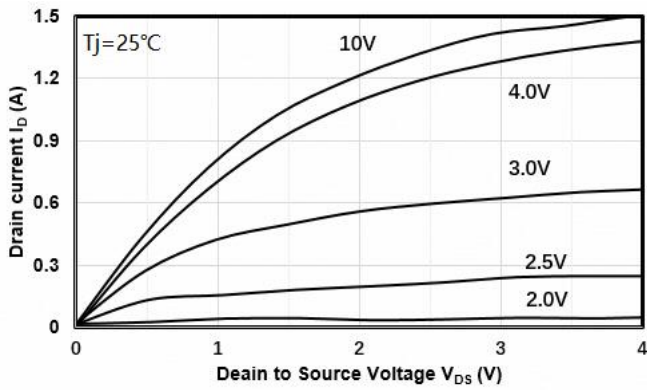


Figure1. Output Characteristics

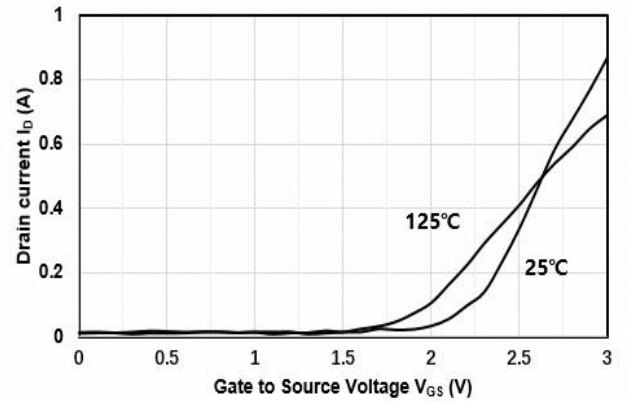


Figure2. Transfer Characteristics

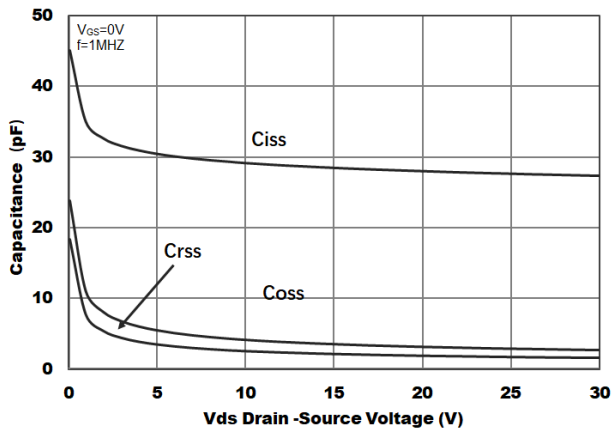


Figure3. Capacitance Characteristics

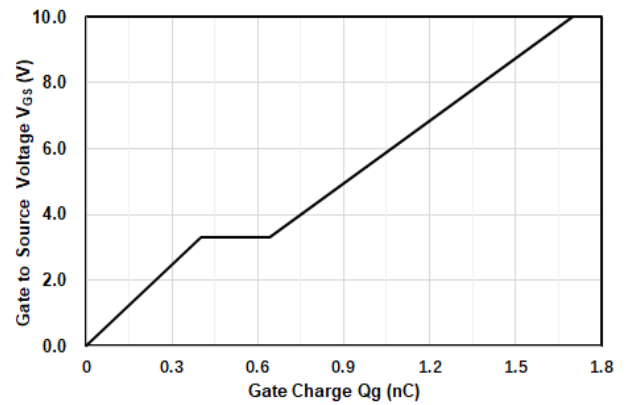


Figure4. Gate Charge

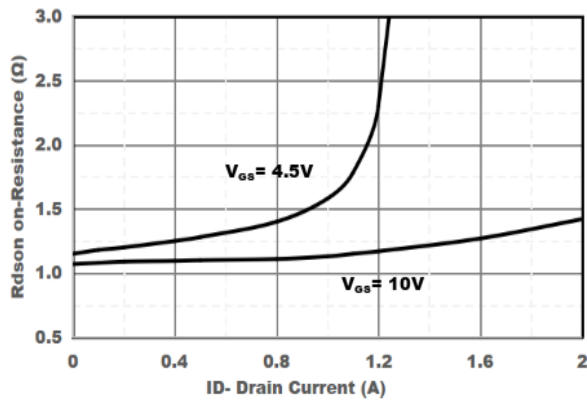


Figure5. Drain-Source on Resistance

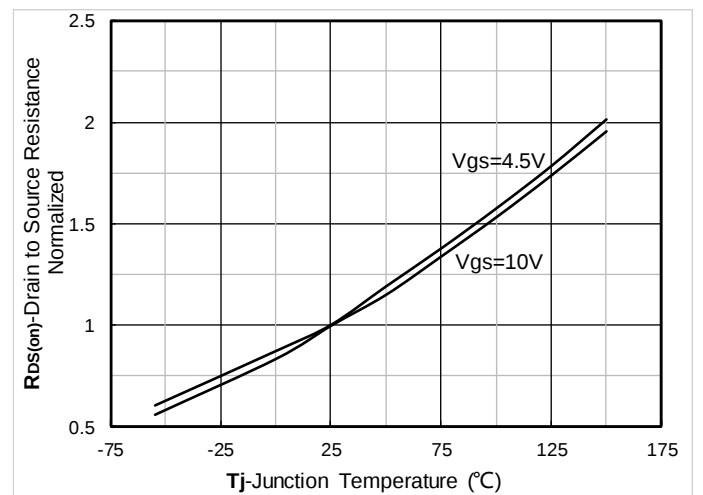


Figure6. Drain-Source on Resistance

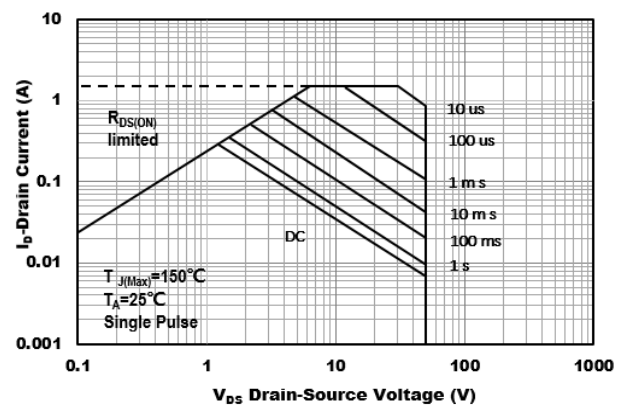


Figure7. Safe Operation Area

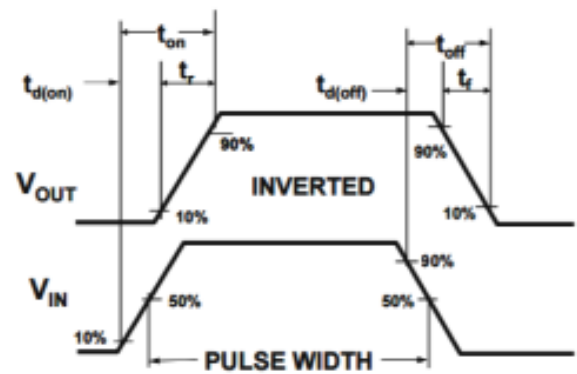


Figure8. Switching wave

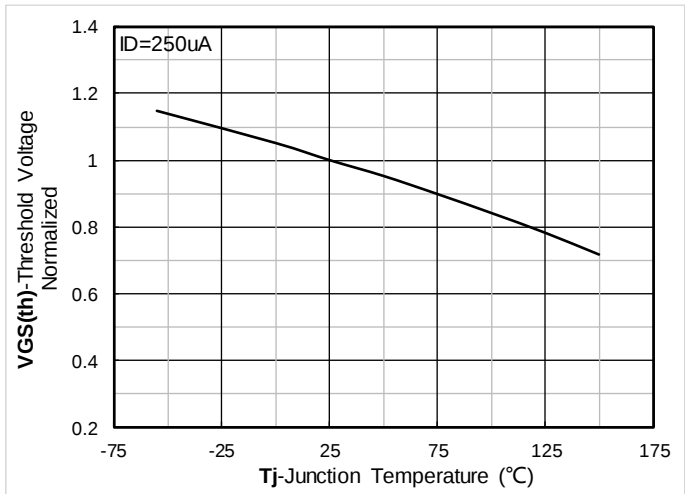


Figure 9. Normalized Threshold voltage

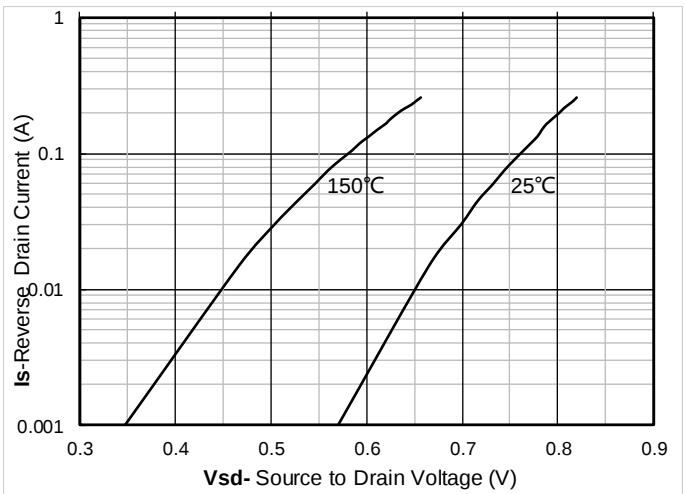
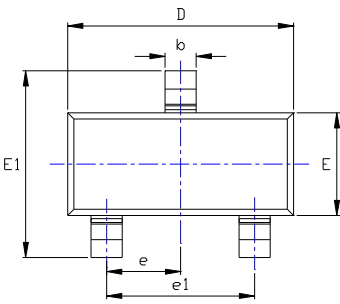
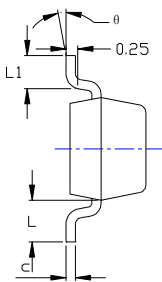


Figure 10. Forward characteristics of reverse diode

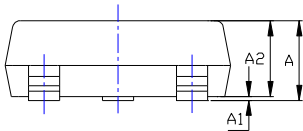
■ SOT-23 Package information



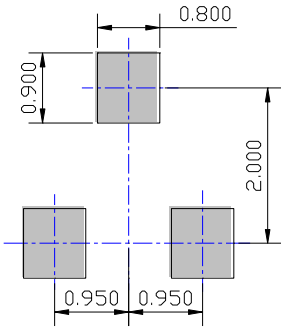
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.200	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.