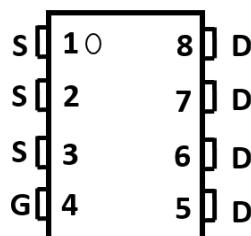
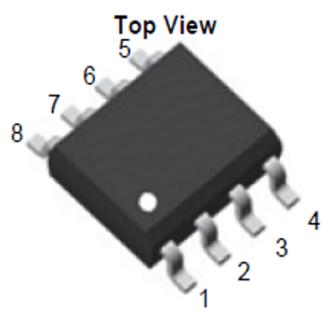
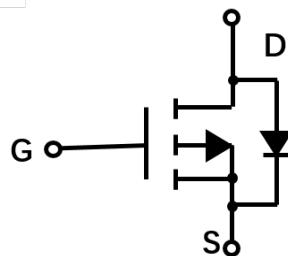


P-Channel Enhancement Mode Field Effect Transistor



SOP-8



Product Summary

- V_{DS} -20V
- I_D -13A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 17mohm
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) < 20mohm
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) < 26mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A=25^\circ\text{C}$ @ Steady State	I_D	-13	A
	$T_A=70^\circ\text{C}$ @ Steady State		-10.4	
Pulsed Drain Current ^A		I_{DM}	-55	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$		P_D	3.0	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
ZXS2022A	F2	Q2022	4000	8000	64000	13" reel

ZXS2022A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=0\text{V}, T_c=25^\circ\text{C}$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 10\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}= -4.5\text{V}, I_{\text{D}}=-10\text{A}$		10	17	$\text{m}\Omega$
		$V_{\text{GS}}= -2.5\text{V}, I_{\text{D}}=-6.5\text{A}$		13	20	
		$V_{\text{GS}}= -1.8\text{V}, I_{\text{D}}=-4.0\text{A}$		18	26	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=-13\text{A}, V_{\text{GS}}=0\text{V}$		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_{S}				-13	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-10\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		2992		pF
Output Capacitance	C_{oss}			330		
Reverse Transfer Capacitance	C_{rss}			272		
Switching Parameters						
Total Gate Charge	Q_{g}	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-9.1\text{A}$		72.8		nC
Gate Source Charge	Q_{gs}			6.6		
Gate Drain Charge	Q_{gd}			10.1		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=-6\text{A}, dI/dt=100\text{A/us}$		34		ns
Reverse Recovery Time	t_{rr}			67		
Turn-on Delay Time	$t_{\text{D(on)}}$			7		
Turn-on Rise Time	t_{r}	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-6\text{A}, R_{\text{GEN}}=2.5\Omega$		33		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			130		
Turn-off Fall Time	t_{f}			132		

A. Pulse Test: Pulse Width $\leq 300\text{us}$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

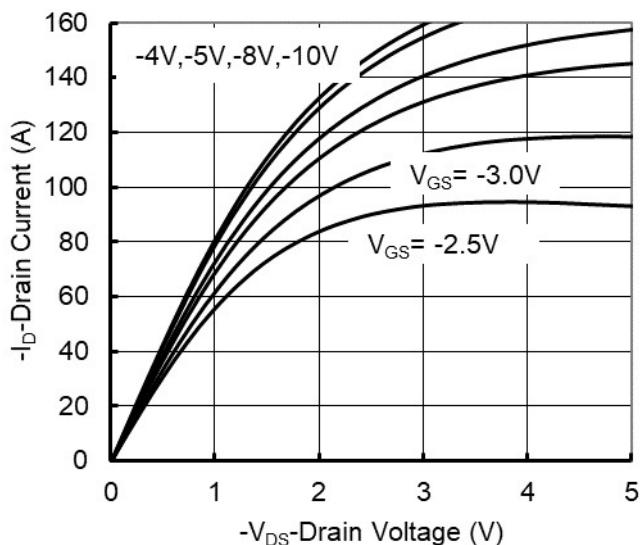


Figure 1. Output Characteristics

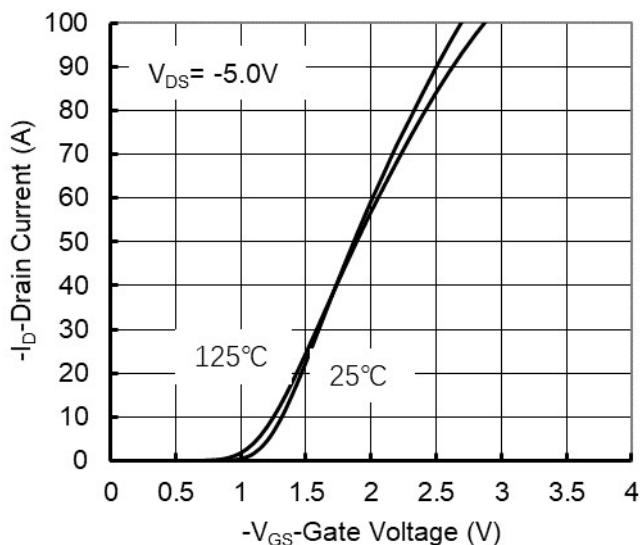


Figure 2. Transfer Characteristics

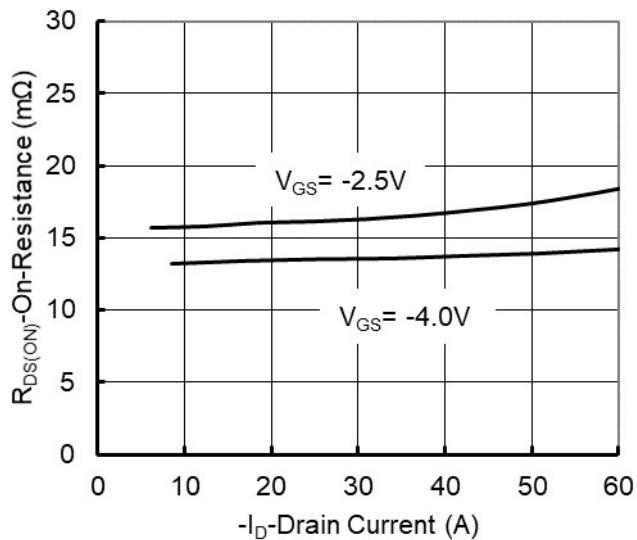


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

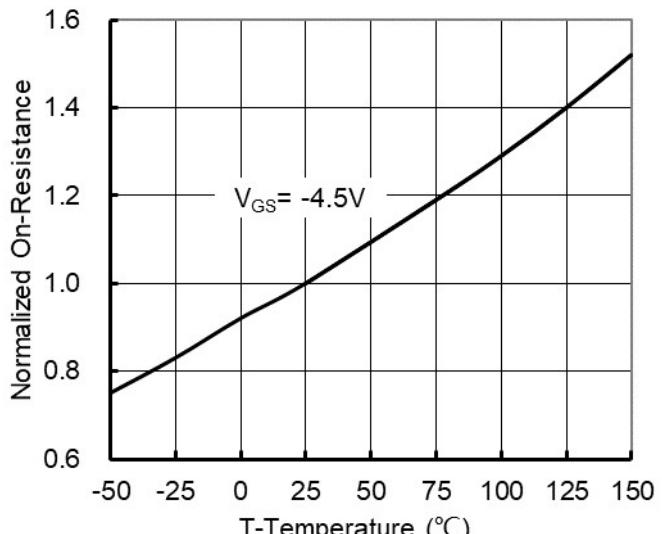


Figure 4. On-Resistance vs. Junction Temperature

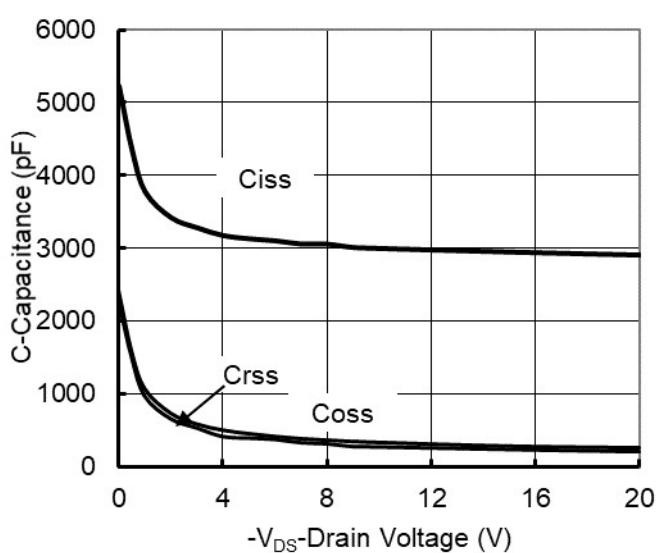


Figure 5. Capacitance Characteristics

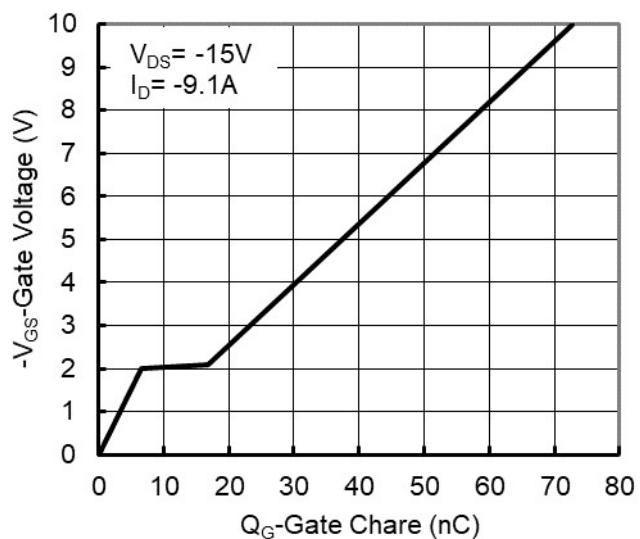


Figure 6. Gate Charge

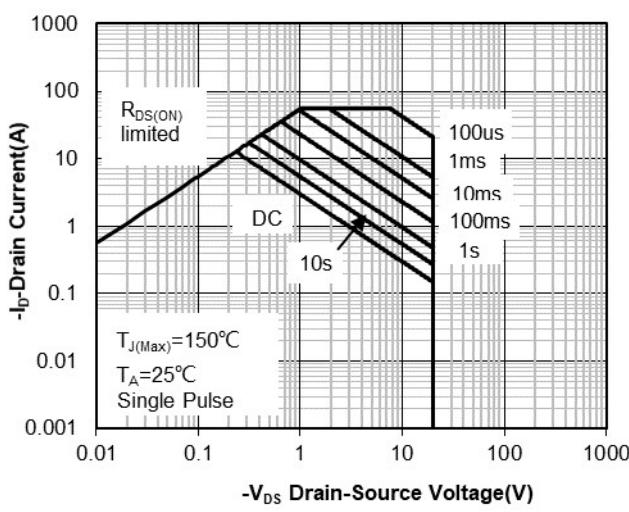


Figure 7. Safe Operation Area

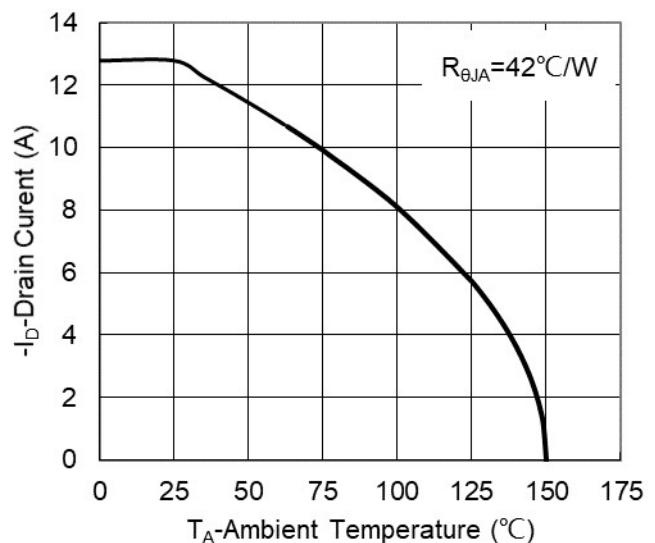


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

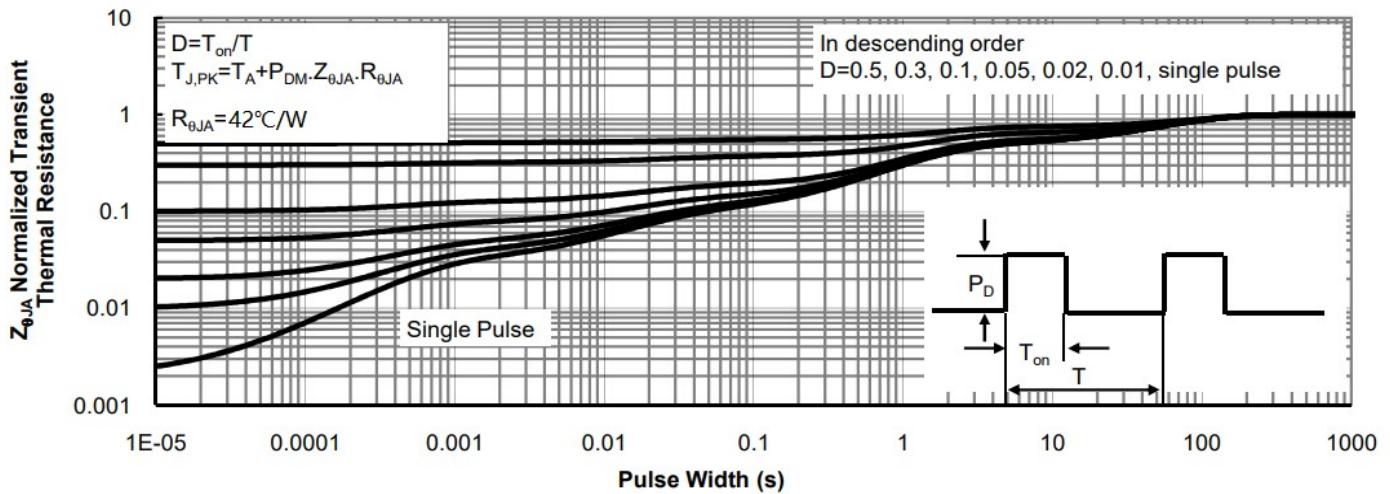
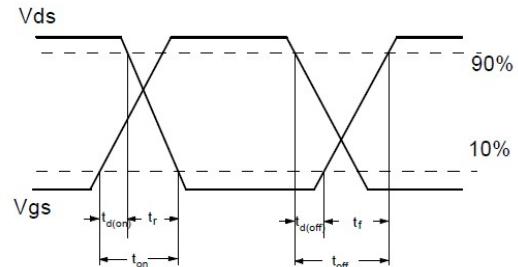
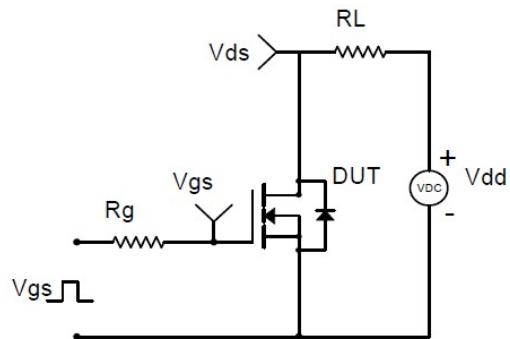
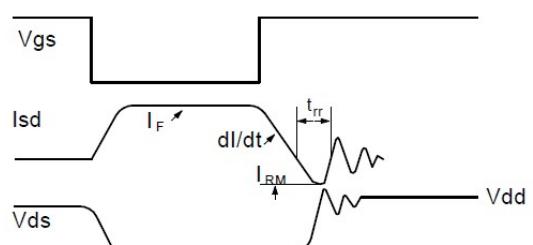
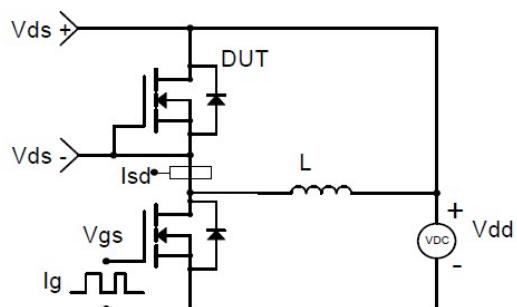


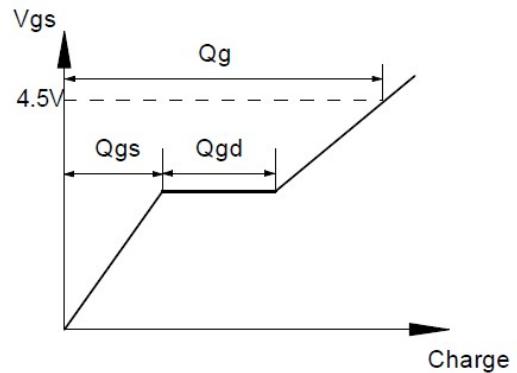
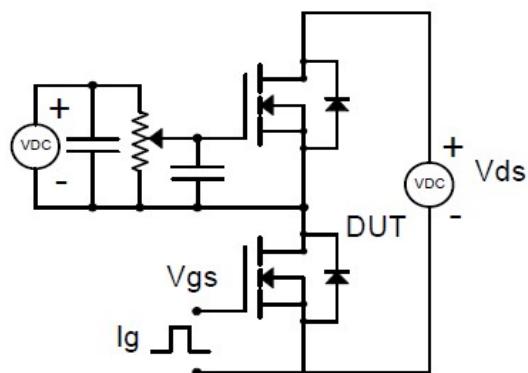
Figure 9. Normalized Maximum Transient Thermal Impedance



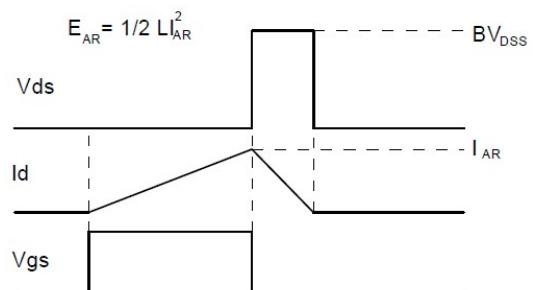
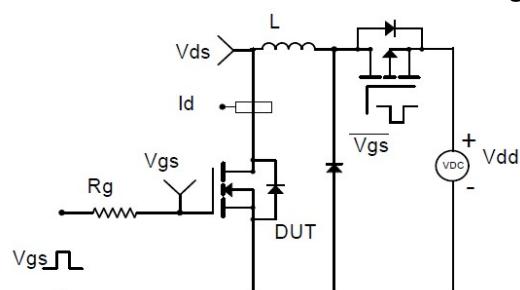
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

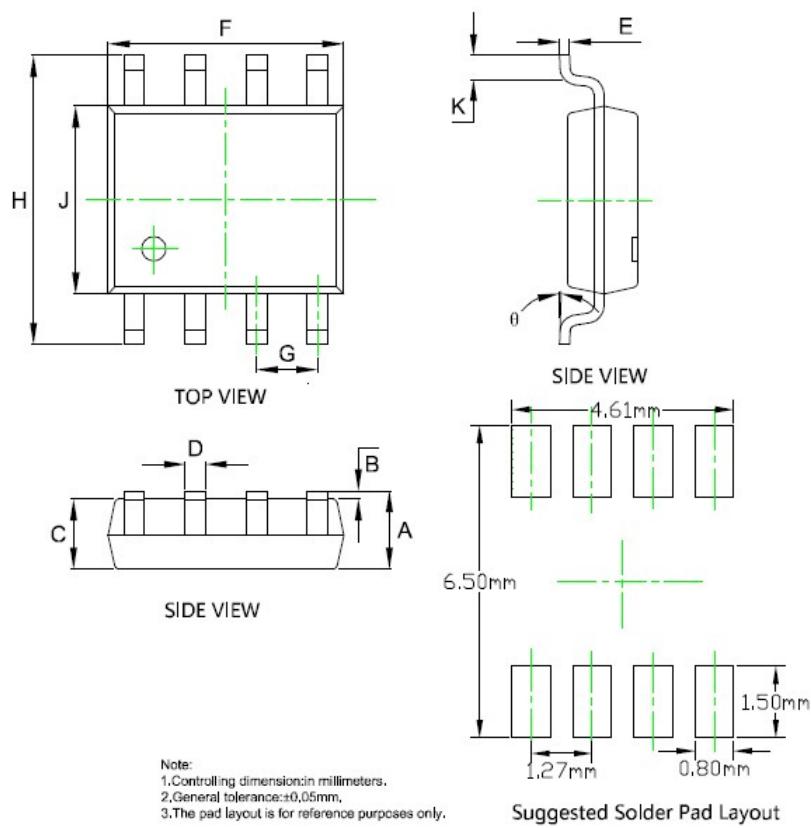


Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
A	MIN. 0.053	MAX. 0.069	MIN. 1.350	MAX. 1.750
B	MIN. 0.004	MAX. 0.010	MIN. 0.100	MAX. 0.250
C	MIN. 0.053	MAX. 0.061	MIN. 1.350	MAX. 1.550
D	MIN. 0.013	MAX. 0.020	MIN. 0.330	MAX. 0.510
E	MIN. 0.007	MAX. 0.010	MIN. 0.170	MAX. 0.250
F	MIN. 0.189	MAX. 0.197	MIN. 4.800	MAX. 5.000
G	0.050BSC		1.270BSC	
H	MIN. 0.228	MAX. 0.244	MIN. 5.800	MAX. 6.200
J	MIN. 0.150	MAX. 0.157	MIN. 3.800	MAX. 4.000
K	MIN. 0.016	MAX. 0.050	MIN. 0.400	MAX. 1.270
θ	MIN. 0°	MAX. 8°	MIN. 0°	MAX. 8°