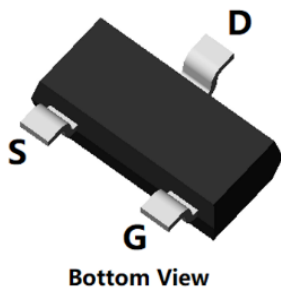
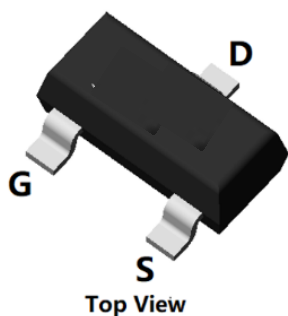
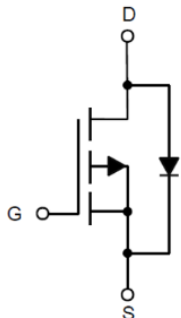


P-Channel Enhancement Mode Field Effect Transistor



SOT-23



Product Summary

- V_{DS} -15V
- I_D -5.6A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <34 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <44 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-1.8V$) <62 mohm

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|------------------|-----------------|----------|--------------|
| Drain-source Voltage | | V_{DS} | -15 | V |
| Gate-source Voltage | | V_{GS} | ± 10 | V |
| Drain Current | $T_A=25^\circ C$ | I_D | -5.6 | A |
| | $T_A=70^\circ C$ | | -4.5 | |
| Pulsed Drain Current ^A | | I_{DM} | -23 | A |
| Total Power Dissipation @ $T_A=25^\circ C$ Steady State | | P_D | 1.2 | W |
| Thermal Resistance Junction-to-Ambient ^B | | $R_{\theta JA}$ | 105 | $^\circ C/W$ |
| Junction and Storage Temperature Range | | T_J, T_{STG} | -55~+150 | $^\circ C$ |

■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| ZXL2305A | F2 | 2305. | 3000 | 30000 | 120000 | 7" reel |

ZXL2305A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|---------------------|---|------|-------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} =0V, I _D =-250μA | -15 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =-15V, V _{GS} =0V | | | -1 | μA |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} =±10V, V _{DS} =0V | | | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} , I _D =-250μA | -0.4 | -0.62 | -1.0 | V |
| Static Drain-Source On-Resistance | R _{Ds(on)} | V _{GS} =-4.5V, I _D =-5.4A | | 23 | 34 | mΩ |
| | | V _{GS} =-2.5V, I _D =-4A | | 31 | 44 | |
| | | V _{GS} =-1.8V, I _D =-3A | | 44 | 62 | |
| Diode Forward Voltage | V _{SD} | I _S =-5.4A, V _{GS} =0V | | | -1.2 | V |
| Maximum Body-Diode Continuous Current | I _S | | | | -5.6 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =-9V, V _{GS} =0V, f=1MHZ | | 1010 | | pF |
| Output Capacitance | C _{oss} | | | 135 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 109 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =-4.5V, V _{DS} =-9V, I _D =-5.6A | | 11.0 | | nC |
| Gate-Source Charge | Q _{gs} | | | 2.2 | | |
| Gate-Drain Charge | Q _{gd} | | | 2.5 | | |
| Reverse Recovery Charge | Q _{rr} | I _F =-4A, di/dt=100A/us | | 4.4 | | |
| Reverse Recovery Time | t _{rr} | | | 25 | | |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =-4.5V, V _{DS} =-9V, I _D =-1A R _{GEN} =2.5Ω | | 8 | | ns |
| Turn-on Rise Time | t _r | | | 36 | | |
| Turn-off Delay Time | t _{D(off)} | | | 77 | | |
| Turn-off fall Time | t _f | | | 56 | | |

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{θJL} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

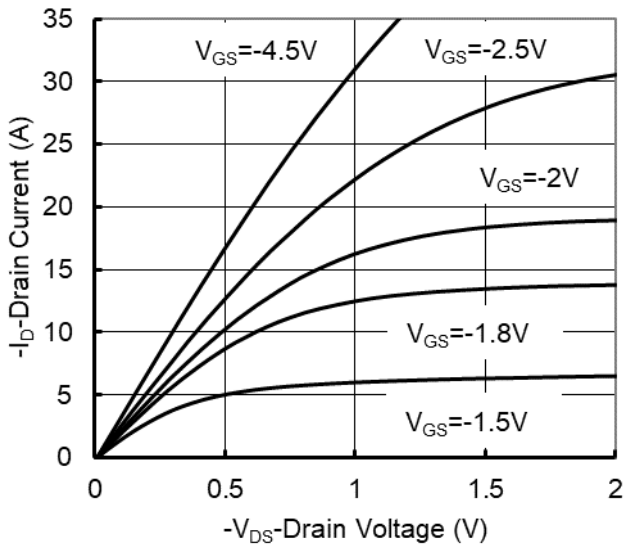


Figure1. Output Characteristics

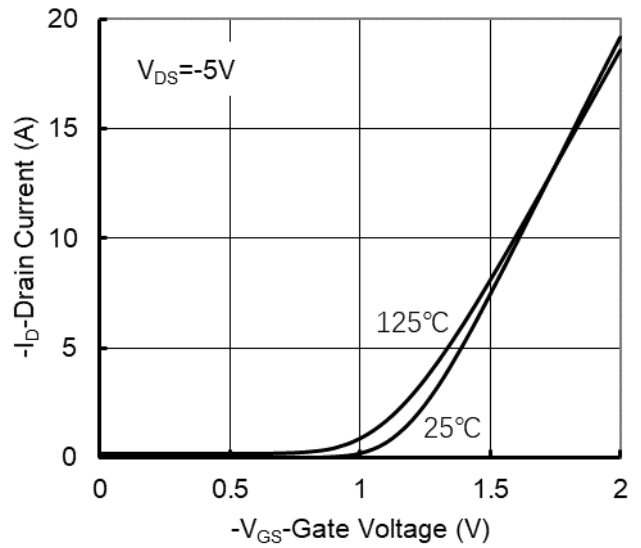


Figure2. Transfer Characteristics

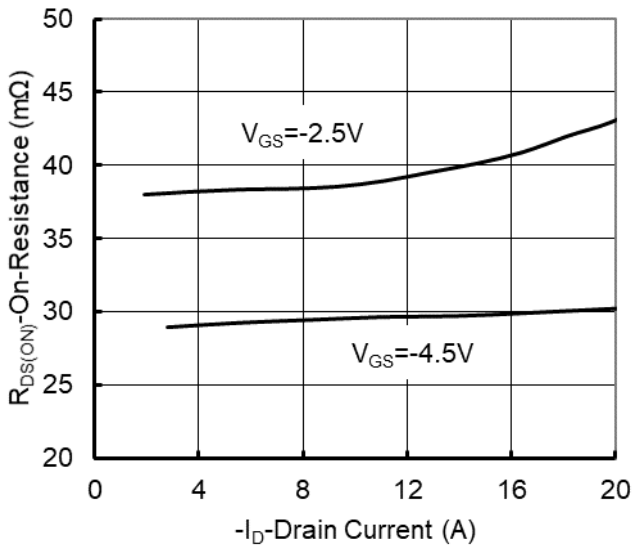


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

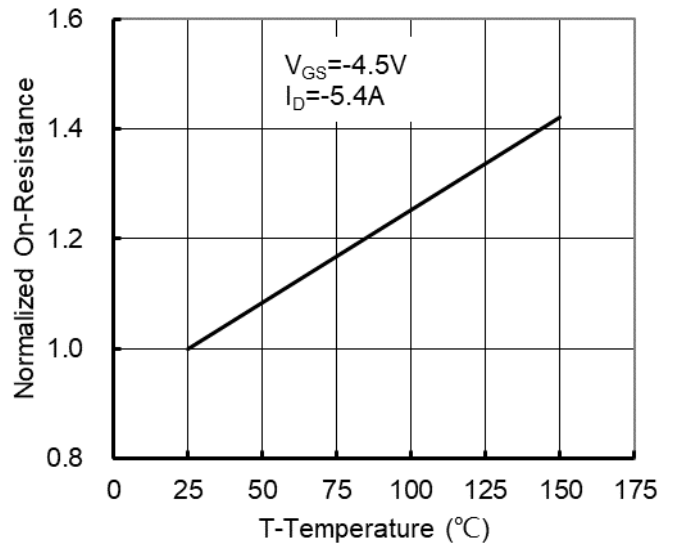


Figure 4: On-Resistance vs. Junction Temperature

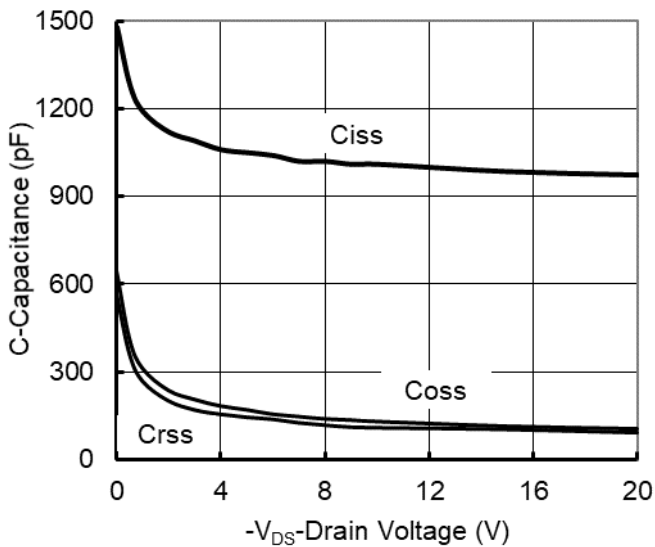


Figure5. Capacitance Characteristics

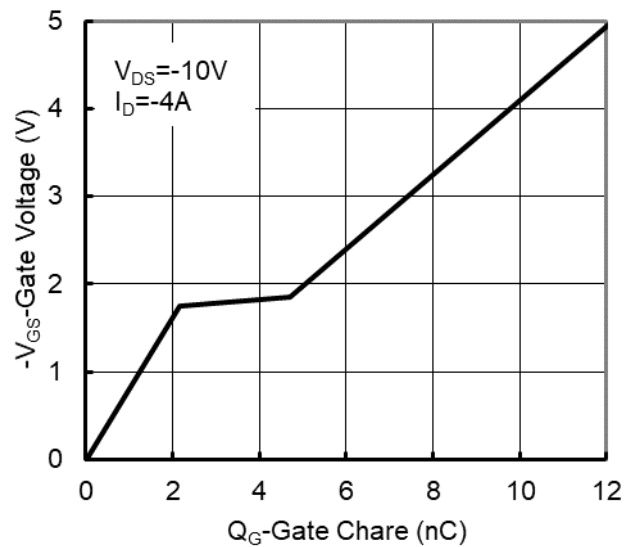


Figure6. Gate Charge

ZXL2305A

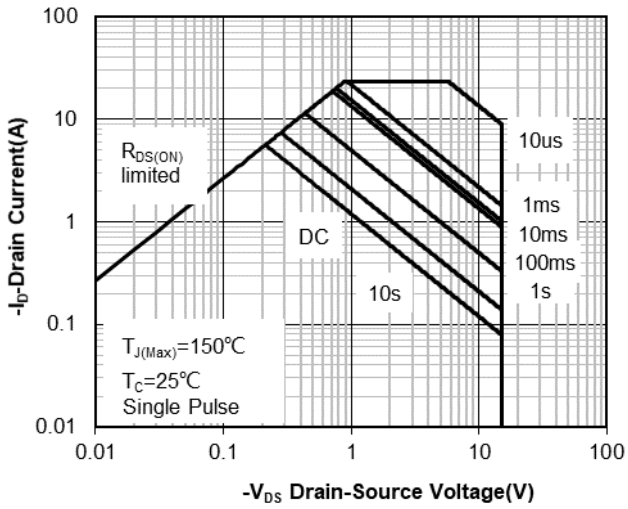


Figure7. Safe Operation Area

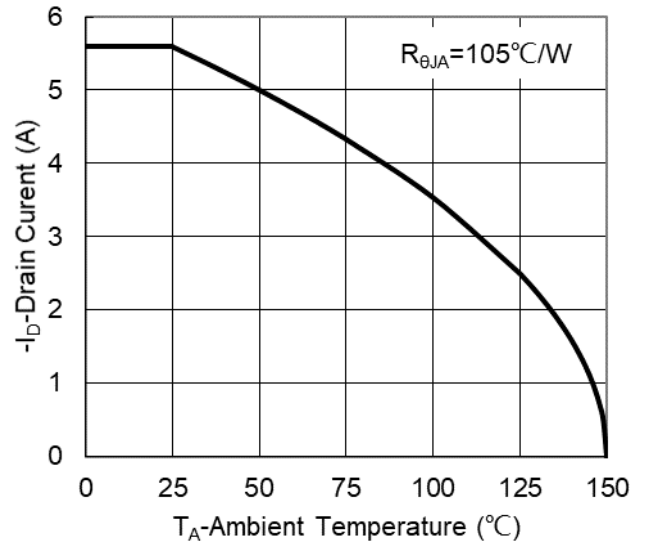


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

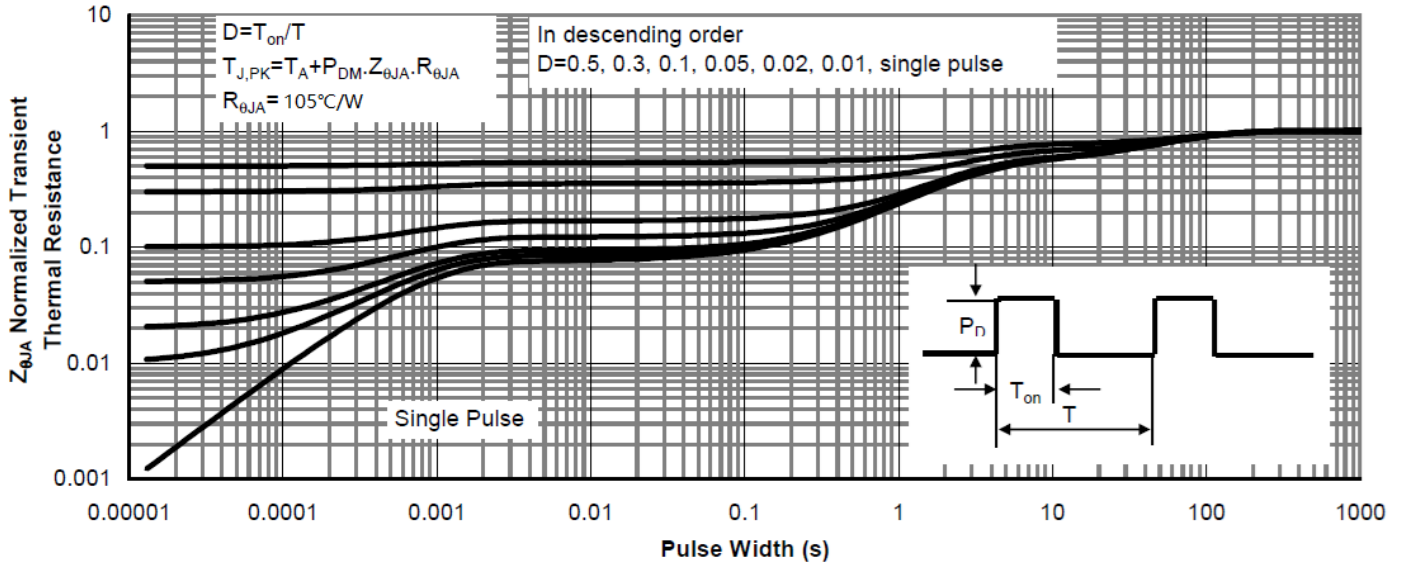
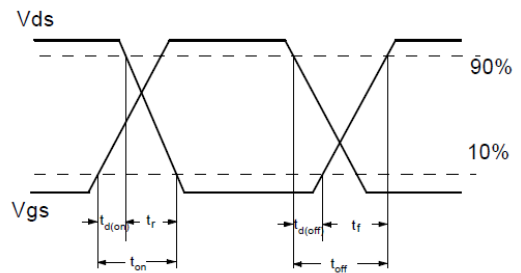
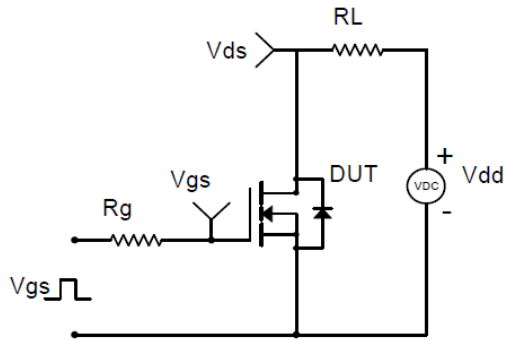
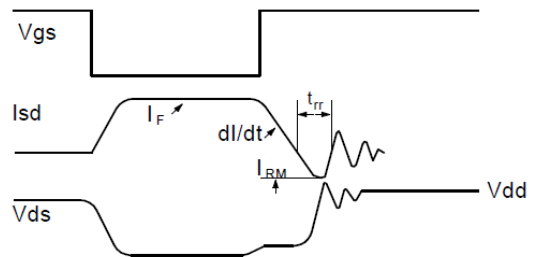
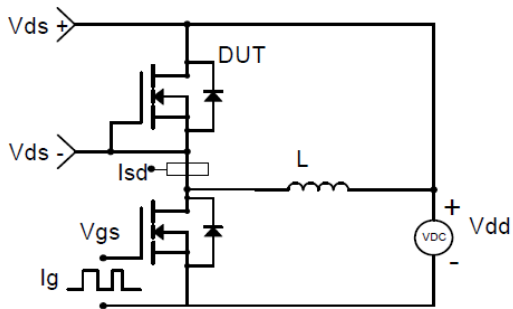


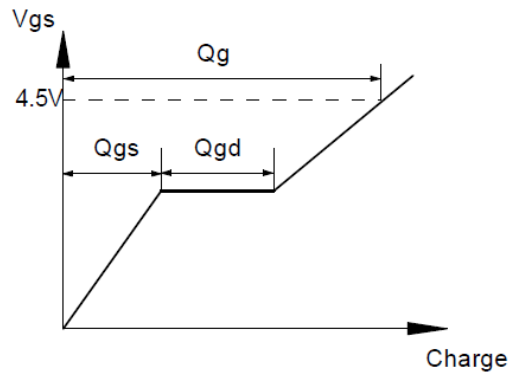
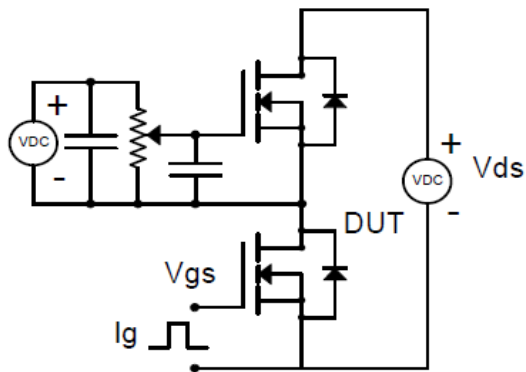
Figure9. Normalized Maximum Transient Thermal Impedance



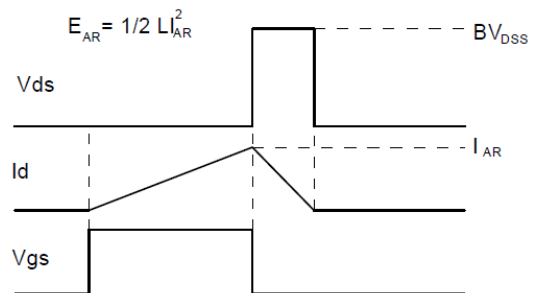
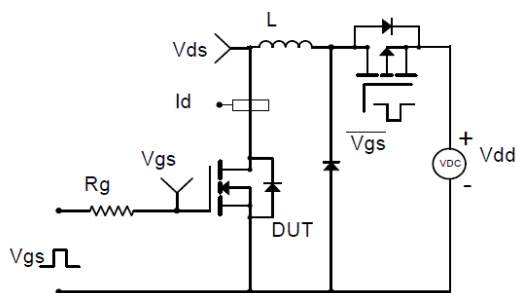
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



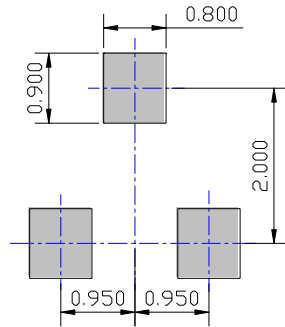
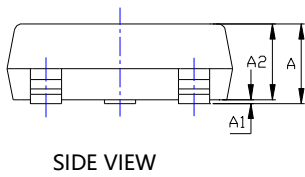
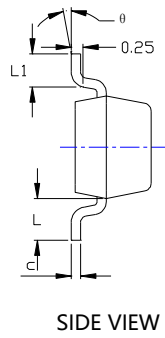
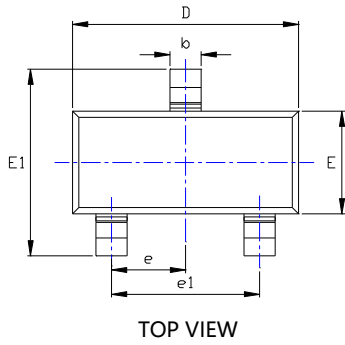
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

ZXL2305A

■ SOT-23 Package Information



UNIT: mm

| SYMBOL | DIMENSIONS | | | |
|--------|------------|-------|------------|-------|
| | INCHES | | Millimeter | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.035 | 0.045 | 0.900 | 1.150 |
| A1 | 0.000 | 0.004 | 0.000 | 0.100 |
| A2 | 0.035 | 0.041 | 0.900 | 1.050 |
| b | 0.012 | 0.020 | 0.300 | 0.500 |
| c | 0.004 | 0.008 | 0.100 | 0.200 |
| D | 0.110 | 0.118 | 2.800 | 3.000 |
| E | 0.047 | 0.055 | 1.200 | 1.400 |
| E1 | 0.089 | 0.100 | 2.250 | 2.550 |
| e | 0.037TYP | | 0.950TYP | |
| e1 | 0.071 | 0.079 | 1.800 | 2.000 |
| L | 0.022REF | | 0.550REF | |
| L1 | 0.012 | 0.200 | 0.300 | 0.500 |
| θ | 0° | 8° | 0° | 8° |

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.