IP179N/H Integrated 9 PHYceivers Ethernet Switch

(Advanced Switching Engine, LBAS® and 3.3/2.5/1.8V RGMII)

Features

- Family (Part Numbers)
  - IP179N (88Pins QFN)
    9 FE ports
    8 FE ports + 1 MAC w/ 1RMII
  - IP179H (128Pins LQFP)
    8 FE ports + 1 Giga MAC
- Advanced Ethernet Switching Engine support 2 operation modes
  - Normal Mode (Default)
  - IPC Mode
- MAC address up to 2K
- 1Mbits packet buffer memory
- Support 1552bytes maximum packet length
- Built in 9 port PHYceivers
- Each port can be configured to be 10Based-T, 100Base-TX
- Support IEEE802.3az at 100M Full Duplex
- Support Auto MDI-MDIX
- Support up to 3 optional Fiber ports
- IEEE802.1Q VLAN
  - Support 16 VLAN groups
  - Support Port-based/tagged-based VLAN
  - Support SVL/IVL
  - Support Insert and Remove Tag
- Class of Service
  - Port based, VLAN priority, IPv4 ToS, IPv6 DSCP
- QoS
  - Support 2-level priority queues per port WRR/SP
- Support Hardware IGMP v1/v2/v3 snooping
- Support STP, RSTP and MSTP
- Support LBAS® (Length/Link Based Auto Switch)
- Broadcast Storm Protection
- Support Special Tag and QinQ header
- Support Port Trunking (Link Aggregation)
- Support Port Mirror
- Power Management
  - Support APS (Auto Power Saving Mode) while Link-off
  - Support IEEE802.3az protocol based power saving
- IP179H supports 3.3/2.5/1.8V RGMII
- IP179HI supports 3.3/2.5V RGMII
- Support Statistics Counters
- Support WOL Interrupt Pin
- 85nm Process

General Description

The IP179N/H is a professional high-end SoC targeted for the Ethernet switch (w/ or w/o POE chips) or NVR application. This SoC is built in with an advanced switch engine, aiming to provide high-quality imagery output. Other built-in IPs, included a low power 9-port fast Ethernet transceivers, SSRAM, regulator, ESD protection and etc.

The built-in transceivers, all complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. These transceivers were designed under DSP approach and produced with 85nm technology, hence the high noise immunity and robust performance.

The switch controller of IP179N/H is designed to operate under store and forward mode.

It supports up to 2K MAC addresses. These tables are accessible through MII register. The address table can configure either “2K unicast addresses” or “1K unicast addresses and 1K multicast addresses“. Rich control and management features supported, included IEEE 802.1Q, IGMP Snooping, QoS and etc.

As an advanced Ethernet Switch controller, IP179N/H supports 2 operation modes to serve different application requirements precisely, Normal mode (Best quality for the down/up-load stream both) and IPC mode (Best efforts for the upload stream data).

Beside this, considering the distance problem that could be generated while installing a far away (> 100meters) IP CAM to link with the Switch device. IP179N/H supports the LBAS function to handle/fix this situation.

All of the functions that described above, an external MAC/CPU can monitor or configure them by accessing MII registers through MDC/MDIO that IP179N/H supported.

Table of Contents

Revision History

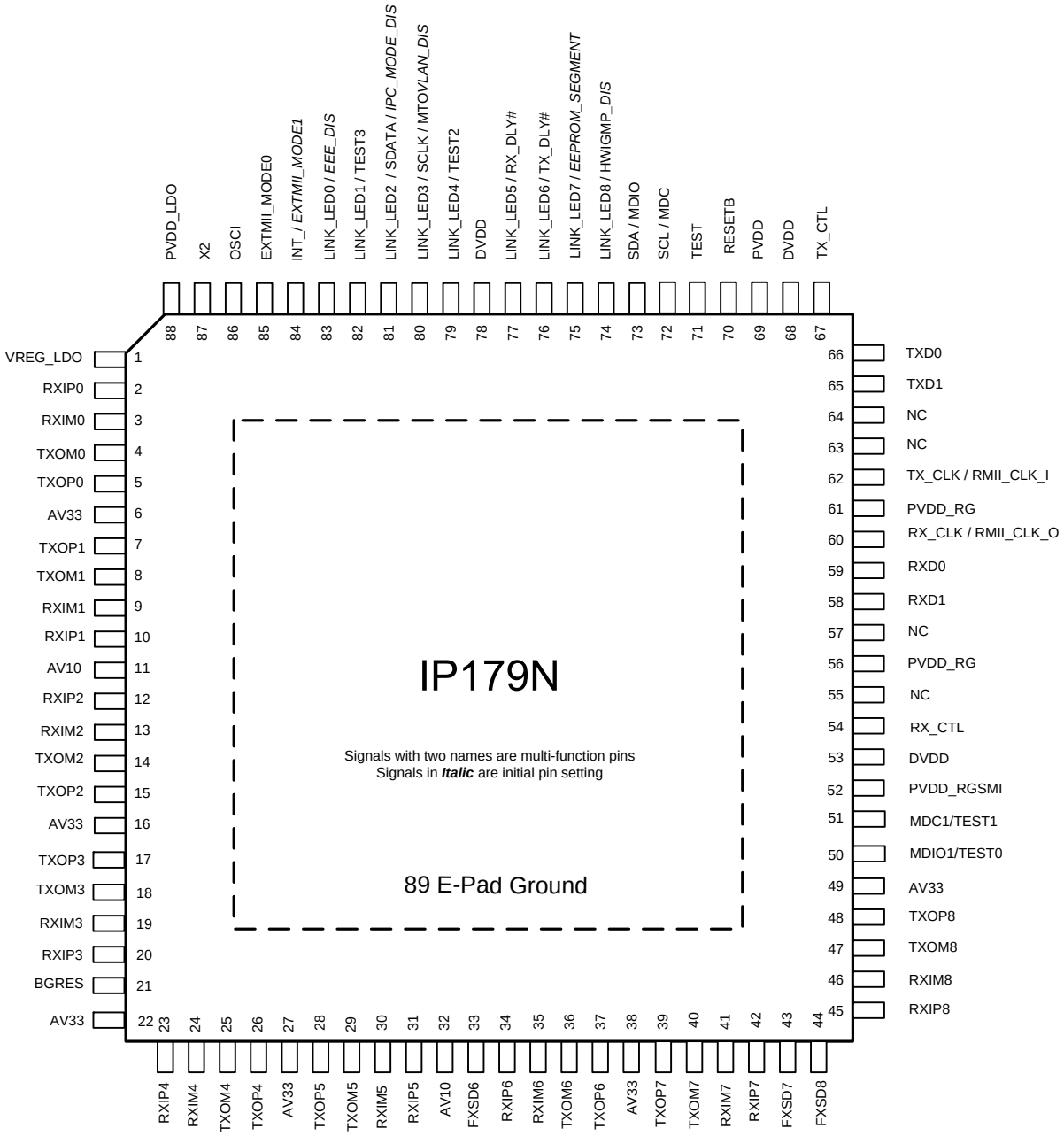
Revision #	Change Description
IP179M/N/H-DS-R01	Initial release
IP179M/N/H-DS-R02	1. Modify the default value of registers. 2. Modify the IP179N/H Pin diagrams.
IP179N/H-DS-R03	Remove IP179M model and related information.
IP179N/H-DS-R04	1. Modify the MII page6 register 16 description. 2. Remove the MII page7 register 16. 3. Remove the IP179H RMII1 application and related information. 4. Remove the loop detection function. 5. Modify the serial LED mode circuit.
IP179N/H-DS-R05	Modify the X1 input low/high voltage.
IP179N/H-DS-R06	1. Add the spanning tree description. 2. Add the special tag description. 3. Add the MAC/IP table description. 4. Add the MDI/MDIX control register.
IP179N/H-DS-R07	1. Add 1Mbits packet buffer memory description. 2. Modify the INT_ type. 3. Modify the WOL control register.
IP179N/H-DS-R08	1. Add 1552bytes maximum packet length feature. 2. Modify the default VLAN information register. 3. Modify the default driving current register. 4. Modify the external MII0 pins description. 5. Modify the function pins description. 6. Modify the EEPROM/SMI pins description.
IP179N/H-DS-R09	1. Add 3.3V SFP BOM. 2. Modify the P_{IDLE} Power consumption.

Disclaimer

This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

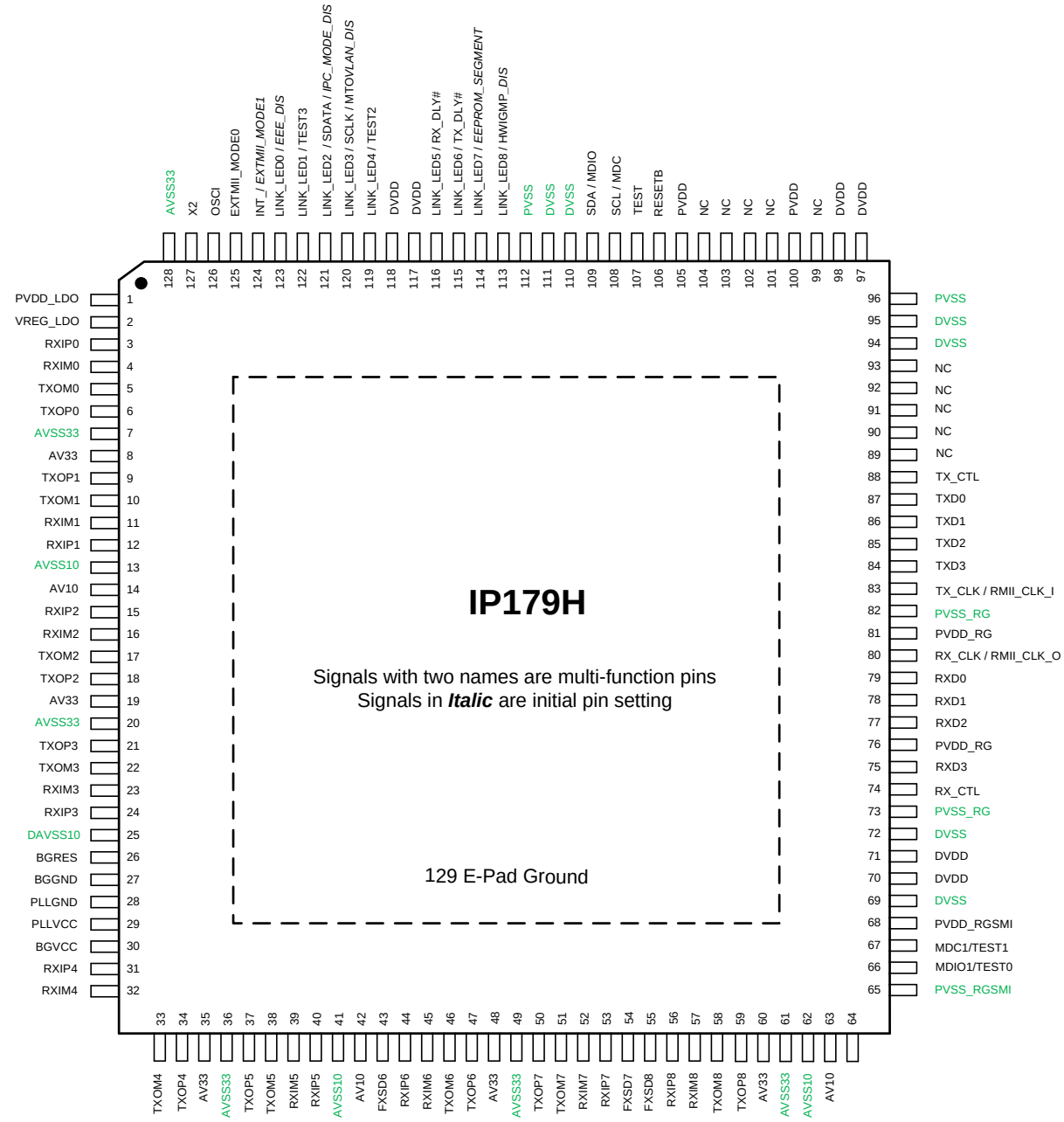
1 Pin Diagram

1.1 IP179N Pin Diagram (QFN88)



Exposed pad (pad 89) is system GND, must be soldered to PCB ground plane
Figure 1. Pin Diagram (IP179N)

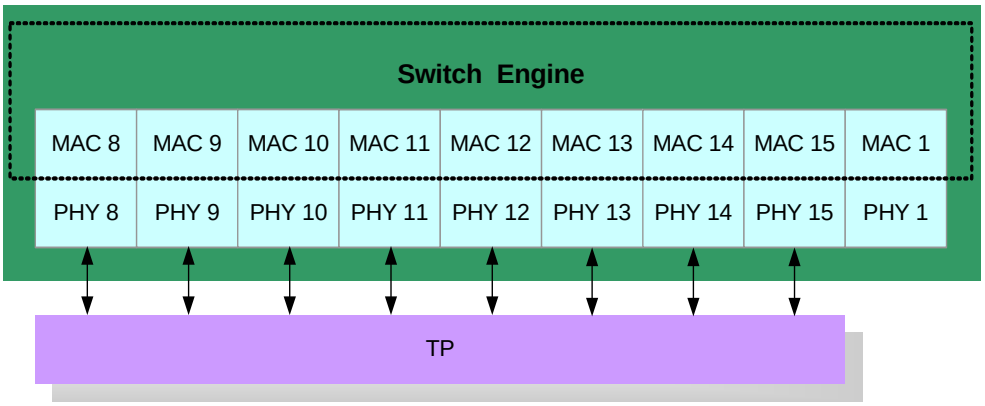
1.2 IP179H Pin Diagram (LQFP128)



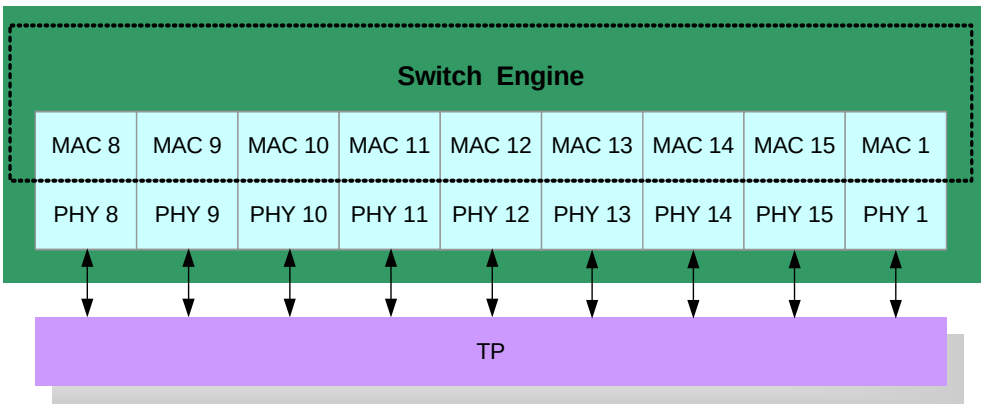
Exposed pad (pad 129) is system GND, must be soldered to PCB ground plane
Figure 2. Pin Diagram (IP179H)

2 Application Diagram

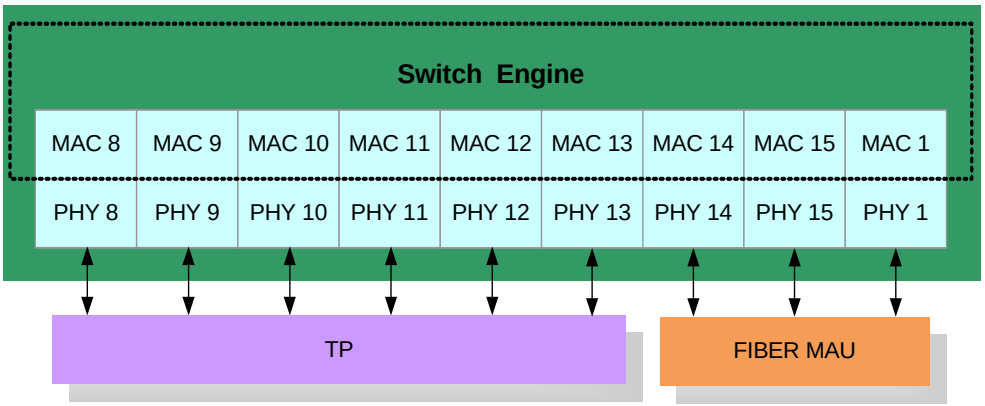
IP179N, 8 FE-TP Ports Switch



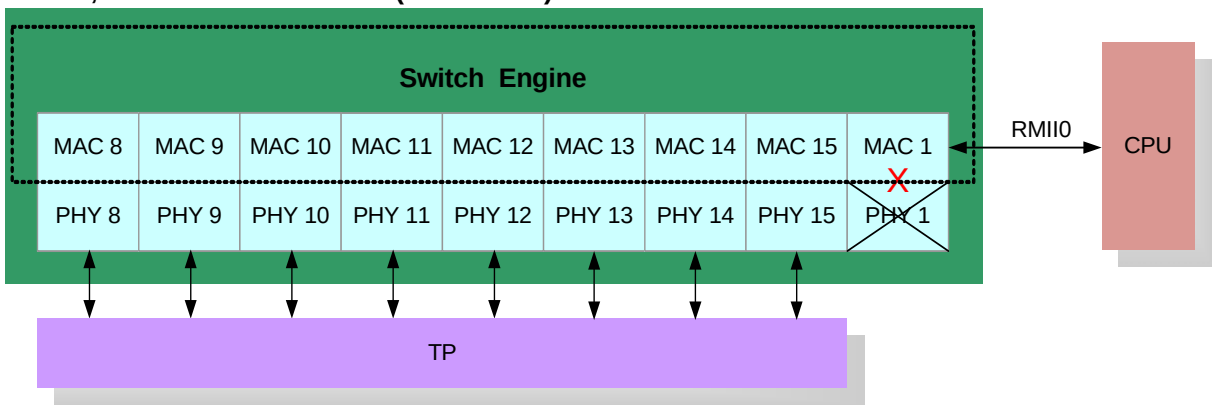
IP179N, 9 FE-TP Ports Switch



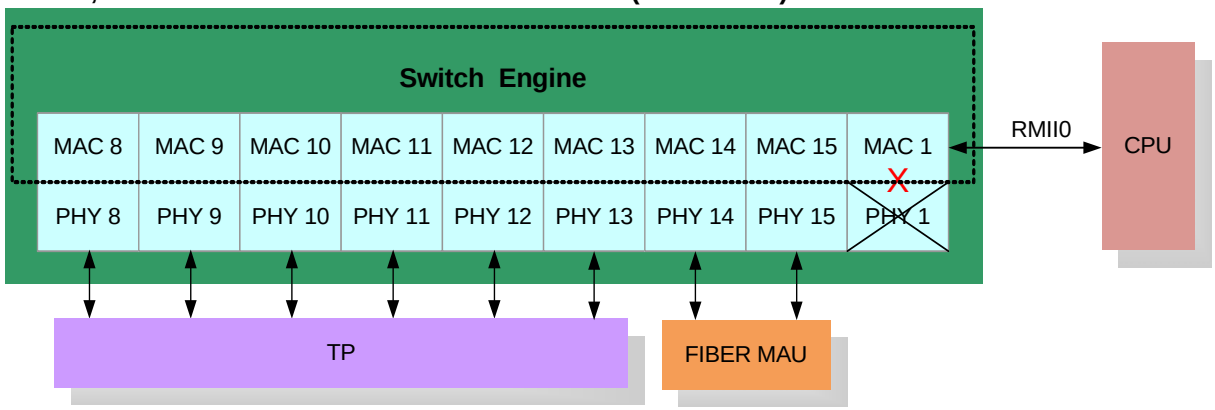
IP179N, 6 FE-TP Ports + 3 FE-Fiber Ports Switch



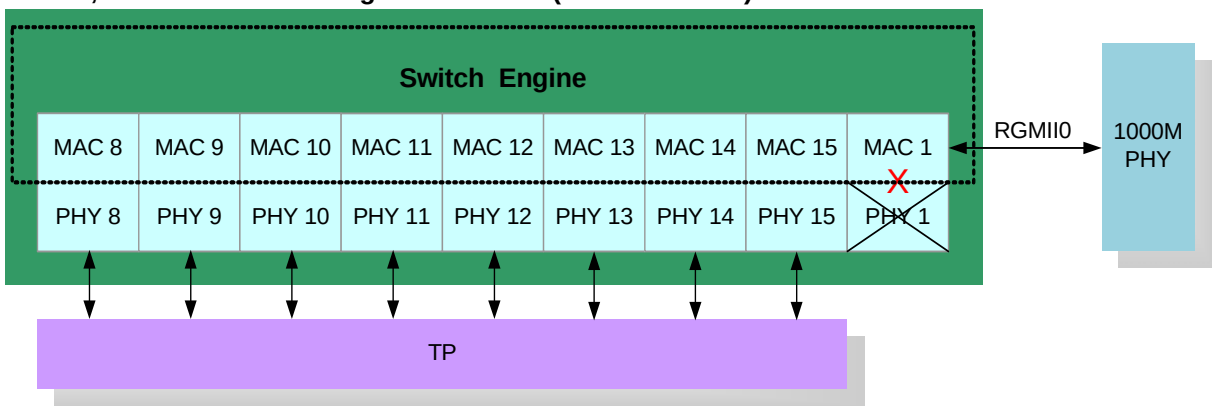
IP179N, 8 FE-TP Ports + 1 RMII (+MAC/CPU)



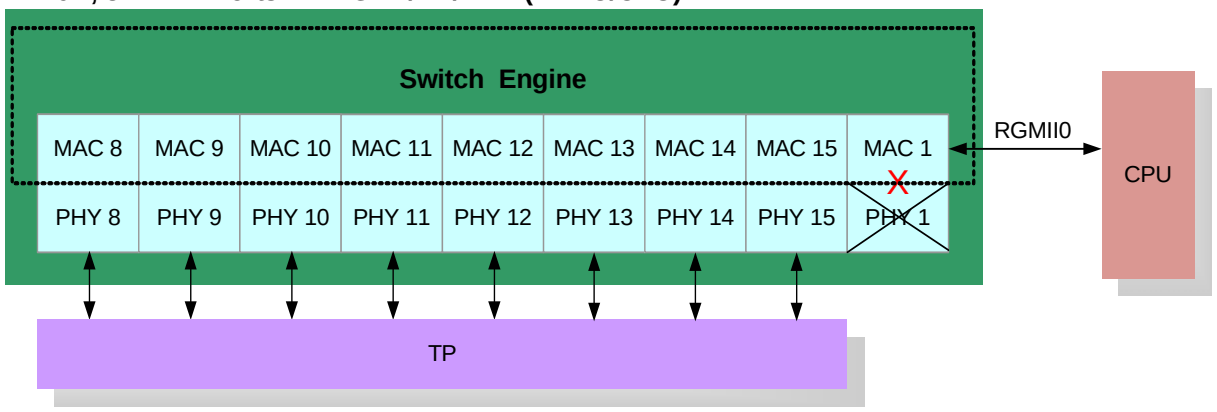
IP179N, 6 FE-TP Ports + 2 FE-Fiber Ports + 1 RMII (+MAC/CPU)



IP179H, 8 FE-TP Ports + 1 Giga Port Switch (+External PHY)



IP179H, 8 FE-TP Ports + 1 RGMII/MII/RMII (+MAC/CPU)



3 Pin Description

Type	Description	Type	Description
I	Input pin	IPL	Input pin with internal pull low 100K ohm
O	Output pin	IPH	Input pin with internal pull high 200K ohm
P	Power or Ground		

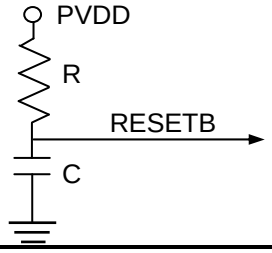
3.1 LDO Regulator

Pin No.		Label	Type	Description
IP179N	IP179H			
1	2	VREG_LDO	P	LDO regulator output It is an output power pin for 1.1V power source.
88	1	PVDD_LDO	P	LDO regulator input It is an input power pin for reference voltage.

3.2 MDI (Media Dependent Interface)

Pin No.		Label	Type	Description
IP179N	IP179H			
2, 3 10, 9 12, 13 20, 19 23, 24 31, 30 34, 35 42, 41 45, 46	3, 4 12, 11 15, 16 24, 23 31, 32 40, 39 44, 45 53, 52 56, 57	RXIP0, RXIM0 RXIP1, RXIM1 RXIP2, RXIM2 RXIP3, RXIM3 RXIP4, RXIM4 RXIP5, RXIM5 RXIP6, RXIM6 RXIP7, RXIM7 RXIP8, RXIM8	I/O	TP receive
5, 4 7, 8 15, 14 17, 18 26, 25 28, 29 37, 36 39, 40 48, 47	6, 5 9, 10 18, 17 21, 22 34, 33 37, 38 47, 46 50, 51 59, 58	TXOP0, TXOM0 TXOP1, TXOM1 TXOP2, TXOM2 TXOP3, TXOM3 TXOP4, TXOM4 TXOP5, TXOM5 TXOP6, TXOM6 TXOP7, TXOM7 TXOP8, TXOM8	I/O	TP transmit
33 43 44	43 54 55	FXSD6 FXSD7 FXSD8	I	Fiber signal detection of port 6,7,8 Port 6,7,8 can be configured to be either a TP port or a Fiber port with this pin. Connect this pin to GND for TP mode, and do not left this pin floating. Please refer to the paragraph “I/O Electrical Characteristics” for more detail information. In IP179N/H these pins should be connected to ground.
21	26	BGRES	O	Band gap resistor. It is connected GND through a precision resistor (R=6.19K, 1%) for band gap reference. Please refer to application circuit for more information.

3.3 System Clock & Reset Pins

Pin No.		Label	Type	Description
IP179N	IP179H			
86	126	OSCI	I	25MHz system clock input It is recommended to connect OSCI and X2 to a 25MHz crystal. If the clock source is from another chip or oscillator, the clock should be active at least for 10ms before RESETB de-asserted. X2 should be left open in this application.
87	127	X2	O	Crystal pin A 25Mhz crystal can be connected to OSCI and X2.
70	106	RESETB	IPH	Reset It is a low active input pad with Schmitt trigger. The reset time must be hold for more than 10 ms. If an R/C reset circuit is used; the capacitor should be connected to GND as shown in the figure. 

3.4 Test Mode

Pin No.		Label	Type	Description
IP179N	IP179H			
71	107	TEST	IPL	Test mode enable It should be connected to GND for normal operation
50	66	TEST0	IPH	Test0 Only for Test mode
51	67	TEST1	IPL	Test1 Only for Test mode
79	119	TEST2	IPH	Test2 Only for Test mode.
82	122	TEST3	IPH	Test3 Only for Test mode.

3.5 EEPROM Interface / Serial Management Interface (SMI)

Pin No.		Label	Type	Description
IP179N	IP179H			
EEPROM (only 24C02~16 supported)				
72	108	SCL/MDC	IPL/I	After reset release, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP179N/H stops reading EEPROM if it finds there is no 0xAA55 pattern in address 0. After reading EEPROM, this pin will switch to SMI mode MDC input. If EEPROM is unused, the duration from reset release to SCL switching to MDC is about 5ms.
73	109	SDA/MDIO	IPH, I/O	After reset release, it is used as data pin SDA of EEPROM. A bi-directional multi-drop bus for accessing the internal registers. It's recommended to add a 4.7K pull up resistor connecting to PVDD and a 30pf capacitor connecting to ground. After reading EEPROM, this pin will switch to SMI mode MDIO for read/write internal register. If EEPROM is unused, the duration from reset release to SDA switching to MDIO is about 5ms.
51	67	MDC1	IPL/O	Used for periodically polling the status of external PHY
50	66	MDIO1	IPH, I/O	Used for periodically polling the status of external PHY

3.6 Function Pins

Pin No.		Label	Type	Description
IP179N	IP179H			
85 84	125 124	EXTMII_MODE 0 EXTMII_MODE 1	IPH, I/O	External MII mode select EXTMII_MODE[1:0] 0x0：Disable (IP179N/H) 0x1：RMII (IP179N/H) 0x2：MII (IP179H) 0x3：RGMII (IP179H) RGMII 3.3/2.5/1.8V for IP179H RGMII 3.3/2.5V for IP179HI
83	123	EEE_DIS	IPH, I/O	IEEE 802.3az Energy Efficient Ethernet feature 1: Disable (Default) 0: Enable
81	121	IPC_MODE_DIS	IPH, I/O	IPCAM mode feature 1: Disable (Default) 0: Enable

Pin No.		Label	Type	Description
IP179N	IP179H			
80	120	MTOVLAN_DIS	IPH, I/O	Many-to-one VLAN setting Port0 to Port7 are isolated from each other and only communicate with Port8. 1: Disable (Default) 0: Enable
77	116	RX_DLY#	IPH, I/O	RX_CLK delay setting 1: RX_CLK delay 2ns (Default) 0: RX_CLK delay 0ns
76	115	TX_DLY#	IPH, I/O	TX_CLK delay setting 1: TX_CLK delay 2ns (Default) 0: TX_CLK delay 0ns
75	114	EEPROM_SEGMENT	IPH, I/O	EEPROM segment selection 1: Segment 1 (Default) 0: Segment 0
74	113	HWIGMP_DIS	IPH, I/O	Hardware IGMP feature 1: Disable (Default) 0: Enable

3.7 External MII0 Interface

Pin No.		Label	Type	Description
IP179N	IP179H			
External MII0 Interface (RGMII/MII/RMII)				
62	83	TX_CLK/ RMII_CLK_I	I/O	RGMII transmit clock / MII transmit clock / RMII reference clock input 1. RGMII mode (IP179H): clock input pin 1000Mbps : 125MHz 100Mbps : 25MHz 10Mbps : 2.5MHz 2. RMII mode (IP179N/H): clock input pin Clock : 50MHz 3. MII mode (IP179H, MAC mode)：clock input pin 100Mbps : 25MHz 10Mbps : 2.5MHz 4. MII mode (IP179H, PHY mode): clock output pin 100Mbps : 25MHz 10Mbps : 2.5MHz

67	88	TX_CTL	I	RGMII transmit control / MII transmit enable / RMII transmit enable RGMII: TX_CTL indicates a TX_EN at the rising edge of TX_CLK. TX_ER is derived from the logical operation of latched "TX_EN" and the value at the falling edge of TX_CLK.
-	87 86 85 84	TXD0 TXD1 TXD2 TXD3	I	RGMII transmit data / MII transmit data / RMII transmit data
66 65	-	TXD0 TXD1	I	RMII transmit data
60	80	RX_CLK/ RMII_CLK_O	I/O	RGMII receive clock / MII receive clock / RMII reference clock output 1. RGMII mode (IP179H): clock output pin 1000Mbps : 125MHz 100Mbps : 25MHz 10Mbps : 2.5MHz 2. RMII mode (IP179N/H): clock output pin Clock : 50MHz 3. MII mode (IP179H, MAC mode): clock input pin 100Mbps : 25MHz 10Mbps : 2.5MHz 4. MII mode (IP179H, PHY mode): clock output pin 100Mbps : 25MHz 10Mbps : 2.5MHz
54	74	RX_CTL	O	RGMII receive control / MII receive data valid / RMII receive data valid RGMII: RX_CTL indicates RX_DV at the rising edge of RX_CLK. RX_ER is derived from the logical operation of latched RX_DV and the value at the falling edge of RX_CLK.
-	79 78 77 75	RXD0 RXD1 RXD2 RXD3	O	RGMII receive data / MII receive data / RMII receive data RGMII: IP179H sends out RXD [3:0] and RX_CTL at both the rising edge and falling edge of RXCLK.
59 58	-	RXD0 RXD1	O	RMII receive data

3.8 LED

Pin No.		Label	Type	Description
IP179N	IP179H			

Pin No.		Label	Type	Description
IP179N	IP179H			
LED				
83 82 81 80 79 77 76 75 74	123 122 121 120 119 116 115 114 113	LINK_LED0 LINK_LED1 LINK_LED2 LINK_LED3 LINK_LED4 LINK_LED5 LINK_LED6 LINK_LED7 LINK_LED8	IPH/O	LINK LED It should be connected to PVDD through a LED and resistor.
Serial LED				
81	121	SDATA	IPH/O	LED serial data
80	120	SCLK	PH/O	LED serial clock It is a 312.5KHz clock.

3.9 Miscellaneous

Pin No.		Label	Type	Description
IP179N	IP179H			
84	124	INT_	O	Interrupt pin MII Register 20.2[9:8] can select interrupt event

3.10 Power & Ground

Pin No.		Label	Type	Description
IP179N	IP179H			
-	30	BGVCC	P	3.3V Band gap power
-	27	BGGND	P	Band gap ground
-	29	PLLVCC	P	3.3V PLL power
-	28	PLLGND	P	PLL ground
11, 32	14, 42, 63	AV10	P	1V analog power These pins must be connect to VREG_LDO via a resister or bead.
-	13,41,62 25	AVSS10, DAVSS10	P	1V analog ground
6, 16 22, 27 38, 49	8, 19 35, 48 60	AV33	P	3.3V analog power
-	7, 20 36, 49 61,128	AVSS33	P	3.3V analog ground
53, 68 78	70, 71 97, 98 117, 118	DVDD	P	1V digital core power These pins must be connect to VREG_LDO via a resister or bead.

Pin No.		Label	Type	Description
IP179N	IP179H			
-	69, 72 94, 95 110, 111	DVSS	P	1V digital ground
69	105, 100	PVDD	P	3.3V digital pad power
-	96, 112	PVSS	P	3.3V digital pad ground
56, 61	76, 81	PVDD_RG	P	MII0 I/O power. Please refer to 8.2 DC Characteristic.
-	73, 82	PVSS_RG	P	MII0 I/O ground
52	68	PVDD_RGSMI	P	SMI1 I/O power. Please refer to 8.2 DC Characteristic.
-	65	PVSS_RGSMI	P	SMI1 I/O ground
89	129	E-pad GND	P	Exposed pad for system ground, must be soldered to PCB ground plane.

4 Function Description

4.1 Switch Engine and Queue Management

4.1.1 Switch Engine

IP179N/H integrates an 8+1G switch controller, SSRAM, and 9 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE 802.3, IEEE 802.3u, and IEEE 802.3x specifications. IP179N/H offers all the rich features of a high-speed broadband wire Internet services including non-blocking switch fabric. Except the normal operation mode, IP179N/H offers an IPC mode to serve the extreme heavy upload stream application (ex. Extreme high definition IP CAM). This function could be enabled by the strapped pin (IP179N Pin 81 or IP179H Pin121) with a pull low resistor via a Hardware-PW-ON procedure.

4.1.2 Packet Forwarding

IP179N/H utilizes the “store & forward” method to handle packet transfer. IP179N/H begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

4.1.3 Flow control

IP179N/H jams or pauses a port, which causes output queue over the threshold. Its link partner will defer transmission after detecting the jam or pause frame. A port of IP179N/H defers transmission when it receives a jam or a pause frame. The source address (SA) of pause control frame will be [IP179N/H OUI (0090C3), port number]. For example, the SA of port 1 pause control frame will be “ 00 90 C3 00 00 01”.

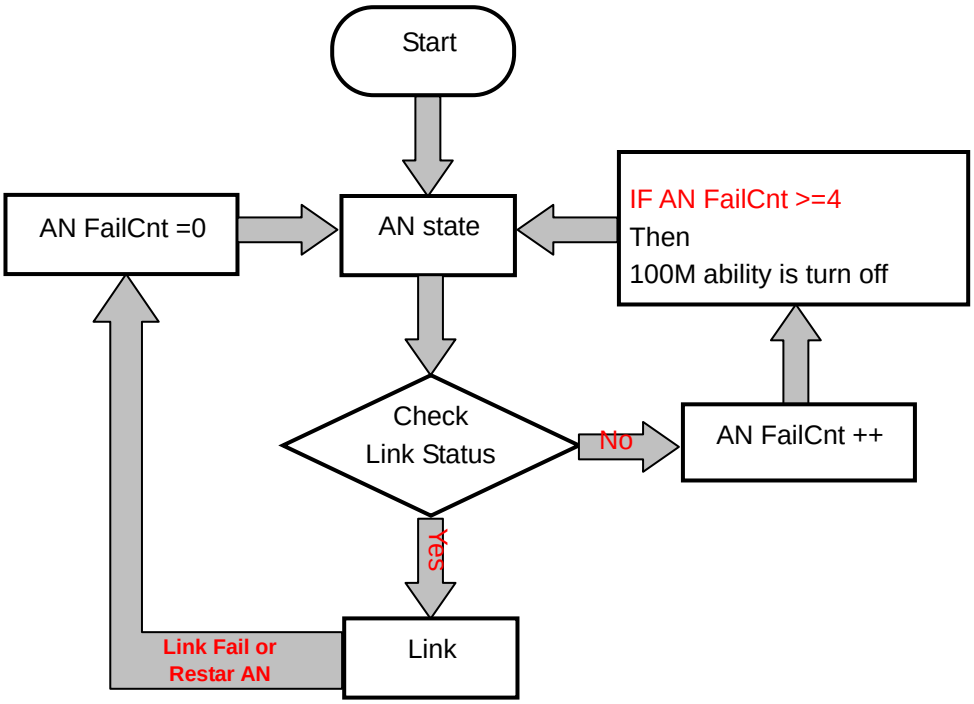
The flow control function can be enabled by programming registers 4[11:10]

4.1.4 Backpressure

In half duplex mode, the IP179N/H supports backpressure flow control. When set BK_EN of MII register 20.1[4] to “1”, the packets in buffer reach the threshold, IP179N/H generates a jam pattern to back off the link partner.

4.2 LBAS (Length/Link Based Auto Switch)

IP179N/H supports LBAS function, it can auto switch to 10BASE-T to establish link in extra-long cable.
IP179N/H performs LBAS function through auto-negotiation process.
As the flow chart, when IP179N/H starts to link, it advertises 100BASE-TX/10BASE-T ability in default.
Once auto-negotiation process is completed and 100BASE-TX is selected.
Then IP179N/H checks 100Mbps receiving quality (performance). If the receiving quality is good, the 100Mbps link will be established.
If not good IP179N/H will restart auto-negotiation to do another try and AN_fail_cnt count 1.
While AN_fail_cnt reaches the specified value, IP179N/H will restart auto-negotiation and advertises 10BASE-T ability only to establish 10Mbps link to link partner.
Also when break link, IP179N/H will keep mask 100BASE-TX ability for 5~10 seconds to speed up next LBAS link process.
It can shrink link time (down speed to 10M) from 8 second to 1 second.
Any restart-AN event will clear AN_fail_cnt then IP179N/H will stop mask 100BASE-TX ability in auto-negotiation process.



4.3 External MII

IP179N is designed for single RMII interface (MII0), while IP179H provides 1 RGMII/MII/RMII interface (MII0). Both IP179N and IP179H are compatible with IEEE 802.3, and connection to either an external MAC or PHY.

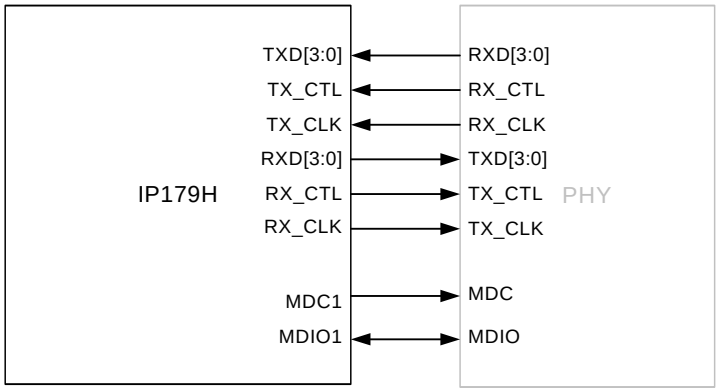
IP179H MII0 provides a faster RGMII interface, and also allowing configuration into MII/RMII. These interfaces provide flexible applications, such as 8 FE-TP Ports + 1 Giga Port Ethernet switch (w/ or w/o POE chips) and NVR application.

By adjusting PVDD_RG power supply, IP179H RGMII supports a wider range of voltage power (3.3/2.5/1.8V). IP179HI only supports 3.3/2.5V RGMII voltage.

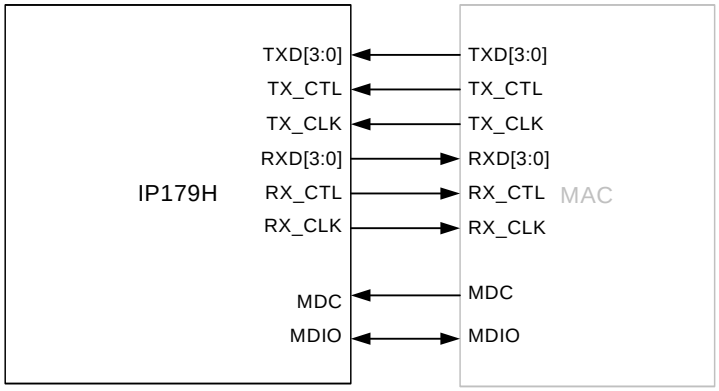
4.3.1 The Application Circuit of RGMII

(EXTMII_MODE1=1, EXTMII_MODE0=1)

External PHY
The following circuit diagram is the RGMII circuit of IP179H MII0.



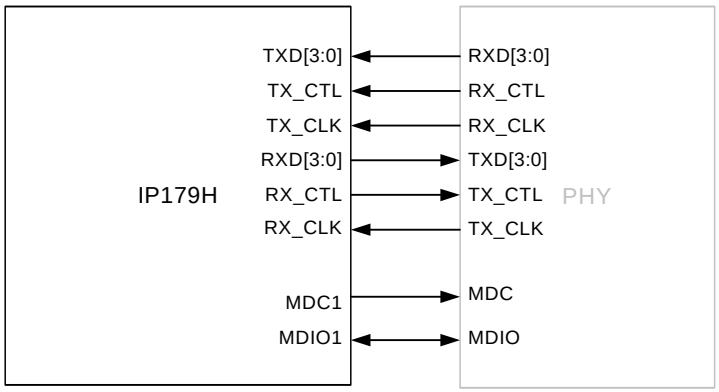
External MAC
The following circuit diagram is the RGMII circuit of IP179H MII0.



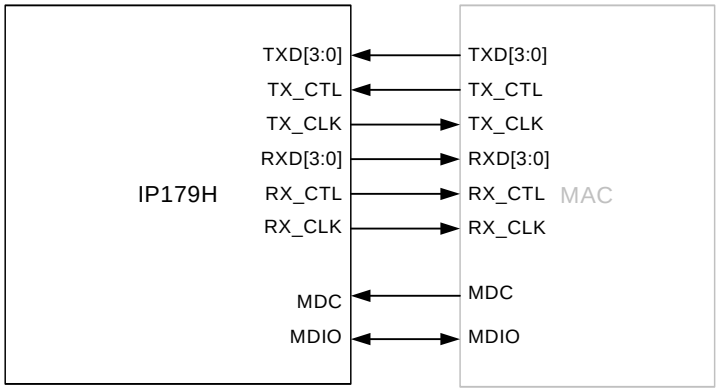
4.3.2 The Application Circuit of MII

(EXTMII_MODE1=1, EXTMII_MODE0=0)

External PHY (MII0_MAC_MODE=1)
The following circuit diagram is the MII circuit of IP179H MII0 MAC mode.



External MAC (MII0_MAC_MODE=0)
The following circuit is the MII circuit of IP179H MII0 PHY mode.

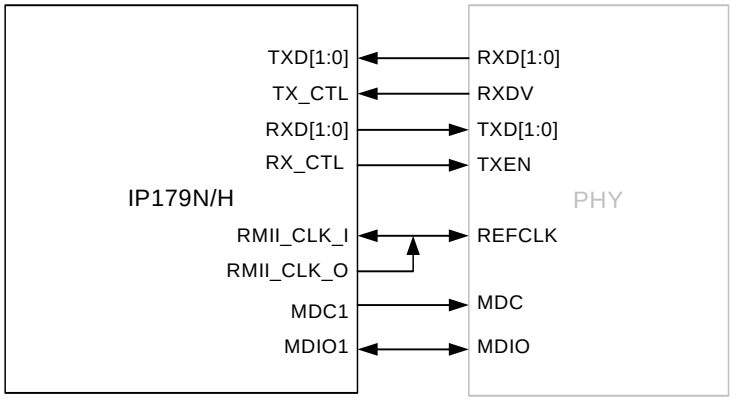


4.3.3 The Application Circuit of RMII

(EXTMII_MODE1=0, EXTMII_MODE0=1)

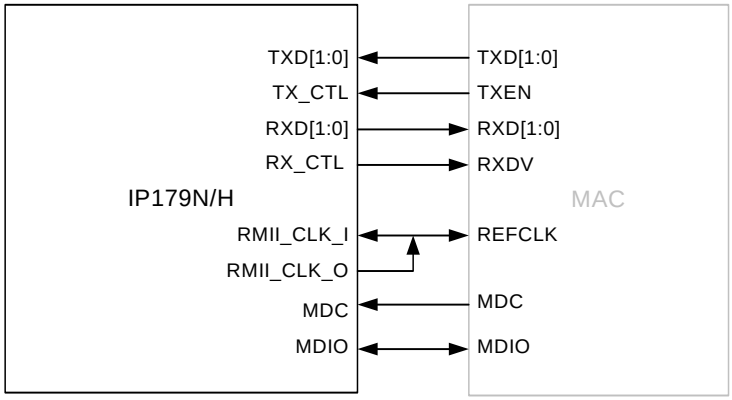
External PHY

The following circuit diagram is the RMII circuit of IP179N/H MII0.



External MAC

The following circuit is the RMII circuit of IP179N/H MII0.



4.4 Virtual LAN (VLAN)

IP179N/H is a VLAN aware-switch and support two classification rule: port-based VLAN and tag-based VLAN. Each port can configure its classification rule respectively. In tag-based VLAN the switch supports up to 16 VLAN groups. Two ingress VLAN rule and egress VLAN rule are provided. The ingress VLAN rule is used to discard packet that violate this rule. The egress rule checks VLAN member set and performs the determination of tagging or un-tagging. In learning process the switch supports shared and independent VLAN learning.

4.4.1 Port-based VLAN

Port based VLAN divides switching ports into different VLAN base on per port basis. IP179N/H provides 9 port-based VLAN configurations for each ingress port. The port-based VLAN feature filter out traffic that is not in VLAN domain port. The port-based VLAN domain selected for each ingress via REG22.16-24、23.0-8 and 23.16-24. Packet inserts or removes tag depending on the port defined as tagged or untagged port.

4.4.2 Tag-based VLAN

In tag-based VLAN classification two modes are provided for applying VLAN classification: using VID to classify VLAN and using PVID to classify VLAN. Using VID to classify VLAN, VID searching is performed according to frame's VID. If any packets carrier no VID information, the VID searching is performed using PVID. In using PVID to classify VLAN the PVID for a given port is used for VID searching, whether VLAN tagged or untagged frames are received on this port.

The VLAN table consists of 16 entries, with the contents described in the following table.

VLAN Entry Field	MII Register	Descriptions
Valid	22.15[15:0]	Entry is valid
VID and FID	24.0-15	VLAN identifier and Filtering Identifier
Add Tag	24.16-31	To add VLAN tag to frame
Remove Tag	25.0-15	To remove VLAN tag from frame
VLAN Member set	25.16-31	Membership for each VLAN

4.4.3 VLAN Ingress Filtering

IP179N/H specify a VLAN ingress rule in MII register 22.2. Any frames received on a port are discarded if it violates this rule.

4.4.4 Shared and Independent VLAN Learning

The learning process extracts SA+FID information encapsulated in reception of incoming packet and store to MAC table for future purpose of forwarding frames. An entry is created or updated in MAC table if all conditions are met:

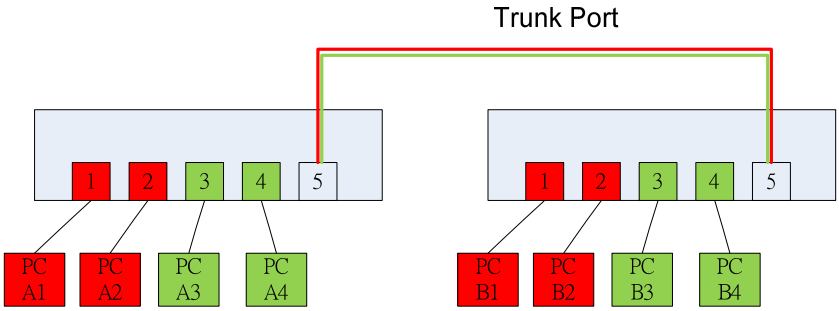
1. The port on which frame is received is on learning enable (REG20.5[8:0])
2. The SA of received frame is unicast address
3. The frame has been received without error
4. The Member set for the frame's VID includes at least one Port

The learning process supports shared and independent VLAN learning according to REG20.7[0] setting . In shared VLAN learning rule the learning information from a VLAN can make used by the others VLANs. In independent VLAN learning rule the learning information from a VLAN makes use only itself. This standard was specified in IEEE 802.1Q.

4.4.5 The determination of the requirement to insert or remove tag

IP179N/H supports the ability of insertion and removal tag header from a VLAN. Tagged means that the vlan information is added to the frame before it is sent to trunk port. Untagged means that the vlan information is remove from the frame before it is sent.

For example, a switch is divided into two logical switches (RAD VLAN and GREEN VLAN). A single switch port can be used as trunk port for connection between more than one Ethernet switch. Trunk links provide VLAN information for frames traveling between switches. If switch support tagged VLAN, you can extend VLANs across more the one switches.



4.5 Quality of Service (QoS)

IP179N/H provides two queues per-port to be assigned according to information in
1. Ingress Port
2. VLAN Priority
3. ToS/DSCP

The priority classification determines which one is assigned to queue-mapping for a given frame. Priority classification table summarizes how the registers (MII register 20.8-15) setting to affect the result of queue-mapping.

PORT_PRI_EN	COS_EN	TOS_OVER_VLAN	Queue mapping
1	Don't care	Don't care	Port based mapping
0	1	0	802.1p mapping for tagged frame; otherwise, DSCP mapping for IP frame; otherwise, port-based mapping
0	1	1	DSCP mapping for IP frame; otherwise, 802.1p mapping for tagged frame; otherwise, port-based mapping

Each output port has two queues and two queue scheduling are used：WRR (Weighed Round Robin) and SP (Strict Priority)

SP:
In strictly priority, the packets in a queue will go first till its queue is empty.
WRR:
User can control the number of packet transmission on an output queue by setting its weight.

4.6 IGMP Snooping

IGMP is used between hosts and neighboring multicast routers, IP179N/H listens the IGMP message communication between router and host to establish multicast group membership. Based on the group membership information, IP179N/H forwards IP multicast data to its membership which registered in group table. For hardware IGMP snooping timeout mechanism is provided by applying the hosts silently leave a specific multicast group. “Silently Leave” means that a host does not respond to query message when it want to leaves group.

4.7 Spanning Tree

In IP179N/H spanning tree operation separate into software implement and hardware implement. In software implement CPU must process BPDU packet and configure the sate of each port. In hardware implement the switch trap BPDU to CPU. The following table describes how to configure the state of each port in IP179N/H.

State	Fwd BPDU packet to CPU	Fwd BPDU packet from CPU	Address learning	Fwd all packet normally	(Forward enable, Learning enable)[1]
Disable	X (note 2)	X (note 2)	X	X	(0,0)
Blocking	O	X (note 3)	X	X	(0,0)
Listening	O	O	X	X	(0,0)
Learning	O	O	O	X	(0,1)
Forwarding	O	O	O	O	(1,1)

Note1: O: enabled, X: disabled
Note2: CPU should not send packets to IP179N/H and should discard packets from IP179N/H.
Note3: CPU should not send packets to IP179N/H.

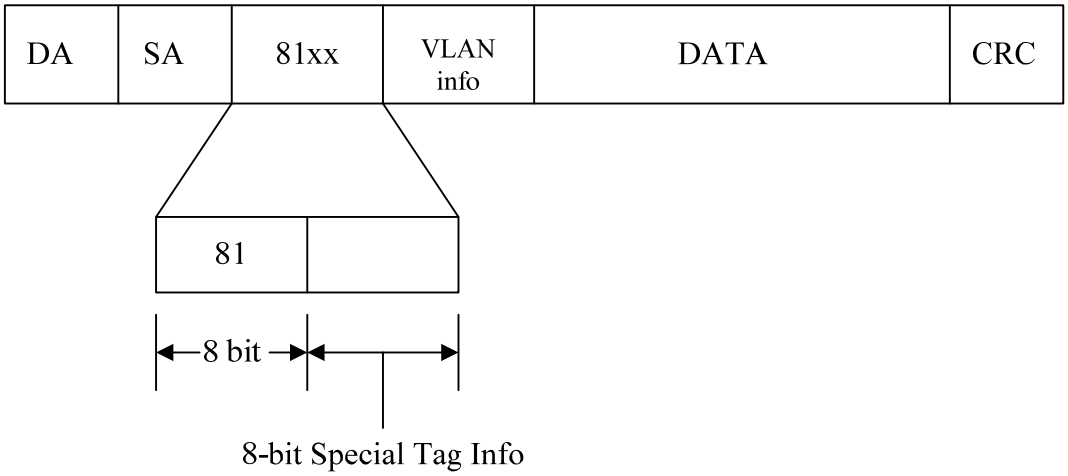
IP179N/H support fast aging function for RSTP, User can configure the parameter from MII register 21.4[9:8] and 21.4[4:0].

4.8 Special Tag

The purpose of special tag is:

- To allow a frame (IP179N/H to CPU) to carrier ingress port number.
- To allow a frame (CPU to switch) to indicate the output port mask in special tag header.

The VLAN TPID is represented in two octets, the hexadecimal value 8100. The octets display from left to right, the left octet is 0x81 and the right octet is 0x00. Special tag information appears in the right octet whose value is not a zero.



Special tag format

[1] The forwarding and learning ability of each port are configured in MII register 20.4 and 20.5.

There are two formats of special tag, depending on the frame direction. The special tag format is defined as following.

1. Special Tag for RX (From switch to CPU)
Frame direction is from switch to CPU. The special tag information consists of ingress port number.

Special Tagged Information	Description
Bit 3-0	Ingress Port number - 4'b0000: Disabled - 4'b0001: Port 0 - 4'b0010: Port 1 - 4'b0011: Port 2 - 4'b0100: Port 3 - 4'b0101: Port 4 - 4'b0110: Port 5 - 4'b0111: Port 6 - 4'b1000: Port 7 - Other: Reserved

2. Special Tag for TX (From CPU to switch)
Frame direction is from CPU to switch. This function provides for forwarding decision. These parameter embedded in special tag header can be set by CPU.
If the CPU transmits packet without Special Tag, the packet will be forwarded according to the MAC address table.

Special Tagged Information	Description
Bit 7-0	Output Port Mask - bit 7: port 7 - bit 6: port 6 - bit 5: port 5 - bit 4: port 4 - bit 3: port 3 - bit 2: port 2 - bit 1: port 1 - bit 0: port 0

4.9 MAC Address Table

IP179N/H support 2K MAC addresses. The address table can configure either 2K unicast address or 1K unicast address/1K multicast address. The multicast table occupies the MAC table from 0x400 to 0x7FF if the AT_STR bit (register 20.7.2) set to high. The MAC table is organized as hash table which consist of 512 buckets with four entries in each bucket. Each bucket is located through its respective hash key, calculated from MAC and FID by using XOR algorithm. It is possible that multiple MAC addresses index to the same bucket, term as collision. IP179N/H provides four entries within each buck for reducing collision rate. Finally, the 11-bit hash index mapping to MAC table consist of three parameters: multicast address bit, hash key and entry number. The MSB of hash index distinguishes multicast address from MAC addresses. The least two significant bit in hash index indicates entry number. The other bit is hash key which calculated from MAC and FID using XOR algorithm. In IP179N/H the formula of hash index is computed based on table structure. The user can set AT_STR bit to configure table structure. The 11-bit hash index is computed as following:

AT_STR=0 (2K unicast table)

Hash Index = { XOR({2'b00,FID,MAC[47:45]}, MAC[44:36], MAC[35:27], MAC[26:18], MAC[17:9], MAC[8:0]), Entry Number }

AT_STR=1 (1K unicast table and 1K multicast table)

Hash Index = {Multicast Address Bit, XOR({4'h0,FID}, MAC[47:40], MAC[39:32], MAC[31:24], MAC[23:16], MAC[15:8], MAC[7:0]), Entry Number }

4.9.1 Entry Content

Entry content in MAC table contains the forwarding information for a specific MAC address. This table content is automatically updated by learning process and can directly access from the CPU through Address Table Access register (see MII register 21.8-13).

4.9.2 Accessing MAC Table

The MAC table can be accessed by through MII register 21.8-13. IP179N/H provides two access commands: single read and single write. A single read or write transfer only executes a single I/O operation and user only can access a particular memory address. When a given MAC+FID read from (or write to) MAC table, the MAC+FID is used to compute hash index for mapping to MAC table.

Single Read
The single read process is described as following steps:

Step 1 – Set hash index in register 21.8[10:0]
Step 2 – Set single read command in register 21.8[14]
Step 3 – Set START bit in register 21.8[15] to initiate read command
Step 5 – read data from data buffer register (register 21.9-13). User must read data buffer register from register 21.9 to register 21.13 in regular order.

Single Write
The single write process is described as following steps:

Step 1 – Write desired data to data buffer register (register 21.9-13)
Step 2 – Set hash index in register 21.8[10:0]
Step 3 – Set single write command in register 21.8[14]
Step 4 – Set START bit in register 21.14[15] to initiate write command

4.9.3 Address Aging

The MAC address is removed from MAC table by aging process. The aging process periodically check aging time field of MAC table and the aging time is programmed in 21.4. The aging function can be enabled based on per port or a FID.

The aging function can quickly aged out MAC address from a unlink port and the enable bit is in register 20.7[3].

4.10 MAC/IP Table

IP179N/H MAC/IP table is used to record the latest source MAC and IP address. The MAC/IP table is accessed by CPU through MII registers.

Source port	Source MAC Address (SMAC)	Source IP Address (SIP)
0	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
1	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
2	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
3	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
4	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
5	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
6	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
7	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx
8	48'hxx_xx_xx_xx_xx_xx	32'hxx_xx_xx_xx

4.10.1 MAC/IP Table register

MII Register	Name	Description
21.8[13]	DISPLAY_SRC_ADR	Display the source MAC and IP address associated with the source port.
21.8[12]	SIP_ADR_VALID	Source IP address field of entry content is valid. 1: Valid 0: Invalid
21.8[11]	SMAC_ADR_VALID	Source MAC address field of entry content is valid. 1: Valid 0: Invalid
21.8[3:0]	SRC_PORT	Source port 0x0: Port0 0x1: Port1 0x2: Port2 0x3: Port3 0x4: Port4 0x5: Port5 0x6: Port6 0x7: Port7 0x8: Port8

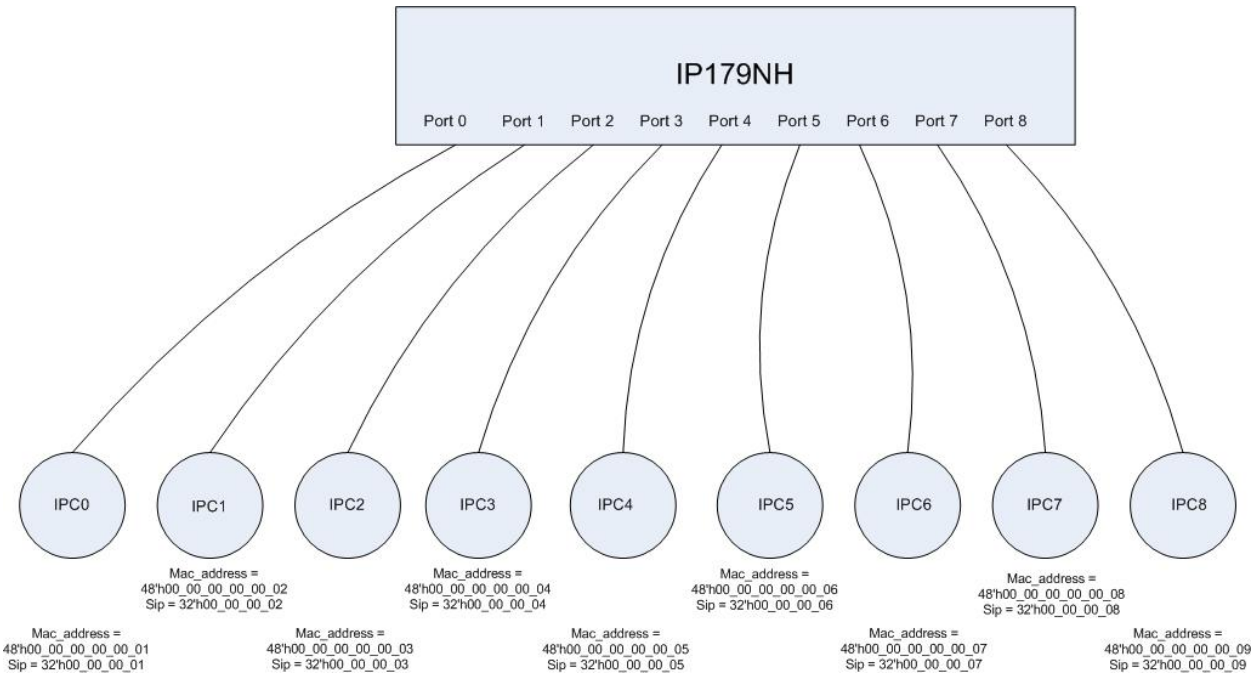
Command register for source MAC/IP address associated with the source port

MII Register	Name	Description
21.9[15:0]	SRC_MAC_ADDR[15:0]	Source MAC address[15:0]
21.10[15:0]	SRC_MAC_ADDR[31:16]	Source MAC address[31:16]
21.11[15:0]	SRC_MAC_ADDR[47:32]	Source MAC address[47:32]
21.12[15:0]	SIP[15:0]	Source IP address[15:0]
21.13[15:0]	SIP[31:16]	Source IP address[31:16]

Entry content for the source MAC/IP address associated with source port

4.10.2 Display the MAC/IP table of source port

Example: Read the source MAC/IP address associated with the source port (Read port 0~8 SMAC and SIP address).



Source port	Source MAC Address (SMAC)	Source IP Address (SIP)
0	48'h00_00_00_00_00_01	32'h00_00_00_01
1	48'h00_00_00_00_00_02	32'h00_00_00_02
2	48'h00_00_00_00_00_03	32'h00_00_00_03
3	48'h00_00_00_00_00_04	32'h00_00_00_04
4	48'h00_00_00_00_00_05	32'h00_00_00_05
5	48'h00_00_00_00_00_06	32'h00_00_00_06
6	48'h00_00_00_00_00_07	32'h00_00_00_07
7	48'h00_00_00_00_00_08	32'h00_00_00_08
8	48'h00_00_00_00_00_09	32'h00_00_00_09

MAC/IP Table

Read port 0:
Step 1 – Write reg 21.8[15:0] = 16'h2000 (read port 0 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 1:
Step 1 – Write reg 21.8[15:0] = 16'h2001 (read port 1 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 2:
Step 1 – Write reg 21.8[15:0] = 16'h2002 (read port 2 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 3:
Step 1 – Write reg 21.8[15:0] = 16'h2003 (read port 3 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 4:
Step 1 – Write reg 21.8[15:0] = 16'h2004 (read port 4 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 5:
Step 1 – Write reg 21.8[15:0] = 16'h2005 (read port 5 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 6:
Step 1 – Write reg 21.8[15:0] = 16'h2006 (read port 6 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 7:
Step 1 – Write reg 21.8[15:0] = 16'h2007 (read port 7 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

Read port 8:
Step 1 – Write reg 21.8[15:0] = 16'h2008 (read port 8 SMAC and SIP address)
Step 2 – Read reg 21.8[15:0], If reg 21.8[12:11] =2'b11 (SIP and SMAC data is ready to read)
Step 3 – Read reg 21.9[15:0] (MAC[15:0] hashing table data)
Step 4 – Read reg 21.10[15:0] (MAC[31:16] hashing table data)
Step 5 – Read reg 21.11[15:0] (MAC[47:32] hashing table data)
Step 6 – Read reg 21.12[15:0] (SIP[15:0] hashing table data)
Step 7 – Read reg 21.13[15:0] (SIP[31:16] hashing table data)

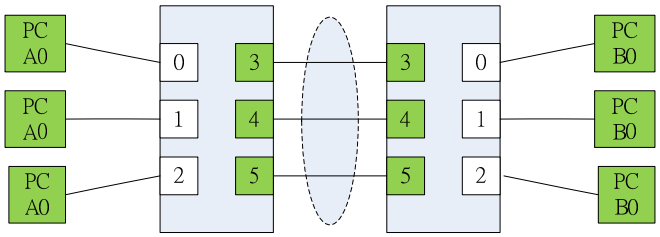
4.11 Link Aggregation

Link aggregation is a method of logically combing multiple ports together to increase a single high-throughput path and implement load balanced among the member ports of the group. If some of ports are in a trunk group, all ports in that trunk group shall be in the same VLAN group. It also provides failover capabilities to maintain networks connectivity if a port becomes unavailable.

The following example is shown how to configure three links between two switches.

1. Set AGGR_MODE (REG21.14[14:13]), four ways determine how to search aggregation table
   i. 21.14[14:13]=0x0, using source port as index to select one of aggregation table
2. Set AGGR_GROUP_0(REG21.14[8:0]), to add ports into a aggregation group.
   i. 21.14[8:0]=0x38, port3-4 are aggregated a group
3. Set aggregation table, it guarantee any frames only transmitted to one port within an aggregation group.

21.16[8:0]	9'b1_1100_1111	Port 0 select port 3 as destination port within group
21.17[8:0]	9'b1_1101_0111	Port 1 select port 4 as destination port within group
21.18[8:0]	9'b1_1110_0111	Port 2 select port 5 as destination port within group

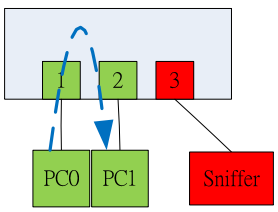


4.12 Port Mirror

Port mirror allows the ingress or/and egress packets to be captured to the port that connect to analyzer device. The feature can monitor the traffic activity on the given port and check intruders.

An example, traffic sent by pc0 to pc1 is copied to port 2 (sniffer).

21.24[15]	0x1	Port mirror is enabled
21.24[14]	0x1	Sniffer port receive only mirrored packets and discard others packets
21.24[13:12]	0x2	Traffic from ingress port to egress port is mirrored.
21.24[8:0]	0x4	Port 2 connect to sniffer
21.25[8:0]	0x1	To specified which ingress port to be mirrored.
21.26[8:0]	0x2	To specified which egress port to be mirrored.



4.13 Broadcast Storm Protection

Broadcast storm is the broadcast or multicast traffic flooding the network to degrade network performance by excessive packets. Broadcast storm protection filter that measure the broadcast traffic over threshold at predefine time interval. If the threshold is reached, further broadcast traffics are suppressed.

4.14 Reserved MAC Address

The action of multicast MAC addresses summarize in register 21.27. Packet with reserved multicast address are reserved for special function, switch can handle uniquely.

4.15 Statistic Counters

IP179N/H implement 3 counters on per-port and one global FCS error packet counter.

32-bit Counter	Description
FCS error packet counter	The number of packets received by a port that do not pass FCS check.
Received packet counter	Total good packets received on a port
Transmitted packet counter	Total packets transmitted on a port
Global FCS error packet counter	Total error packets received on all ports

4.16 Green Power

IP179N/H provides various power management modes to save the power consumption. In addition to the power down mode defined on IEEE802.3, two extra power saving modes are used to further reduce the system power consumption.

4.16.1 Auto Power Saving Mode

IP179N/H will automatically enter this mode if no cable link is established. After entering this mode, IP179N/H will shutdown unnecessary function and issue the link pulse at a rate lower than the regular rate specified on IEEE 802.3.

4.16.2 IEEE802.3az EEE (Energy Efficient Ethernet)

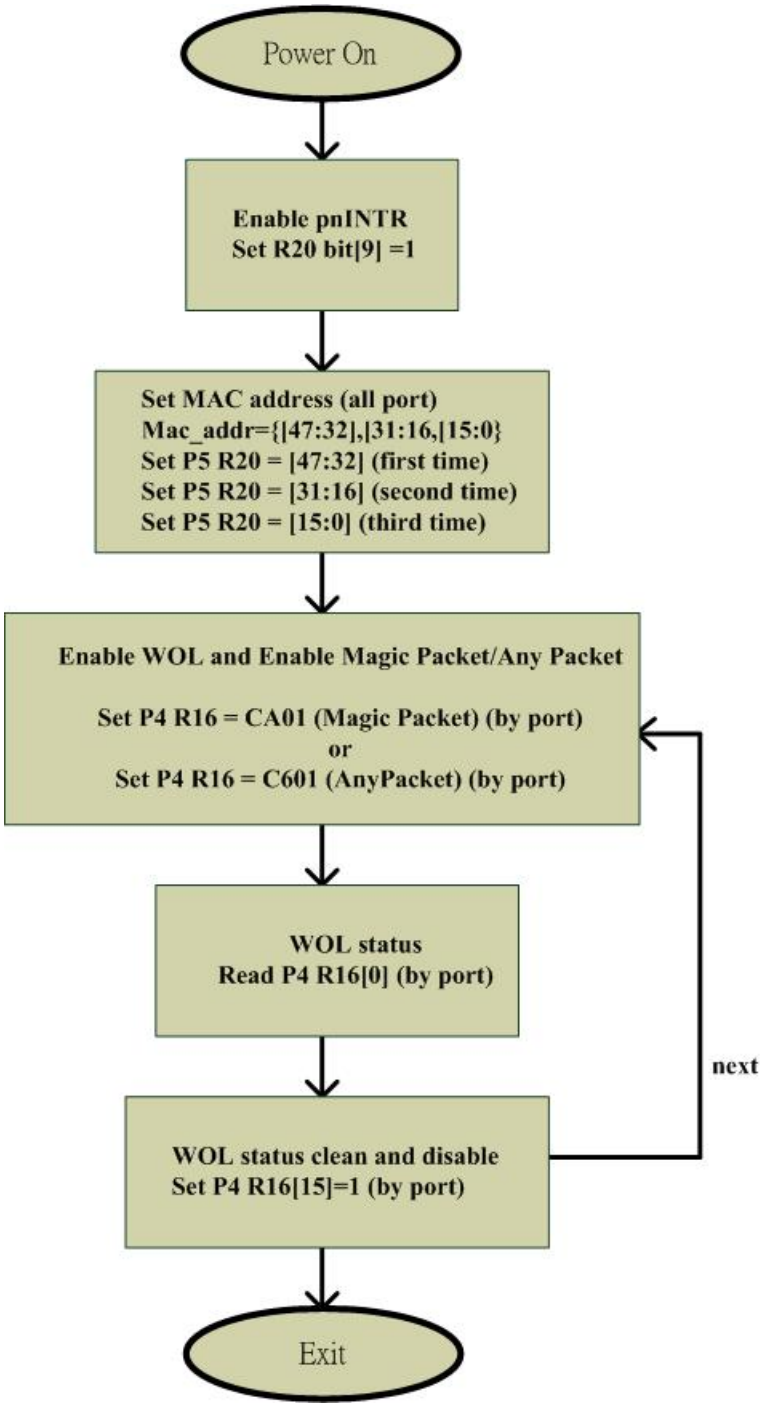
In order to enter this mode, the PHY part should declare the EEE capability during the auto-negotiation phase.
It's the higher layer's responsibility to memorize the link partner's wakeup time and wakeup the link partner before sending data. The higher layer means a mechanism that can evaluate the packet buffer utilization and wake the link partner before sending the data. In general speaking, this mechanism probably consists of at least one of the following items: the packet buffer manager, the application program and OS.

The EEE module works well at LPI (Low Power Idle) mode under the following conditions:

1. Link at full-duplex.
2. Auto-negotiation is enabled in both local and remote PHYs.
3. 100Mbps full duplex.
4. EEE ability is supported in both local & remote PHYs.
5. EEE_EN (Register 22.25[8:0]) is enabled for EEE function via default value.
6. SLEEP_TIME (Register 22.26[11:0]) is the default value for EEE sleep time.
7. WAKE_TIME (Register 22.27-31) is the default value for EEE wake time.

4.16.3 Wake on LAN (WOL)

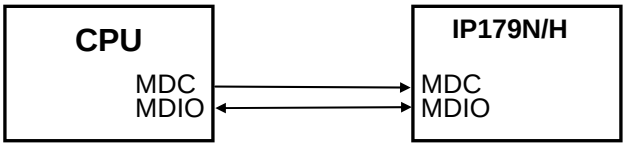
IP179N/H supports three WOL events: link change, magic packet and any packet. If the WOL event happened, the interrupt pin (IP179N Pin 84 or IP179H Pin124) would be activated. The diagram below is the WOL flow chart.



4.17 Serial Management Interface

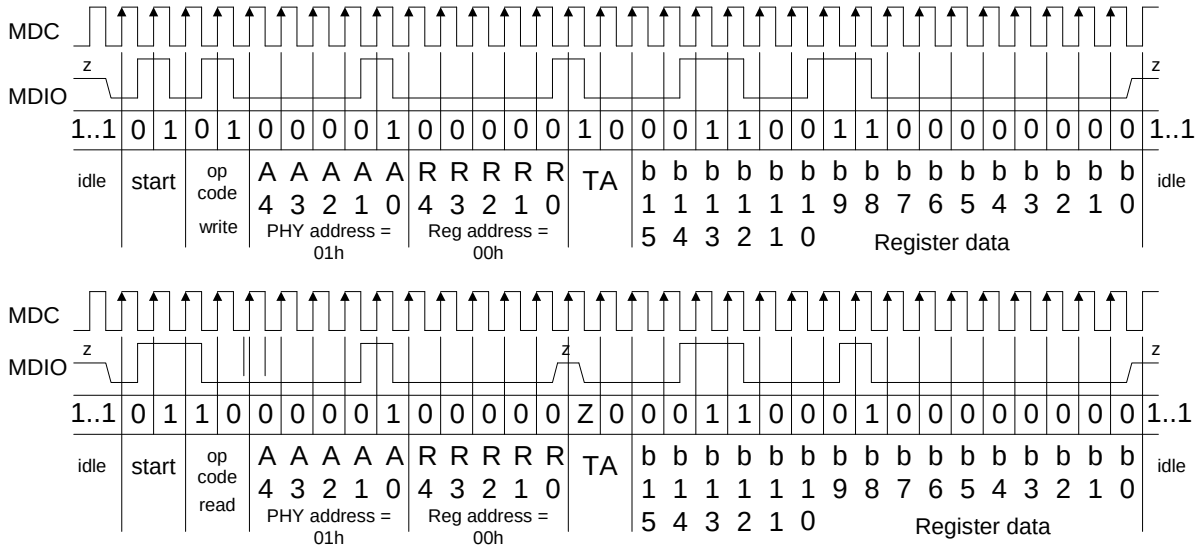
User can access IP179N/H's MII registers through serial management interface with pin MDC and MDIO. Its format is shown in the following table. To access MII register in IP179N/H, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

System diagram



Frame format	**<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>**
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10> <b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>

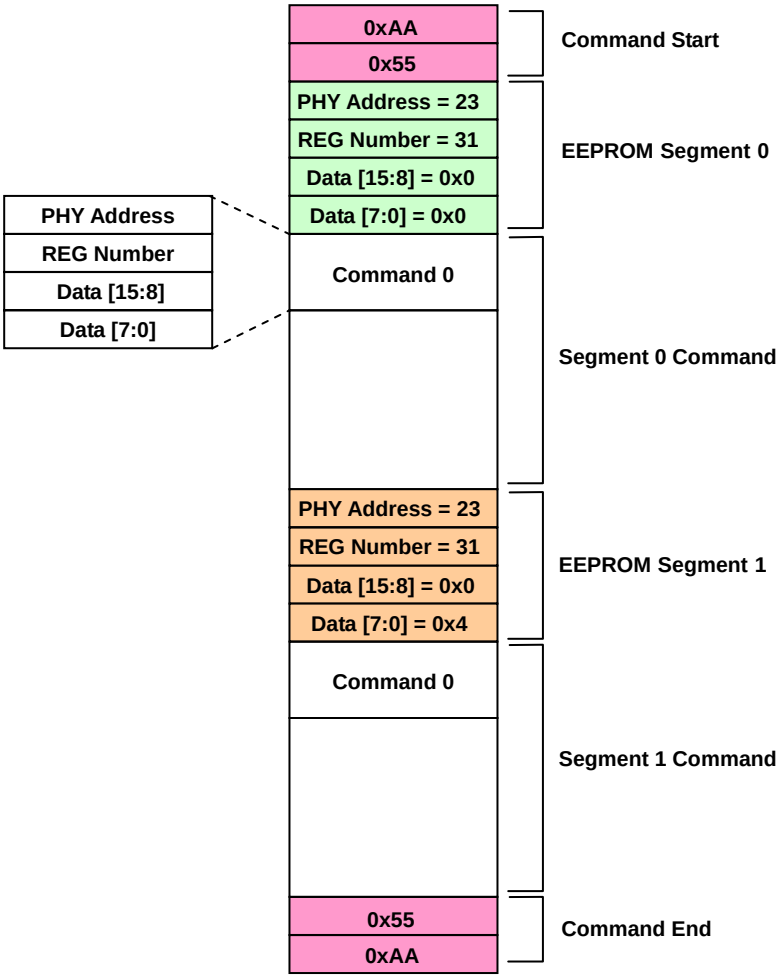
Figure 1 Serial management interface Read / Write Diagram



4.18 EEPROM Interface

IP179N/H supports EEPROM interface to program configuration registers during power-on reset. When power on and EEPROM is present, if the fist 16-bit data match command-start 0xAA55 and then the data read from EEPROM until that command-end pattern 0x55AA is read-in. In the case where the first data does not math 0xAA55, the load EEPROM process stops and IP179N/H treats it as no EEPROM exist.

The EEPROM can be partitioned into two segments and select which segment command you want to load the switch by setting EEPROM_SEGMENT pin and register 23.31[2]. The register 23.31[2] read-in and it matches EEPROM_SEGMENT pin, then the future command fetch into switch registers. If it does not match EEPROM_SEGMENT pin, the fetch command process ignore command fetch into switch registers until a match is found.



4.19 LED display (normal operation)

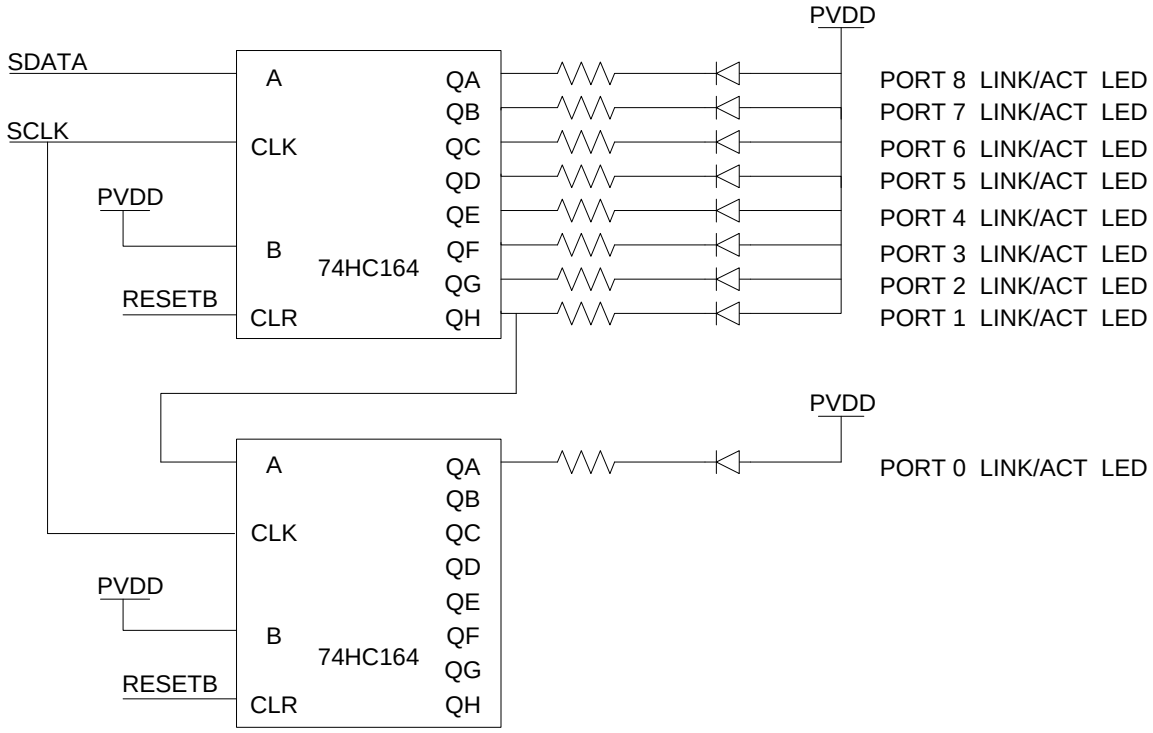
	LED mode 0	LED mode 1	LED mode 2	LED mode 3
LED_SEL[1:0]	00	01	10	11
LINK_LED[8:0]	100M Link + Activity (1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity)	Link (1: link fail, 0: link ok)	100M Link + Activity (same as mode 0)	Link + Activity (1: link fail, 0: link ok, flash: Link ok and TX/ RX activity)
SPEED_LED[8:0]	flash: Link ok and TX/ RX activity	flash: Link ok and TX/ RX activity	Full/half (1: half, 0: full, flash: collision)	Speed (1: speed=10M, 0: speed=100M
FULL_LED[8:0]	0: 10M Link ok 1: 100M Link ok	Full/half (same as mode 3)	10M Link + Activity (1: 10M Link fail, 0: 10M Link ok and no activity, flash: 10M Link ok and TX/RX activity)	Full/half (1: half, 0: full, flash: collision)

4.20 Serial LED Mode

IP179N/H supports serial LED mode and can be setting MII register SERIAL_LED_EN to 1 by MII page3 register 16[12].
There are no enough pins for LED and IP179N/H sends out LED information through SCLK (IP179N pin 80 or IP179H pin 120) and SDATA (IP179N pin 81 or IP179H pin 121). It is necessary to use TTL chip to decode and drive LED. The application circuit is shown below.
IP179N/H supports two types of serial LED mode and can be setting by MII page3 register 16[11]. The default value is 0 (SERIAL_LED_MODE = 0) and can be setting to 1 by MII page3 register 16[11].

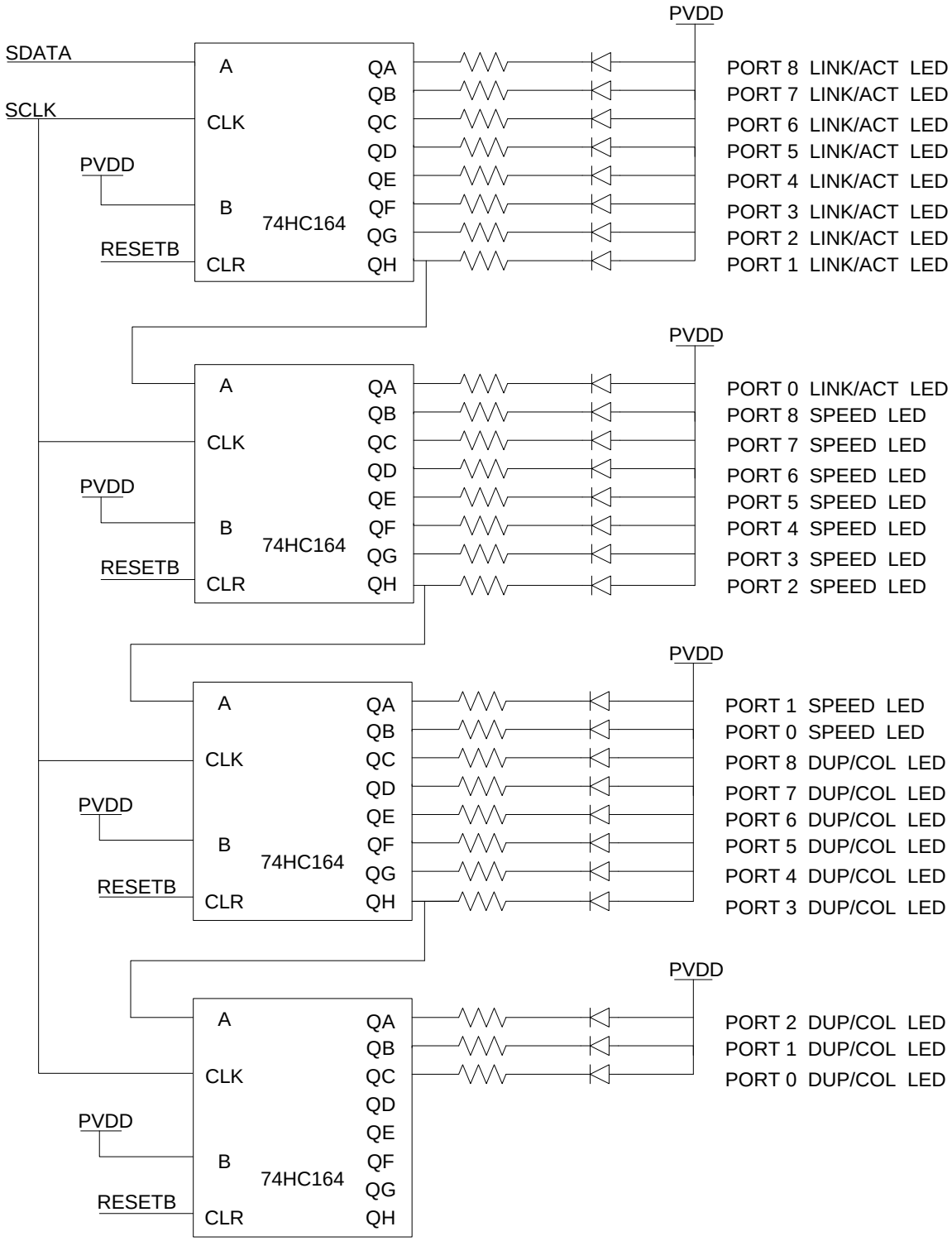
4.20.1 Supports Link LED Only

IP179N/H supports link LED only when setting SERIAL_LED_MODE to 1 and SERIAL_LED_EN to 1.



4.20.2 Supports Link, Speed, and Duplex LED

IP179N/H supports link, speed, and duplex LED when setting SERIAL_LED_MODE to 0 and SERIAL_LED_EN to 1.



4.21 LED Blink Timing

Table 1 LED Blink Timing

LED mode	Blinking speed
Serial mode update period	10ms
Active LED blink	Off 105ms → On 105ms → Off 105ms → …
Collision LED blink	Off 105ms → On 105ms → Off 105ms → …

Although the blinking period is the same for all ports, the LED of different port may blink in different phase.

4.22 Fiber Port Configuration

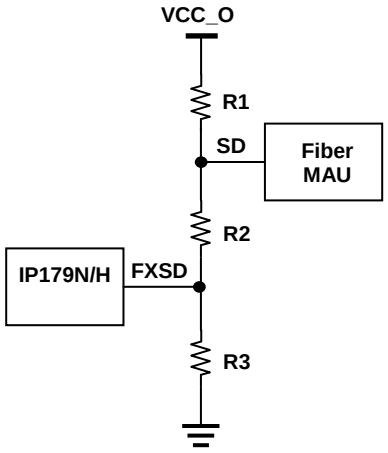
Port 6 ~ Port 8 of IP179N/H can be configured to be a fiber port or a TP port individually. A port becomes a fiber port if its FXSDx is connected to a fiber MAU or pulled to high. A port becomes a TP port if it's FXSDx is pulled low.

Table 2 Fiber port parameter

Parameter	Symbol	MIN.	Type	MAX.	Unit
Fiber Rx common mode Voltage	V_{FRC}	-	0.6*AV33	-	V
Fiber Rx differential mode Voltage	V_{FRD}	0.4	-	-	V

PVDD = 3.3V

Voltage on FXSDx	TP port	Fiber port	Fiber signal detect	Condition
< 0.4 V	Yes	--	--	
> 1.2 V < 1.7 V	--	Yes	Off	Fiber unplugged
> 1.95 V < 3.3 V	--	Yes	On	Fiber plugged



	Fiber MAU		
	3.3V SFP	3.3V 1x9	5V 1x9
R1	1K	1K	470
R2	50	100	300
R3	2K	910	330

5 PHY Register

5.1 PHY Register Map

Page	Register	Description	Default	Note
0	0	Control Register		PHY 8~15, 1
0	1	Status Register		PHY 8~15, 1
0	2	PHY Identifier 1 Register		PHY 8~15, 1
0	3	PHY Identifier 2 Register		PHY 8~15, 1
0	4	Auto-Negotiation Advertisement Register		PHY 8~15, 1
0	5	Auto-Negotiation Link Partner Ability Register		PHY 8~15, 1
0	6	Auto-Negotiation Expansion Register		PHY 8~15, 1
0	7	Auto-Negotiation Next Page Transmit Register		PHY 8~15, 1
0	8	Auto-Negotiation Link Partner Next Page Register		PHY 8~15, 1
0	13	MMD Access Control Register		PHY 8~15, 1
0	14	MMD Access Address Data Register		PHY 8~15, 1
0	3.0	PCS control 1 register		PHY 8~15, 1
0	3.1	PCS status 1 register		PHY 8~15, 1
0	3.20	EEE capability		PHY 8~15, 1
0	3.22	EEE wake error count		PHY 8~15, 1
0	7.60	EEE advertisement register		PHY 8~15, 1
0	7.61	EEE link partner ability		PHY 8~15, 1
0	16	Special Control Register (APS)		SHARE
0	18	Special Status Register		PHY 8~15, 1
0	23	MDI/MDIX Control Register		PHY 8~15, 1
X	20	Page Control Register		SHARE
3	16	LED Control Register		SHARE
6	16	LBAS Control Register		SHARE

Share: 9 PHYs share the register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High.

5.2 MII Register

5.2.1 MII Register 0

(Each PHY has its own MII register 0 with different PHY address)

PHY	MII	R/W	Description	Default
Control Register				
8~15 1	0.15	RW/ SC	Reset The PHY is reset if user writes “1” to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP179N/H.（according design should delete）	0
8~15 1	0.14	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, IP179N/H will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test. （according design should delete）	0
8~15 1	0.13	RW	Speed Selection 1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
8~15 1	0.12	RW	Auto-Negotiation(AN) Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
8~15 1	0.11	R/W	Power Down 1: power down mode 0: normal operation	0
8~15 1	0.10		Isolate IP179N/H doesn’t support this function.	0
8~15 1	0.9	RW SC	Restart Auto-Negotiation 1 = re-starting Auto-Negotiation 0: normal operation	0
8~15 1	0.8	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	1
8~15 1	0.7	R/W	Collision test	0
8~15 1	0[6:0]	RO	Reserved	0

5.2.2 MII Register 1

(Each PHY has its own MII register 1 with different PHY address)

PHY	MII	R/W	Description	Default
Status Register				
8~15 1	1.15	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP179N/H does not support 100Base-T4. This bit is fixed to be 0.	0
8~15 1	1.14	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
8~15 1	1.13	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
8~15 1	1.12	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
8~15 1	1.11	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
8~15 1	1.10	RO	100Base-T2 full duplex Capable 1 = 100Base-T2 full duplex capable 0 = not 100Base-T2 full duplex capable	0
8~15 1	1.9	RO	100Base-T2 half duplex Capable 1 = 100Base-T2 half duplex capable 0 = not 100Base-T2 half duplex capable	0
8~15 1	1.8	RO	Extended Status	0
8~15 1	1.7	RO	Reserved	1
8~15 1	1.6	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
8~15 1	1.5	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0
8~15 1	1.4	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP179N/H has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP179N/H reset.	0

PHY	MII	R/W	Description	Default
Status Register				
8~15 1	1.3	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP179N/H has the ability to perform Auto-Negotiation.	1
8~15 1	1.2	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP179N/H has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
8~15 1	1.1	RO LH	Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP179N/H has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP179N/H reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
8~15 1	1.0	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities IP179N/H has extended register capabilities.	1

5.2.3 MII Register 2

(Each PHY has its own MII register 2 with different PHY address)

PHY	MII	R/W	Description	Default
PHY Identifier 1 Register				
8~15 1	2	RO	IP179N/H OUI (Organizationally Unique Identifier) ID, the MSB is 3rd bit of IP179N/H OUI ID, and the LSB is 18th bit of IP179N/H OUI ID. IP179N/H OUI is 0090C3.	16'h0243

5.2.4 MII Register 3

(Each PHY has its own MII register 3 with different PHY address)

PHY	MII	R/W	Description	Default
PHY Identifier 2 Register				
8~15 1	3[15:10]	RO	PHY identifier IP179N/H OUI ID, the MSB is 19th bit of IP179N/H OUI ID, and LSB is 24th bit of IP179N/H OUI ID.	6'h03
8~15 1	3[9:4]	RO	Manufacture's Model Number IP179N/H model number	6'h01
8~15 1	3[3:0]	RO	Revision Number IP179N/H revision number	0

5.2.5 MII Register 4

(Each PHY has its own MII register 4 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Advertisement Register				
8~15 1	4.15	R/W	1 = Next pages are supported 0 = Next pages are not supported	0
8~15 1	4.14	RO	Reserved by IEEE, write as 0, ignore on read	0
8~15 1	4.13	R/W	Remote Fault 1 = Advertises that this port has detected a remote fault. 0 = There is no remote fault.	0
8~15 1	4.12	RO	Reserved for future IEEE use, write as 0, ignore on read	0
8~15 1	4.11	RW	Asymmetric PAUSE 1 = Asymmetric flow control is supported 0 = Asymmetric flow control is not supported	1
8~15 1	4.10	RW	PAUSE 1 = Symmetric flow control is supported 0 = Symmetric flow control is not supported	1
8~15 1	4.9	RO	100BASE-T4 Not supported	0
8~15 1	4.8	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
8~15 1	4.7	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
8~15 1	4.6	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
8~15 1	4.5	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
8~15 1	4[4:0]	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	5'b00001

5.2.6 MII Register 5

(Each PHY has its own MII register 5 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Ability Register				
8~15 1	5.15	RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
8~15 1	5.14	RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
8~15 1	5.13	RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
8~15 1	5.12	RO	Reserved by IEEE for future use, write as 0, and read as 0.	0
8~15 1	5.11	RO	Asymmetric PAUSE 1 = Link partner support Asymmetric PAUSE 0 = Link partner does not support Asymmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4.[11:10].	0
8~15 1	5.10	RO	PAUSE 1 = Link partner support Symmetric PAUSE 0 = Link partner does not support Symmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4.[11:10].	0
8~15 1	5.9	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
8~15 1	5.8	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
8~15 1	5.7	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
8~15 1	5.6	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
8~15 1	5.5	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T When AN is disabled, this bit is set if register 0.13=0	0
8~15 1	5[4:0]	RO	Selector Field Protocol selector of the link partner	5’b00000

5.2.7 MII Register 6

(Each PHY has its own MII register 6 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Expansion Register				
8~15 1	6[15:5]	RO	Reserved	0
8~15 1	6.4	RO/ LH	Parallel Detection Fault 1 = a fault has been detected via parallel detection function. 0 = a fault has not been detected via parallel detection function.	0
8~15 1	6.3	RO	Link Partner Next Page Able 1 = Link partner is next page able. 0 = Link partner is not next page able.	0
8~15 1	6.2	RO	Next Page Able 1 = IP179N/H next page able. 0 = IP179N/H is not next page able.	1
8~15 1	6.1	RO/ LH	Page Recieved 1 = A new page has been received. 0 = A new page has not been received.	0
8~15 1	6.0	RO	If AN is enabled, this bit means: 1 = Link partner is Auto-Negotiation able. 0 = Link partner is not Auto-Negotiation able. In 100FX or AN disabled, then this bit is always equal to 0.	0 (AN) (100FX)

5.2.8 MII Register 7

(Each PHY has its own MII register 7 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Next Page Transmit Register				
8~15 1	7.15	RW	Next Page Transmit Code Word Bit 15	0
8~15 1	7.14	RO	Reserved Transmit Code Word Bit 14	0
8~15 1	7.13	RW	Message Page Transmit Code Word Bit 13	1
8~15 1	7.12	RW	Acknowledge 2 Transmit Code Word Bit 12	0
8~15 1	7.11	RO	Toggle Transmit Code Word Bit 11	0
8~15 1	7[10:0]	RW	Message/Unformatted Field Transmit Code Word Bit 10:0	1

5.2.9 MII Register 8

(Each PHY has its own MII register 8 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Next Page Register				
8~15 1	8.15	RO	Next Page Received Code Word Bit 15	0
8~15 1	8.14	RO	Acknowledge Received Code Word Bit 14	0
8~15 1	8.13	RO	Message Page Received Code Word Bit 13	0
8~15 1	8.12	RO	Acknowledge 2 Received Code Word Bit 12	0
8~15 1	8.11	RO	Toggle Received Code Word Bit 11	0
8~15 1	8[10:0]	RO	Message/Unformatted Field Received Code Word Bit 10:0	0

5.2.10 MII Register 16

(9 PHYs share the MII register)

PHY	MII	R/W	Description	Default
Special Control Register				
8~15 1	16.7	RW	Advance power saving mode 1 = Enable APS mode (Default) 0 = Disable APS mode Please refer to the Power Saving application note for more detail description.	1
8~15 1	16.4	RW	Far end fault function 1 = Far end fault function disable 0 = Far end fault function enable (Default) This bit is only used for fiber mode.	0

5.2.11 MII Register 18

(Each PHY has its own MII register 18 with different PHY address)

PHY	MII	R/W	Description	Default
Special Status Register				
8~15 1	18.14	RO	Linkup 1 = linkup 0 = unlink	0
8~15 1	18.11	RO	Speed Mode 1 = 100 Mbps 0 = 10 Mbps	0
8~15 1	18.10	RO	Duplex Mode 1 = Full Duplex 0 = Half Duplex	0

5.2.12 MII Register 23

(Each PHY has its own MII register 23 with different PHY address)

PHY	MII	R/W	Description	Default
MDI/MDIX Control Register				
8~15 1	23[15:8]	RW	Reserved	0
8~15 1	23.7	RW	Reserved	0
8~15 1	23.6	RW	Reserved	1
8~15 1	23.5	RW	Reserved	0
8~15 1	23.4	RW	Reserved	1
8~15 1	23.3	RW	Reserved	0
8~15 1	23.2	RW	Reserved	1
8~15 1	23.1	RW	Auto MDI/MDIX function 1 = Enable auto MDI/MDIX function (Default) 0 = Disable auto MDI/MDIX function	1
8~15 1	23.0	RW	MDI/MDIX selection 1 = MDIX mode 0 = MDI mode(Default)	0

5.3 MMD Control Register

MII register 13 (Each PHY has its own MII register 13 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Control Register				
8~15 1	13[15:14]	R/W	Function 00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	0
8~15 1	13[13:5]	RO	Reserved Write as 0, ignore on read	0
8~15 1	13[4:0]	R/W	DEVAD Device Address	0

MII register 14 (Each PHY has its own MII register 14 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Address Data Register				
8~15 1	14[15:0]	R/W	Address Data If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	0

Example 1, Read 0.3.20 (Read Data from MMD register 3.20 of PHY address 0):

1. Write 0.13 = 0x0003 //MMD DEVAD 3
2. Write 0.14 = 0x0014 //MMD Address 20
3. Write 0.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 0.14 //Read MMD Data from 0.3.20

Example 2, Write 1.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 1):

1. Write 1.13 = 0x0007 //MMD DEVAD 7
2. Write 1.14 = 0x003C //MMD Address 60
3. Write 1.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 1.14 = 0x3210 //Write MMD Data 0x3210 to 1.7.60

5.4 MMD Data Register

MMD register 3.0 (Each PHY has its own MMD register 3.0 with different PHY address)

PHY	MII	R/W	Description	Default
PCS control 1 Register				
8~15 1	3.0[15:11]	RO	Reserved Ignore when read	0
8~15 1	3.0.10	R/W	Clock stop enable 1 = PHY may stop xMII Rx clock during LPI（IP179N/H doesn't support） 0 = Clock not stoppable	0
8~15 1	3.0[9:0]	RO	Reserved Ignore when read	0

MMD register 3.1 (Each PHY has its own MMD register 3.1 with different PHY address)

PHY	MII	R/W	Description	Default
PCS status 1 Register				
8~15 1	3.1[15:12]	RO	Reserved Ignore when read	0
8~15 1	3.1.11	RO/LH	Tx LPI received 1 = Tx PCS has received LPI 0 = LPI not received	0
8~15 1	3.1.10	RO/LH	Rx LPI received 1 = Rx PCS has received LPI 0 = LPI not received	0
8~15 1	3.1.9	RO	Tx LPI indication 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
8~15 1	3.1.8	RO	Rx LPI indication 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
8~15 1	3.1.7	RO	Reserved Ignore on read	0
8~15 1	3.1.6	RO	Clock stop capable 1 = The MAC may stop the xMII Tx clock during LPI 0 = Clock not stoppable	0
8~15 1	3.1[5:0]	RO	Reserved Ignore when read	0

MMD register 3.20 (Each PHY has its own MMD register 3.20 with different PHY address)

PHY	MII	R/W	Description	Default
EEE capability Register				
8~15 1	3.20[15:7]	RO	Reserved Ignore when read	0
8~15 1	3.20.6	RO	10GBASE-KR EEE 1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	0
8~15 1	3.20.5	RO	10GBASE-KX4 EEE 1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	0
8~15 1	3.20.4	RO	1000BASE-KX EEE 1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	0
8~15 1	3.20.3	RO	10GBASE-T EEE 1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	0
8~15 1	3.20.2	RO	1000BASE-T EEE 1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	0
8~15 1	3.20.1	RO	100BASE-TX EEE 1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	1
8~15 1	3.20.0	RO	Reserved Ignore when read	0

MMD register 3.22 (Each PHY has its own MMD register 3.22 with different PHY address)

PHY	MII	R/W	Description	Default
EEE wake error count				
8~15 1	3.22[15:0]	RO	EEE wake error count Count wake time faults where IP179N/H fails to complete its normal wake sequence within the time required for the specific PHY type. This register keeps the value before reading the contents of the register.	0x0000

MMD register 7.60 (Each PHY has its own MMD register 7.60 with different PHY address)

PHY	MII	R/W	Description	Default
EEE advertisement Register				
8~15 1	7.60[15:7]	RO	Reserved Ignore when read	0
8~15 1	7.60.6	RO	10GBASE-KR EEE 1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	0
8~15 1	7.60.5	RO	10GBASE-KX4 EEE 1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	0

MMD register 7.60 (Each PHY has its own MMD register 7.60 with different PHY address)

PHY	MII	R/W	Description	Default
8~15 1	7.60.4	RO	1000BASE-KX EEE 1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	0
8~15 1	7.60.3	RO	10GBASE-T EEE 1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	0
8~15 1	7.60.2	RO	1000BASE-T EEE 1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	0
8~15 1	7.60.1	R/W	100BASE-TX EEE 1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	1
8~15 1	7.60.0	RO	Reserved Ignore when read	0

MMD register 7.61 (Each PHY has its own MMD register 7.61 with different PHY address)

PHY	MII	R/W	Description	Default
EEE link partner ability				
8~15 1	7.61[15:7]	RO	Reserved Ignore when read	0
8~15 1	7.61.6	RO	10GBASE-KR EEE 1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	0
8~15 1	7.61.5	RO	10GBASE-KX4 EEE 1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for 10GBASE-KX4	0
8~15 1	7.61.4	RO	1000BASE-KX EEE 1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	0
8~15 1	7.61.3	RO	10GBASE-T EEE 1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	0
8~15 1	7.61.2	RO	1000BASE-T EEE 1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	0
8~15 1	7.61.1	RO	100BASE-TX EEE 1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	0
8~15 1	7.61.0	RO	Reserved Ignore when read	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.5 LED Mode Control Register

MII page3 register16 of PHY0 (9 PHYs share the MII register)

page	MII	R/W	Description	Default
LED Control Register				
3	16[15:14]	R/W	LED_SEL[1:0] LED output mode selection. LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 (default)	11
	16.12	RW	SERIAL_LED_EN 1: supports LED serial mode 0: supports LED direct mode (default)	0
	16.11	RW	SERIAL_LED_MODE 1: supports link LED only 0: supports link, speed, and duplex LED (default)	0
	16.10	RW	Serial upd fast 1:10ms(default) 0:20ms	1

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

LED mode behavior:

	LED mode 0	LED mode 1	LED mode 2	LED mode 3
LED_SEL[1:0]	00	01	10	11
LINK_LED[8:0]	100M Link + Activity (1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity)	Link (1: link fail, 0: link ok)	100M Link + Activity (same as mode 0)	Link + Activity (1: link fail, 0: link ok, flash: Link ok and TX/ RX activity)
SPEED_LED[8:0]	flash: Link ok and TX/ RX activity	flash: Link ok and TX/ RX activity	Full/half (1: half, 0: full, flash: collision)	Speed (1: speed=10M, 0: speed=100M
FULL_LED[8:0]	0: 10M Link ok 1: 100M Link ok	Full/half (same as mode 3)	10M Link + Activity (1: 10M Link fail, 0: 10M Link ok and no activity, flash: 10M Link ok and TX/RX activity)	Full/half (1: half, 0: full, flash: collision)

5.6 WOL Control Register

MII page4 register16 (9 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL Control Register				
4	16.[15]	RW	WOL Interrupt Enable Set high to enable WOL interrupt 1=Enable 0=Disable Each PHY address can access the register of the corresponding port.	0
	16.[14]	RW	Reserved	1
	16.[13]	RW	Reserved	0
	16.[12]	RW	Sense Link Change Set high to enable WOL interrupt when link change is sensing. 1=Enable 0=Disable	0
	16.[11]	RW	Sense Magic Packet Set high to enable WOL interrupt when magic packet is receiving. 1=Enable 0=Disable	1
	16.[10]	RW	Sense Any Packet Set high to enable WOL interrupt when any packet is receiving. 1=Enable 0=Disable	0
	16.[9]	RW	Reserved	1
	16.[8]	RW	Reserved	0
	16.[7:1]	RO	Reserved	0x00
	16.[0]	RO	PHY WOL Interrupt Status Interrupt Status Each PHY address can access the register of the corresponding port.	1

MII page5 register16 (9 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL MAC Address Register_0~2				
5	16[15:0]	R/W	WOL MAC Address_0~2 WOL MAC Address = {WOL_MAC_Address_0, WOL_MAC_Address_1, WOL_MAC_Address_2}	0x0000

5.7 LBAS Control Register

MII page6 register16 (9 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY LBAS Control Register				
6	16[15:12]	R/W	AN_FAIL_CNT[3:0]	0100
	16[10]	R/W	LBAS (Length/Link Based Auto Switch) 1 = LBAS is supported for PHY 8~15 0 = LBAS is not supported for PHY 8~15	1

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Example 1, Read page3 register16 (Read Data from page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Read 0.16 //Read Data from page3 register16
3. Write 0.20 = 0x0000 //restore to page0

Example 2, Write page3 register16 = 0x3400 (Write Data 0x3400 to page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Write 0.16 = 0x3400 //Write Data 0x3400 to page3 register16
3. Write 0.20 = 0x0000 //restore to page0

5.8 Page Mode Control Register

MII register 20 (9 PHYs share the MII register)

PHY	MII	R/W	Description	Default
Page Control Register				
8~15 1	20[4:0]	RW	Reg16~31_Page_Sel[4:0]	00000

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6 Switch Register Descriptions

The IP179N/H can be configured via external EEPROM interface at boot time. During operation, IP179N/H registers are accessible via SMI interface.

6.1 Switch Register Map

	PHY 20
REG 0	Software Reset
REG 1	Basic Register 0
REG 2	Basic Register 1
REG 3	Basic Register 2
REG 4	Learn/Forward Enable
REG 5	
REG 6	
REG 7	
REG 8	QoS
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	
REG 15	
REG 16	Test Mode
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	
REG 25	
REG 26	
REG 27	
REG 28	
REG 29	
REG 30	
REG 31	

	PHY 21
REG 0	IGMP
REG 1	
REG 2	
REG 3	
REG 4	Age Time
REG 5	
REG 6	Loop Detection
REG 7	
REG 8	MAC Table Accessing
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	Link Aggregation
REG 15	
REG 16	
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	Port Mirror
REG 25	
REG 26	
REG 27	Reserved MAC Address
REG 28	Broadcast Storm Protection
REG 29	Statistics Counter
REG 30	
REG 31	

	PHY 22
REG 0	VLAN Classification
REG 1	
REG 2	VLAN Ingress Rule
REG 3	VLAN Egress Rule
REG 4	
REG 5	Default VLAN Information
REG 6	
REG 7	
REG 8	
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	
REG 15	VLAN Table Enable Mask
REG 16	Port-Based VLAN – VLAN Forward Mask
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	
REG 25	EEE
REG 26	
REG 27	
REG 28	
REG 29	
REG 30	
REG 31	

	PHY 23
REG 0	Port-Based VLAN – Add Tag Mask
REG 1	
REG 2	
REG 3	
REG 4	
REG 5	
REG 6	
REG 7	
REG 8	
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	
REG 15	
REG 16	Port-Based VLAN – Remove Tag Mask
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	
REG 25	PHY Address
REG 26	
REG 27	
REG 28	WoL
REG 29	External PHY Register
REG 30	
REG 31	EEPROM Segment ID

	PHY 24
REG 0	VLAN Table – VID and FID
REG 1	
REG 2	
REG 3	
REG 4	
REG 5	
REG 6	
REG 7	
REG 8	
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	
REG 15	
REG 16	VLAN Table – Add Tag Mask
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	
REG 25	
REG 26	
REG 27	
REG 28	
REG 29	
REG 30	
REG 31	

	PHY 25
REG 0	VLAN Table – Remove Tag Mask
REG 1	
REG 2	
REG 3	
REG 4	
REG 5	
REG 6	
REG 7	
REG 8	
REG 9	
REG 10	
REG 11	
REG 12	
REG 13	
REG 14	
REG 15	
REG 16	VLAN Table – Forward Mask
REG 17	
REG 18	
REG 19	
REG 20	
REG 21	
REG 22	
REG 23	
REG 24	
REG 25	
REG 26	
REG 27	
REG 28	
REG 29	
REG 30	
REG 31	

6.2 Switch Control Register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only

6.2.1 Software Reset

PHY	MII	ROM	R/W	Description	Default
20	0		WO	Software reset register MII register 0 is software reset register. User can reset IP179N/H by writing 55AA to this register.	
	0[0]		RO	PKG_128 0: 88 pins 1: 128 pins	

6.2.2 Switch Basic Registers 0

PHY	MII	ROM	R/W	Description	Default
20	1[15:13]			Reserved	
	1[12]		R/W	ALL_PASS	0x0
	1[11:8]			Reserved	
	1[7]		R/W	TABLE_LOCK Lock MAC table	0x0
	1[6]			Reserved	
	1[5]		R/W	X_EN IEEE 802.3x flow control enable 1: Enable (default) 0: Disable	0x1
	1[4]		R/W	BK_EN, Backpressure enable 1: Enable (default) 0: Disable	0x1
	1[3]		R/W	Drop16 1: Enable 0: Disable (default)	0x0
	1[2]		R/W	TWOPART	0x0
	1[1]		R/W	MODBCK. Turn on modified back off algorithm The maximum back off period is limited to 8-slot time if this function is turned on. 1: Turn on 0: Turn off	0x0
	1[0]		R/W	LEARN_DIS_PAUSE PAUSE packet does not perform address learning	0x1

6.2.3 Switch Basic Registers 1

PHY	MII	ROM	R/W	Description	Default
20	2[15:11]			Reserved	
	2[10:8]		R/W	INT_EVENT Bit 0: Reserved Bit 1: WOL interrupt Bit 2: Reserved	0x1
	2[7:4]		R/W	LEAKY_VLAN Bit 0: Unicast Address Bit 1: Multicast Address Bit 2: Broadcast Address Bit 3: ARP Address	0x0
	2[3]			Reserved	
	2[2]		R/W	HP_DIS_FLOW_EN Disable flow control when received high priority packet	0x0
	2[1:0]		R/W	LONG_PACKET 2'b00: 1536 bytes (default) 2'b01: 1552 bytes 2'b10: 1522 bytes 2'b11: reserved	0x0

6.2.4 Switch Basic Registers 2

PHY	MII	ROM	R/W	Description	Default
20	3[15:7]			Reserved	0x0
	3[6:4]		R/W	FIBER_DUPLEX Fiber duplex setting for each port. 1: Fiber port is full-duplex 0: Fiber port is half-duplex	0x7
	3[3]			Reserved	
	3[2]			Reserved	
	3[1]		R/W	STAG_TX_EN Special tagging for TX enable 1: Enable 0: Disable (default)	0x0
	3[0]		R/W	STAG_RX_EN Special tagging for RX enable 1: Enable 0: Disable (default)	0x0

6.2.5 Learn & Forward Enable Register

PHY	MII	ROM	R/W	Description	Default
20	4[8:0]		R/W	PORT_FWD_EN Frame forwarding capability enable for each port	0x1FF
	5[8:0]		R/W	PORT_LEARN_EN MAC address Learning capability enable for each port	0x1FF
	6[8:0]		R/W	PORT_FLOOD_FRM Received frames can be flooded	0x000
	7[15:9]			Reserved	
	7[8]		R/W	CHK_VLAN If CHK_VLAN for a given port is set, frame ignore SMAC learning on that port whose VLAN classification does not include that port in it member set.	0x0
	7[7:6]		R/W	FILTER_MDMAC Filter unknown multicast DMAC 2'b00 : Flooding (default) 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved Note : Multicast DMAC does not include broadcast DMAC	0x0
	7[5:4]		R/W	FILTER_UDMAC Filter unknown unicast DMAC 2'b00 : Flooding (default) 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved	0x0
	7[3]		R/W	FLUSH_EN Memory flush delete unlink entries	0x1
	7[2]		R/W	AT_STR Address Table Structure 0: 2K Address Table for unicast frame (default) 1: 1K Address Table for unicast frame and 1K Address Table for multicast frame	0x0
	7[1]			IGMP_LEARN_CONSTRAIN 1: SVL 0: IVL	
	7[0]		R/W	LEARN_CONSTRAIN Learning Constraint 0 : VLAN information(FID) is not used to create a hash key 1 : VLAN information(FID) is used to create a hash key	0x0

6.3 QoS

PHY	MII	ROM	R/W	Description	Default
20	8[15]		R/W	TOS_OVER_VLAN ToS Precedence over VLAN Priority	0x0
	8[14]			SP_EN Strict Priority Enable 1: Enable 0: Disable (default)	0x0
	8[13:9]			Reserved	
	8[8:0]		R/W	COS_EN Class of Service Enable Frame Based QoS 1: Enable 0: Disable (default)	0x000
	9[8:0]		R/W	PORT_PRI_EN Port Based QoS 1: Enable 0: Disable (default)	0x000
	10[8:0]		R/W	PORT_PRI 1: High priority 0: Low priority (default)	0x000
	11[15:8]		R/W	VLAN_PRI2Q To map a VLAN priority to different output queue VLAN priority 7~0 to Queue 1: High priority 0: Low priority (default)	0x0
	11[7:4]		R/W	WRR_WEIGHT_1 Queue 1 Weight	0xF
	11[3:0]		R/W	WRR_WEIGHT_0 Queue 0 Weight	0x1
	12[15:0]		R/W	DSCP2Q_0 To map a DSCP to different output queue DSCP F ~ 0 to Queue 1: High priority 0: Low priority (default)	0x0000
	13[15:0]		R/W	DSCP2Q_1 DSCP 1F ~ 10 to Queue 1: High priority 0: Low priority (default)	0x0000

PHY	MII	ROM	R/W	Description	Default
	14[15:0]		R/W	DSCP2Q_2 DSCP 2F ~ 20 to Queue 1: High priority 0: Low priority (default)	0x0000
	15[15:0]		R/W	DSCP2Q_3 DSCP 3F ~ 30 to Queue 1: High priority 0: Low priority (default)	0x0000

6.4 Debug Register

6.4.1 Test Mode Register for Debug

PHY	MII	ROM	R/W	Description	Default
20	16[13:4]		R/W	TEST_LATIN (only for PHY test mode)	*
	16[1:0]		R/W	TEST_SEL 0x0: Normal mode 0x1: Switch test mode 0x2: PHY test mode	0x0

6.4.2 MII Loopback for Debug

PHY	MII	ROM	R/W	Description	Default
	17[15:9]			Reserved	
	17[8:0]		R/W	MII_LOOPBACK	0x0

6.5 IGMP Control Registers

6.5.1 Base Control Registers

PHY	MII	ROM	R/W	Description	Default
21	0[15:11]			Reserved	
	0[10]		R/W	FAST_LEAVE	0x1
	0[9]		R/W	MG_INCLUDE_RP Multicast group include router port 1: Enable 0: Disable	0x0
	0[8]		R/W	FLOOD_UNIGMP Flood Unknown IGMP 1: Enable 0: Disable Note – Unknown IGMP is not one of following: 1. General Query 2. Group-Specific Query 3. IGMP Report 4. IGMP Leave	0x0
	0[7]		R/W	FLOOD_IPM_CTRL Flood IP Multicast Control Packet 1: Enable 0: Disable Note – IP multicast control packet: DMAC=01-00-5e-xx-xx-xx, DIP= 224.0.0.x and non-IGMP	0x0
	0[6:5]		R/W	UNIPM_MODE[1:0] Unknown IP Multicast Data Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : forward to router port Note – IP multicast data packet: DMAC=01-00-5e-xx-xx-xx and DIP=outside 224.0.0.x	0x3
	0[4]		R/W	DISCARD_LEAVE Discard IGMP leave message 1: Enable 0: Disable	0x0
	0[3]		R/W	FLOOD_RPT Flood report message to other ports 1: Enable 0: Disable	0x0

PHY	MII	ROM	R/W	Description	Default
	0[2]		R/W	LRP_NULL_SIP Learn router port even if source IP address is 0.0.0.0 1: Enable 0: Disable It is valid only if LEARN_RP is enabled	0x0
	0[1]		R/W	LEARN_RP Learn Router Port 1: Enable 0: Disable (default)	0x0
	0[0]		R/W	HW_IGMP_EN Hardware IGMP Enable 1: Enable 0: Disable (default)	0x0

6.5.2 Router Port Timeout

PHY	MII	ROM	R/W	Description	Default
21	1[8:0]		R/W	DEFAULT_ROUTER_PORT[8:0]	0x000
	2[11:4]			ROUTER_TIMEOUT_VLE[7:0] Router Timeout Value Router Timeout = ROUTER_TIMEOUT_UNIT * ROUTER_TIMEOUT_VLE	0x000
	2[1:0]			ROUTER_TIMEOUT_UNIT[1:0] 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	0x0

6.5.3 Group Port Timeout

PHY	MII	ROM	R/W	Description	Default
21	3[11:7]			IGMP_TIMEOUT_VLE[7:0] IGMP Timeout Value IGMP Timeout = IGMP_TIMEOUT_UNIT * IGMP_TIMEOUT_VLE	0x000
	3[1:0]			IGMP_TIMEOUT_UNIT[1:0] IGMP Timeout Unit 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	0x0

6.6 Aging Time Registers

PHY	MII	ROM	R/W	Description	Default
21	4[15]		R/W	PORT_MAP_EN If set, the aging module ages entries whose Port matches PORT_MAP	0x0
	4[14]		R/W	FID_EN If set, the aging module ages entries whose FID matches FID_VAL 1: Enable 0: Disable	0x0
	4[13:10]			Reserved	
	4[9:8]			AGE_TIME_UNIT 2'b00 : 1 minutes 2'b01 : 1 second 2'b10 : 10 ms 2'b11 : Fast (MAC table is cleared after about 0.5ms)	0x0
	4[4:0]		R/W	AGE_TIME_VLE Age Time Value. 5'h00: no aging AGE_TIME= AGE_TIME_UNIT * AGE_TIME_VLE AGE_TIME_UNIT=fast, AGE_TIME_VLE is invalid.	0x5
	5[15:120]			FID_VLE[3:0] FID Value	0x0
	5[11:9]			Reserved	
	5[8:0]			PORT_MAP[3:0] Port MAP	0x0

6.7 Address Table Accessing Registers

6.7.1 Command Registers

PHY	MII	ROM	R/W	Description	Default
21	8[15]		R/W (SC)	START/DONE To initiate a read or write command when set as 1. Self-cleared after read or write command is finished 1: start access the address table 0: access operation is completed	0x0
	8[14]		R/W	COMMAND Address Table Command 0x0: read 0x1: write	0x0
	8[10:0]		R/W	INDEX The index selects one of address table entries	0x000

6.7.2 Data Registers

PHY	MII	ROM	R/W	Description	Default
21	9[15:0]		R/W	MAC[15:0]	0x0000
	10[15:0]		R/W	MAC[31:16]	0x0000
	11[15:0]		R/W	MAC[47:32]	0x0000
	12[15:12]		R/W	FID	0x0
	12[11:9]			Reserved	
	12[8:0]		R/W	PORT_MAP	0x000
	13[15]		R/W	STATIC/VALID Unicast address: Static entry Multicast address: Valid entry	0x0
	13[14:1]			Reserved	
	13[0]		R/W	AGE 1: the entry is aged out (only for unicast address)	0x0

6.7.3 IGMP Data Registers

PHY	MII	ROM	R/W	Description	Default
21	9[15:0]		R/W	MAC[15:0]	0x0000
	10[6:0]		R/W	MAC[22:16]	0x0000
	11[15:0]		R/W	Reserved	
	12[15:12]		R/W	FID	0x0
	12[11:9]			Reserved	
	12[8:0]		R/W	PORT_MAP	0x000
	13[15]		R/W	VALID Valid entry	0x0
	13[14]		R/W	IGMP_ENTRY	0x0
	13[13:9]			Reserved	
	13[8:0]		R/W	TIMEOUT 1: the entry is aged out	0x000

6.8 MAC/IP Table Accessing Registers

6.8.1 Command Registers

PHY	MII	ROM	R/W	Description	Default
21	8[13]		R/W	DISPLAY_SRC_ADR Display the source MAC and IP address associated with the source port.	0x0
	8[12]		RO	SIP_ADR_VALID Source IP address field of entry content is valid. 1: Valid 0: Invalid	0x0
	8[11]		RO	SMAC_ADR_VALID Source MAC address field of entry content is valid. 1: Valid 0: Invalid	0x0
	8[3:0]		R/W	SRC_PORT Source port 0x0: Port0 0x1: Port1 0x2: Port2 0x3: Port3 0x4: Port4 0x5: Port5 0x6: Port6 0x7: Port7 0x8: Port8	0x0

6.8.2 Data Registers

PHY	MII	ROM	R/W	Description	Default
21	9[15:0]		RO	SRC_MAC_ADDR[15:0] Source MAC address[15:0]	0x0000
	10[15:0]		RO	SRC_MAC_ADDR[31:16] Source MAC address[31:16]	0x0000
	11[15:0]		RO	SRC_MAC_ADDR[47:32] Source MAC address[47:32]	0x0000
	12[15:0]		RO	SIP[15:0] Source IP address[15:0]	0x0000
	13[15:0]		RO	SIP[31:16] Source IP address[31:16]	0x0000

6.9 Port Trunk Registers

6.9.1 Trunk Groups

PHY	MII	ROM	R/W	Description	Default
21	14[14:13]			AGGR_MODE Aggregation Mode 2'b00: Source port 2'b01: SMAC 2'b10: DMAC 2'b11: SMAC xor DMAC	0x0
	14[8:0]		R/W	AGGR_GROUP_0	0x000
	15[8:0]		R/W	AGGR_GROUP_1	0x000

6.9.2 Trunk Table

PHY	MII	ROM	R/W	Description	Default
21	16[8:0]		R/W	AGGR_0 Only one port can be selected in each aggregation group	0x1FF
	17[8:0]		R/W	AGGR_1	0x1FF
	18[8:0]		R/W	AGGR_2	0x1FF
	19[8:0]		R/W	AGGR_3	0x1FF
	20[8:0]		R/W	AGGR_4	0x1FF
	21[8:0]		R/W	AGGR_5	0x1FF
	22[8:0]		R/W	AGGR_6	0x1FF
	23[8:0]		R/W	AGGR_7	0x1FF

6.10 Port Mirror Registers

PHY	MII	ROM	R/W	Description	Default
21	24[15]		R/W	MIR_EN	0x0
	24[14]		R/W	ONLY_MIR_PKT Mirror port only transmit the mirrored packets	0x0
	24[13:12]		R/W	MIR_MODE Captured Condition 0x0: mirror RX (default) 0x1: mirror TX 0x2: mirror RX and TX 0x3: mirror RX or TX	0x0
	24[11:9]			Reserved	
	24[8:0]		R/W	MIR_PORT	0x000
	25[8:0]		R/W	MIR_RX	0x000
	26[8:0]		R/W	MIR_TX	0x000

6.11 Reserved MAC Registers

PHY	MII	ROM	R/W	Description	Default
21	27[15:12]			Reserved	
	27[11]		R/W	BLK_RSVD_MAC[11] 01-80-C2-00-00-30 ~ 01-80-C2-00-00-FF	0x0
	27[10]		R/W	BLK_RSVD_MAC[10] 01-80-C2-00-00-22 ~ 01-80-C2-00-00-2F	0x0
	27[9]		R/W	BLK_RSVD_MAC[9] 01-80-C2-00-00-21	0x0
	27[8]		R/W	BLK_RSVD_MAC[8] 01-80-C2-00-00-20	0x0
	27[7]		R/W	BLK_RSVD_MAC[7] 01-80-C2-00-00-11 ~ 01-80-C2-00-00-1F	0x0
	27[6]		R/W	BLK_RSVD_MAC[6] 01-80-C2-00-00-10	0x0
	27[5]		R/W	BLK_RSVD_MAC[5] 01-80-C2-00-00-04 ~ 01-80-C2-00-00-0D 01-80-C2-00-00-0F	0x0
	27[4]		R/W	BLK_RSVD_MAC[4] 01-80-C2-00-00-0E	0x0
	27[3]		R/W	BLK_RSVD_MAC[3] 01-80-C2-00-00-03	0x0
	27[2]		R/W	BLK_RSVD_MAC[2] 01-80-C2-00-00-02	0x0
	27[1]		R/W	BLK_RSVD_MAC[1] 01-80-C2-00-00-01	0x1

PHY	MII	ROM	R/W	Description	Default
	27[0]		R/W	BLK_RSVD_MAC[0] 01-80-C2-00-00-00 0x0: forward 0x1: discard	0x0

6.12 Broadcast Storm Protection

PHY	MII	ROM	R/W	Description	Default
21	28[15]		R/W	BF_STM_EN, Broadcast storm enable 1: Enable Switch drops the incoming packet if the number of broadcast packet in queue is over the threshold. 0: Disable	0x0
	28[14]		R/W	BF_FFFF_ONLY 1: Broadcast DA=FFFFFFFF 0: Broadcast DA=FFFFFFFF and multicast frame	0x0
	28[10:0]		R/W	BF_THR[10:0]. Broadcast storm threshold During Time intervals, the amount of broadcast traffic exceeded the configured threshold would be dropped. T=1ms for 1000Mbps; T=10ms for 100Mbps; T=100ms for 10Mbps	0x100

6.13 Statistics Counters Registers

PHY	MII	ROM	R/W	Description	Default
21	29[15]		R/W (SC)	CLR_STATS_CNT	0x0
	29[14:11]			Reserved	
	29[10:8]			SEL_STATS_CNT Statistics Counter Selection 0x0: FCS error packet counter 0x1: Received packet counter 0x2: Transmitted packet counter 0x3: Global FCS error packet counter	0x0
	29[7:4]			Reserved	
	29[3:0]		R/W	SEL_STATS_PORT Statistics Port Selection	0x0
	30		RO	STATS_CNT_LWORD	0x0
	31		RO	STATS_CNT_HWORD	0x0

6.14 VLAN Registers

6.14.1 VLAN Classification

PHY	MII	ROM	R/W	Description	Default
22	0[13:12]			UNVID_MODE[1:0] Unknown-VID Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : reserved	0x0
	0[8:0]		R/W	VLAN_MODE[8:0] VLAN Mode setting associated with each port 0 : Port-based VLAN (default) 1 : Tagged-based VLAN	0x000
	1[8:0]		R/W	VLAN_CLS[8:0] VLAN Classification associated with each port Only active at tagged-based VLAN 0 : Use VID to classify VLAN - use VID to search VLAN table if tag packet - use PVID to search VLAN table if untag packet 1 : Use PVID to classify VLAN - always use PVID to search VLAN table	0x000

6.14.2 VLAN Ingress Rule

PHY	MII	ROM	R/W	Description	Default
22	2[13:12]		R/W	ACCEPTABLE_FRM_TYPE[1:0] Acceptable Frame Type 2'b00 Admit all frames (default) 2'b01 Admit VLAN-tagged frames 2'b10 Admit Untagged frames 2'b11 Reserved	0x0
	2[8:0]		R/W	VLAN_INGRESS_FILTER[8:0] VLAN Ingress Filter associated with each port If ingress filter for a given port is set, frame shall discard on that port whose VLAN classification does not include that port in it member set.	0x1FF

6.14.3 VLAN Egress Rule

PHY	MII	ROM	R/W	Description	Default
22	3[8:0]		R/W	KEEP_TAG[8:0] (QinQ register) Keep VLAN Tag Header 0: Disable 1: Keep VLAN tag header from frame. If frames transmission on a egress port tags frame, the frame may contain two tag headers	0x000

PHY	MII	ROM	R/W	Description	Default
	4[8:0]		R/W	IGMP_IGNORE_MEMBER[5:0] IGMP Ignore member set Ignore member set for frame with DMAC inside 01-00-5e-xx-xx-xx	0x000

6.14.4 Default VLAN Information

PHY	MII	ROM	R/W	Description	Default
22	5[15:0]		R/W	TPID_VALUE[15:0] 802.1Q Tag Protocol Type	0x8100

PHY	MII	ROM	R/W	Description	Default
22	6[15:0]		R/W	VLAN_INFO_0. Port 0 default VLAN information value (PVID_0)	0x0001
	7[15:0]		R/W	VLAN_INFO_1. Port 1 default VLAN information value (PVID_1)	0x0001
	8[15:0]		R/W	VLAN_INFO_2. Port 2 default VLAN information value (PVID_2)	0x0001
	9[15:0]		R/W	VLAN_INFO_3. Port 3 default VLAN information value (PVID_3)	0x0001
	10[15:0]		R/W	VLAN_INFO_4. Port 4 default VLAN information value (PVID_4)	0x0001
	11[15:0]		R/W	VLAN_INFO_5. Port 5 default VLAN information value (PVID_5)	0x0001
	12[15:0]		R/W	VLAN_INFO_6. Port 6 default VLAN information value (PVID_6)	0x0001
	13[15:0]		R/W	VLAN_INFO_7. Port 7 default VLAN information value (PVID_7)	0x0001
	14[15:0]		R/W	VLAN_INFO_8. Port 8 default VLAN information value (PVID_8)	0x0001

6.14.5 VLAN Entry

PHY	MII	ROM	R/W	Description	Default
22	15[15:0]		R/W	VLAN_VALID[15:0] VALN filter is valid. The VALN filter entry X is valid associated with the VID_X.	0x0000

6.14.6 Port-Based VLAN – Forward Mask

PHY	MII	ROM	R/W	Description				Default
22	16[8:0]		R/W	VLAN_MEMBER_SET_0 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x101	0x101	0x1ff	0x1ff	
	17[8:0]		R/W	VLAN_MEMBER_SET_1 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x102	0x102	0x1ff	0x1ff	
	18[8:0]		R/W	VLAN_MEMBER_SET_2 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x104	0x104	0x1ff	0x1ff	
	19[8:0]		R/W	VLAN_MEMBER_SET_3 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x108	0x108	0x1ff	0x1ff	
	20[8:0]		R/W	VLAN_MEMBER_SET_4 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x110	0x110	0x1ff	0x1ff	
	21[8:0]		R/W	VLAN_MEMBER_SET_5 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x120	0x120	0x1ff	0x1ff	
	22[8:0]		R/W	VLAN_MEMBER_SET_6 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x140	0x140	0x1ff	0x1ff	

PHY	MII	ROM	R/W	Description				Default
	23[8:0]		R/W	VLAN_MEMBER_SET_7 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x180	0x180	0x1ff	0x1ff	
	24[8:0]		R/W	VLAN_MEMBER_SET_8 Bits [8:0] correspond to port[8:0]				*
				IP179N	IP179H	IP179N	IP179H	
				PIN80=0	PIN120=0	PIN80=1	PIN120=1	
				0x1ff	0x1ff	0x1ff	0x1ff	

6.14.7 Port-Based VLAN – Add Tag Mask

PHY	MII	ROM	R/W	Description	Default
23	0[8:0]		R/W	VLAN_ADD_MASK_0 Bits [8:0] correspond to port[8:0]	0x000
	1[8:0]		R/W	VLAN_ADD_MASK_1 Bits [8:0] correspond to port[8:0]	0x000
	2[8:0]		R/W	VLAN_ADD_MASK_2 Bits [8:0] correspond to port[8:0]	0x000
	3[8:0]		R/W	VLAN_ADD_MASK_3 Bits [8:0] correspond to port[8:0]	0x000
	4[8:0]		R/W	VLAN_ADD_MASK_4 Bits [8:0] correspond to port[8:0]	0x000
	5[8:0]		R/W	VLAN_ADD_MASK_5 Bits [8:0] correspond to port[8:0]	0x000
	6[8:0]		R/W	VLAN_ADD_MASK_6 Bits [8:0] correspond to port[8:0]	0x000
	7[8:0]		R/W	VLAN_ADD_MASK_7 Bits [8:0] correspond to port[8:0]	0x000
	8[8:0]		R/W	VLAN_ADD_MASK_8 Bits [8:0] correspond to port[8:0]	0x000

6.14.8 Port-Based VLAN – Remove Tag Mask

PHY	MII	ROM	R/W	Description	Default
23	16[8:0]		R/W	VLAN_REMOVE_MASK_0 Bits [8:0] correspond to port[8:0]	0x000
	17[8:0]		R/W	VLAN_REMOVE_MASK_1 Bits [8:0] correspond to port[8:0]	0x000
	18[8:0]		R/W	VLAN_REMOVE_MASK_2 Bits [8:0] correspond to port[8:0]	0x000
	19[8:0]		R/W	VLAN_REMOVE_MASK_3 Bits [8:0] correspond to port[8:0]	0x000
	20[8:0]		R/W	VLAN_REMOVE_MASK_4 Bits [8:0] correspond to port[8:0]	0x000
	21[8:0]		R/W	VLAN_REMOVE_MASK_5 Bits [8:0] correspond to port[8:0]	0x000
	22[8:0]		R/W	VLAN_REMOVE_MASK_6 Bits [8:0] correspond to port[8:0]	0x000
	23[8:0]		R/W	VLAN_REMOVE_MASK_7 Bits [8:0] correspond to port[8:0]	0x000
	24[8:0]		R/W	VLAN_REMOVE_MASK_8 Bits [8:0] correspond to port[8:0]	0x000

6.14.9 Tagged-Based VLAN – Identifier Register

PHY	MII	ROM	R/W	Description	Default
24	0[15:12]		R/W	FID_0 VLAN field identifier associated with VALN 0.	0x0
	0[11:0]		R/W	VID_0 VLAN identifier associated with VALN 0.	0x000
	1[15:12]		R/W	FID_1 VLAN field identifier associated with VALN 1.	0x0
	1[11:0]		R/W	VID_1 VLAN identifier associated with VALN 1.	0x000
	2[15:12]		R/W	FID_2 VLAN field identifier associated with VALN 2.	0x0
	2[11:0]		R/W	VID_2 VLAN identifier associated with VALN 2.	0x000
	3[15:12]		R/W	FID_3 VLAN field identifier associated with VALN 3.	0x0
	3[11:0]		R/W	VID_3 VLAN identifier associated with VALN 3.	0x000
	4[15:12]		R/W	FID_4 VLAN field identifier associated with VALN 4.	0x0
	4[11:0]		R/W	VID_4 VLAN identifier associated with VALN 4.	0x000
	5[15:12]		R/W	FID_5 VLAN field identifier associated with VALN 5.	0x0
	5[11:0]		R/W	VID_5 VLAN identifier associated with VALN 5.	0x000
	6[15:12]		R/W	FID_6 VLAN field identifier associated with VALN 6.	0x0
	6[11:0]		R/W	VID_6 VLAN identifier associated with VALN 6.	0x000
	7[15:12]		R/W	FID_7 VLAN field identifier associated with VALN 7.	0x0
	7[11:0]		R/W	VID_7 VLAN identifier associated with VALN 7.	0x000
	8[15:12]		R/W	FID_8 VLAN field identifier associated with VALN 8.	0x0
	8[11:0]		R/W	VID_8 VLAN identifier associated with VALN 8.	0x000
	9[15:12]		R/W	FID_9 VLAN field identifier associated with VALN 9.	0x0
	9[11:0]		R/W	VID_9 VLAN identifier associated with VALN 9.	0x000
	10[15:12]		R/W	FID_A VLAN field identifier associated with VALN A.	0x0
	10[11:0]		R/W	VID_A VLAN identifier associated with VALN A.	0x000

PHY	MII	ROM	R/W	Description	Default
	11[15:12]		R/W	FID_B VLAN field identifier associated with VALN B.	0x0
	11[11:0]		R/W	VID_B VLAN identifier associated with VALN B.	0x000
	12[15:12]		R/W	FID_C VLAN field identifier associated with VALN C.	0x0
	12[11:0]		R/W	VID_C VLAN identifier associated with VALN C.	0x000
	13[15:12]		R/W	FID_D VLAN field identifier associated with VALN D.	0x0
	13[11:0]		R/W	VID_D VLAN identifier associated with VALN D.	0x000
	14[15:12]		R/W	FID_E VLAN field identifier associated with VALN E.	0x0
	14[11:0]		R/W	VID_E VLAN identifier associated with VALN E.	0x000
	15[15:12]		R/W	FID_F VLAN field identifier associated with VALN F.	0x0
	15[11:0]		R/W	VID_F VLAN identifier associated with VALN F.	0x000

6.14.10 Tagged-Based VLAN – Add Tag Control Register

PHY	MII	ROM	R/W	Description		Default
24	16[8:0]		R/W	ADD_TAG_0 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_0.		0x000
				Bit 0	1: port 0 adds a VLAN tag to each outgoing packet. 0: port 0 doesn't add a VLAN tag.	
				Bit 1	1: port 1 adds a VLAN tag to each outgoing packet. 0: port 1 doesn't add a VLAN tag.	
				Bit 2	1: port 2 adds a VLAN tag to each outgoing packet. 0: port 2 doesn't add a VLAN tag.	
				Bit 3	1: port 3 adds a VLAN tag to each outgoing packet. 0: port 3 doesn't add a VLAN tag.	
				Bit 4	1: port 4 adds a VLAN tag to each outgoing packet. 0: port 4 doesn't add a VLAN tag.	
				Bit 5	1: port 5 adds a VLAN tag to each outgoing packet. 0: port 5 doesn't add a VLAN tag.	
				Bit 6	1: port 6 adds a VLAN tag to each outgoing packet. 0: port 6 doesn't add a VLAN tag.	
				Bit 7	1: port 7 adds a VLAN tag to each outgoing packet. 0: port 7 doesn't add a VLAN tag.	
				Bit 8	1: port 8 adds a VLAN tag to each outgoing packet. 0: port 8 doesn't add a VLAN tag.	

PHY	MII	ROM	R/W	Description	Default
	17[8:0]		R/W	ADD_TAG_1 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_1.	0x000
	18[8:0]		R/W	ADD_TAG_2 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_2.	0x000
	19[8:0]		R/W	ADD_TAG_3 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_3.	0x000
	20[8:0]		R/W	ADD_TAG_4 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_4.	0x000
	21[8:0]		R/W	ADD_TAG_5 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_5.	0x000
	22[8:0]		R/W	ADD_TAG_6 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_6.	0x000
	23[8:0]		R/W	ADD_TAG_7 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_7.	0x000
	24[8:0]		R/W	ADD_TAG_8 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_8.	0x000
	25[8:0]		R/W	ADD_TAG_9 Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_9.	0x000
	26[8:0]		R/W	ADD_TAG_A Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_A.	0x000
	27[8:0]		R/W	ADD_TAG_B Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_B.	0x000
	28[8:0]		R/W	ADD_TAG_C Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_C.	0x000

PHY	MII	ROM	R/W	Description	Default
	29[8:0]		R/W	ADD_TAG_D Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_D.	0x000
	30[8:0]		R/W	ADD_TAG_E Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_E.	0x000
	31[8:0]		R/W	ADD_TAG_F Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_F.	0x000

6.14.11 Tagged-Based VLAN – Remove Tag Control Register

PHY	MII	ROM	R/W	Description		Default
25	0[8:0]		R/W	REMOVE_TAG_0 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_0.		0x000
				Bit 0	1: port 0 removes the VLAN tag of each outgoing packet. 0: port 0 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 1	1: port 1 removes the VLAN tag of each outgoing packet. 0: port 1 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 2	1: port 2 removes the VLAN tag of each outgoing packet. 0: port 2 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 3	1: port 3 removes the VLAN tag of each outgoing packet. 0: port 3 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 4	1: port 4 removes the VLAN tag of each outgoing packet. 0: port 4 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 5	1: port 5 removes the VLAN tag of each outgoing packet. 0: port 5 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 6	1: port 6 removes the VLAN tag of each outgoing packet. 0: port 6 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 7	1: port 7 removes the VLAN tag of each outgoing packet. 0: port 7 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 8	1: port 8 removes the VLAN tag of each outgoing packet. 0: port 8 doesn't remove the VLAN tag of each outgoing packet.	
	1[8:0]		R/W	REMOVE_TAG_1 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_1.		0x000
	2[8:0]		R/W	REMOVE_TAG_2 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_2.		0x000
	3[8:0]		R/W	REMOVE_TAG_3 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_3.		0x000

PHY	MII	ROM	R/W	Description	Default
	4[8:0]		R/W	REMOVE_TAG_4 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_4.	0x000
	5[8:0]		R/W	REMOVE_TAG_5 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_5.	0x000
	6[8:0]		R/W	REMOVE_TAG_6 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_6.	0x000
	7[8:0]		R/W	REMOVE_TAG_7 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_7.	0x000
	8[8:0]		R/W	REMOVE_TAG_8 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_8.	0x000
	9[8:0]		R/W	REMOVE_TAG_9 Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_9.	0x000
	10[8:0]		R/W	REMOVE_TAG_A Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_A.	0x000
	11[8:0]		R/W	REMOVE_TAG_B Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_B.	0x000
	12[8:0]		R/W	REMOVE_TAG_C Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_C.	0x000
	13[8:0]		R/W	REMOVE_TAG_D Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_D.	0x000
	14[8:0]		R/W	REMOVE_TAG_E Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_E.	0x000
	15[8:0]		R/W	REMOVE_TAG_F Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_F.	0x000

6.14.12 Tagged-Based VLAN – VLAN Member Register

PHY	MII	ROM	R/W	Description	Default
25	16[8:0]		R/W	VLAN_MEMBER_0 VLAN member port VLAN member port associated with the VID_0.	0x1FF
	17[8:0]		R/W	VLAN_MEMBER_1 VLAN member port VLAN member port associated with the VID_1.	0x1FF
	18[8:0]		R/W	VLAN_MEMBER_2 VLAN member port VLAN member port associated with the VID_2.	0x1FF
	19[8:0]		R/W	VLAN_MEMBER_3 VLAN member port VLAN member port associated with the VID_3.	0x1FF
	20[8:0]		R/W	VLAN_MEMBER_4 VLAN member port VLAN member port associated with the VID_4.	0x1FF
	21[8:0]		R/W	VLAN_MEMBER_5 VLAN member port VLAN member port associated with the VID_5.	0x1FF
	22[8:0]		R/W	VLAN_MEMBER_6 VLAN member port VLAN member port associated with the VID_6.	0x1FF
	23[8:0]		R/W	VLAN_MEMBER_7 VLAN member port VLAN member port associated with the VID_7.	0x1FF
	24[8:0]		R/W	VLAN_MEMBER_8 VLAN member port VLAN member port associated with the VID_8.	0x1FF
	25[8:0]		R/W	VLAN_MEMBER_9 VLAN member port VLAN member port associated with the VID_9.	0x1FF
	26[8:0]		R/W	VLAN_MEMBER_A VLAN member port VLAN member port associated with the VID_A.	0x1FF
	27[8:0]		R/W	VLAN_MEMBER_B VLAN member port VLAN member port associated with the VID_B.	0x1FF
	28[8:0]		R/W	VLAN_MEMBER_C VLAN member port VLAN member port associated with the VID_C.	0x1FF
	29[8:0]		R/W	VLAN_MEMBER_D VLAN member port VLAN member port associated with the VID_D.	0x1FF
	30[8:0]		R/W	VLAN_MEMBER_E VLAN member port VLAN member port associated with the VID_E.	0x1FF

PHY	MII	ROM	R/W	Description	Default
	31[8:0]		R/W	VLAN_MEMBER_F VLAN member port VLAN member port associated with the VID_F.	0x1FF

6.15 EEE Registers

PHY	MII	ROM	R/W	Description				Default
22	25[15]		R/W	EEE_DIS EEE Disable				*
				IP179N	IP179H	IP179N	IP179H	
				PIN83=0	PIN123=0	PIN83=1	PIN123=1	
				Enable	Enable	Disable	Disable	
	25[8:0]		R/W	EEE_EN				0x1FF
	26[15:14]		R/W	SLEEP_TIME_UNIT 0x0: 1s 0x1: 1ms 0x2: 1us				0x2
	26[13:12]			WAKE_TIME_UNIT 0x0: 1s 0x1: 1ms 0x2: 1us				0x2
	26[11:0]		R/W	SLEEP_TIME The time to sleep = SLEEP_TIME_UNIT * SLEEP_TIME				0xF
	27[15:8]		R/W	WAKE_TIME_P1				0x23
	27[7:0]		R/W	WAKE_TIME_P0 Wake Up Time for Port 0 The time to wake = WAKE_TIME_UNIT_P0 * WAKE_TIME_P0 The time is between when switch de-assert LPI and when it can send data.				0x23
	28[15:8]		R/W	WAKE_TIME_P3				0x23
	28[7:0]		R/W	WAKE_TIME_P2				0x23
	29[15:8]		R/W	WAKE_TIME_P5				0x23
	29[7:0]		R/W	WAKE_TIME_P4				0x23
	30[15:8]		R/W	WAKE_TIME_P7				0x23
	30[7:0]		R/W	WAKE_TIME_P6				0x23
	31[7:0]		R/W	WAKE_TIME_P8				0x23

6.16 RGMII Driving Capability Registers

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="4">23</td><td>11[14:12]</td><td></td><td>R/W</td><td>RGMII_TXDATA_DRIVE

RGMII TXD[3:0] driving capability selection
<table>
<tr><th>Drive[2:0]</th><th>3.3V</th><th>2.5V</th><th>1.8V</th></tr>
<tr><td>000</td><td>6.01 mA</td><td>4.71 mA</td><td>3.175 mA</td></tr>
<tr><td>001</td><td>12.02 mA</td><td>9.43 mA</td><td>6.35 mA</td></tr>
<tr><td>010</td><td>18.03 mA</td><td>14.15 mA</td><td>9.525 mA</td></tr>
<tr><td>011</td><td>24.03 mA</td><td>18.87 mA</td><td>12.7 mA</td></tr>
<tr><td>100</td><td>30.04 mA</td><td>23.58 mA</td><td>15.87 mA</td></tr>
<tr><td>101</td><td>36.05 mA</td><td>28.3 mA</td><td>19.05 mA</td></tr>
<tr><td>110</td><td>39.06 mA</td><td>30.66 mA</td><td>20.64 mA</td></tr>
<tr><td>111</td><td>42.06 mA</td><td>33.02 mA</td><td>22.22 mA</td></tr>
</table></td><td>0x3</td></tr>
<tr><td>11[10:8]</td><td></td><td>R/W</td><td>RGMII_TXCLK_DRIVE

RGMII TX_CLK driving capability selection
<table>
<tr><th>Drive[2:0]</th><th>3.3V</th><th>2.5V</th><th>1.8V</th></tr>
<tr><td>000</td><td>6.01 mA</td><td>4.71 mA</td><td>3.175 mA</td></tr>
<tr><td>001</td><td>12.02 mA</td><td>9.43 mA</td><td>6.35 mA</td></tr>
<tr><td>010</td><td>18.03 mA</td><td>14.15 mA</td><td>9.525 mA</td></tr>
<tr><td>011</td><td>24.03 mA</td><td>18.87 mA</td><td>12.7 mA</td></tr>
<tr><td>100</td><td>30.04 mA</td><td>23.58 mA</td><td>15.87 mA</td></tr>
<tr><td>101</td><td>36.05 mA</td><td>28.3 mA</td><td>19.05 mA</td></tr>
<tr><td>110</td><td>39.06 mA</td><td>30.66 mA</td><td>20.64 mA</td></tr>
<tr><td>111</td><td>42.06 mA</td><td>33.02 mA</td><td>22.22 mA</td></tr>
</table></td><td>0x3</td></tr>
<tr><td>11[6:4]</td><td></td><td>R/W</td><td>RGMII_RXDATA_DRIVE

RGMII RXD[3:0] driving capability selection
<table>
<tr><th>Drive[2:0]</th><th>3.3V</th><th>2.5V</th><th>1.8V</th></tr>
<tr><td>000</td><td>6.01 mA</td><td>4.71 mA</td><td>3.175 mA</td></tr>
<tr><td>001</td><td>12.02 mA</td><td>9.43 mA</td><td>6.35 mA</td></tr>
<tr><td>010</td><td>18.03 mA</td><td>14.15 mA</td><td>9.525 mA</td></tr>
<tr><td>011</td><td>24.03 mA</td><td>18.87 mA</td><td>12.7 mA</td></tr>
<tr><td>100</td><td>30.04 mA</td><td>23.58 mA</td><td>15.87 mA</td></tr>
<tr><td>101</td><td>36.05 mA</td><td>28.3 mA</td><td>19.05 mA</td></tr>
<tr><td>110</td><td>39.06 mA</td><td>30.66 mA</td><td>20.64 mA</td></tr>
<tr><td>111</td><td>42.06 mA</td><td>33.02 mA</td><td>22.22 mA</td></tr>
</table></td><td>0x3</td></tr>
<tr><td>11[2:0]</td><td></td><td>R/W</td><td>RGMII_RXCLK_DRIVE

RGMII RX_CLK driving capability selection
<table>
<tr><th>Drive[2:0]</th><th>3.3V</th><th>2.5V</th><th>1.8V</th></tr>
<tr><td>000</td><td>6.01 mA</td><td>4.71 mA</td><td>3.175 mA</td></tr>
<tr><td>001</td><td>12.02 mA</td><td>9.43 mA</td><td>6.35 mA</td></tr>
<tr><td>010</td><td>18.03 mA</td><td>14.15 mA</td><td>9.525 mA</td></tr>
<tr><td>011</td><td>24.03 mA</td><td>18.87 mA</td><td>12.7 mA</td></tr>
<tr><td>100</td><td>30.04 mA</td><td>23.58 mA</td><td>15.87 mA</td></tr>
<tr><td>101</td><td>36.05 mA</td><td>28.3 mA</td><td>19.05 mA</td></tr>
<tr><td>110</td><td>39.06 mA</td><td>30.66 mA</td><td>20.64 mA</td></tr>
<tr><td>111</td><td>42.06 mA</td><td>33.02 mA</td><td>22.22 mA</td></tr>
</table></td><td>0x3</td></tr>
</table>

PHY	MII	ROM	R/W	Description	Default
	12[15:0]			Reserved	
	13[15:0]			Reserved	

6.17 Miscellaneous

PHY	MII	ROM	R/W	Description	Default
23	14[15:1]			Reserved	
	14[0]		R/W	IGMP_EN Setting IGMP_EN=1 will auto-configure register 21.0-3, to enable hardware IGMP function.	0x0

6.18 PHY Address

PHY	MII	ROM	R/W	Description	Default
23	25[15:12]		R/W	PHY_Address_3	0x0b
	25[11:8]		R/W	PHY_Address_2	0x0a
	25[7:4]		R/W	PHY_Address_1	0x09
	25[3:0]		R/W	PHY_Address_0	0x08
	26[15:12]		R/W	PHY_Address_7	0x0f
	26[11:8]		R/W	PHY_Address_6	0x0e
	26[7:4]		R/W	PHY_Address_5	0x0d
	26[3:0]		R/W	PHY_Address_4	0x0c
	27[3:0]		R/W	PHY_Address_8	0x01

6.19 RGMII/MII/RMII Control Register

6.19.1 RGMII/MII/RMII Control Register 0

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="11">23</td><td>29[15]</td><td></td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>29[14]</td><td></td><td>R/W</td><td>TX_INV

Inverted TX_CLK</td><td>0x0</td></tr>
<tr><td>29[13:12]</td><td></td><td>R/W</td><td>TX_DLY

TX_CLK delay selection
0x0: delay 0ns
0x1: delay 1ns
0x2: delay 2ns
0x3: delay 3ns

IP179N PIN76=1 Default=0x2 | IP179H PIN115=1 Default=0x2 | IP179N PIN76=0 Default=0x0 | IP179H PIN115=0 Default=0x0</td><td>*</td></tr>
<tr><td>29[10]</td><td></td><td>R/W</td><td>RX_INV

Inverted RX_CLK</td><td>0x0</td></tr>
<tr><td>29[9:8]</td><td></td><td>R/W</td><td>RX_DLY

RX_CLK delay selection
0x0: delay 0ns
0x1: delay 1ns
0x2: delay 2ns
0x3: delay 3ns

IP179N PIN77=1 Default=0x2 | IP179H PIN116=1 Default=0x2 | IP179N PIN77=0 Default=0x0 | IP179H PIN116=0 Default=0x0</td><td>*</td></tr>
<tr><td>29[7]</td><td></td><td>R/W</td><td>MII0_MAC_MODE

1: MII0 works as a MAC and should be connected to an external PHY.
0: MII0 works as a PHY and should be connected to an external MAC device.

It is only valid in MII Mode</td><td>0x0</td></tr>
<tr><td>29[6]</td><td></td><td>R/W</td><td>FORCE_DUPLEX</td><td>0x1</td></tr>
<tr><td>29[5]</td><td></td><td>R/W</td><td>FORCE_TX_PAUSE</td><td>0x1</td></tr>
<tr><td>29[4]</td><td></td><td>R/W</td><td>FORCE_RX_PAUSE</td><td>0x1</td></tr>
</table>

PHY	MII	ROM	R/W	Description	Default
	29[3:2]		R/W	FORCE_SPEED 0x0: 10Mbps 0x1: 100Mbps 0x2: 1000Mbps If EXTMII_MODE=RGMII then FORCE_SPEED=0x2 If EXTMII_MODE=RMII/MII then FORCE_SPEED=0x1	*
	29[1:0]		R/W	EXTMII_MODE[1:0] 0x0: Disable (IP179N/H) 0x1: RMII (IP179N/H) 0x2: MII (IP179H) 0x3: RGMII (IP179H) Bits [1:0] correspond to IP179N pin84 & pin85 or IP179H pin 124 & pin125, respectively.	*

6.19.2 RGMII/MII/RMII Control Register 1

PHY	MII	ROM	R/W	Description	Default
23	30[15]		R/W	DISPLAY_STATUS Display Link Status	0x0
	30[14]			Reserved	
	30[13]		RO	STATUS_VALID	
	30[12]		RO	LINK_UP	
	30[11]		R/W	EEE_1000	0x1
	30[10]		R/W	EEE_100	0x1
	30[9]		R/W	PAUSE_ON	0x1
	30[8]		R/W	SP1000F 1000Mbps, Full Duplex	0x1
	30[7]		R/W	SP100F 100Mbps, Full Duplex	0x1
	30[6]		R/W	SP100H 100Mbps, Half Duplex	0x1
	30[5]		R/W	SP10F 10Mbps, Full Duplex	0x1
	30[4]		R/W	SP10H 10Mbps, Half Duplex	0x1
	30[3:0]		R/W	EXT_PHY_ADR	0x0

6.20 EEPROM Segment

PHY	MII	ROM	R/W	Description	Default
23	31[15:3]			Reserved	
	31[2]		RW	EE_SEGM	
	31[1]			Reserved	
	31[0]		RO	PIN_SEGM	

7 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25℃	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10℃ ~ +70℃
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100 μW typical
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year

8 Electrical Characteristics

8.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	-0.3V to 3.63V
Input Voltage	-0.3V to 3.63V
Output Voltage	-0.3V to 3.63V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta) (IP179N/H)	0°C to 70°C
IC Junction Temperature (Tj) (IP179N/H)	0°C to 125°C
Ambient Operating Temperature (Ta) (IP179N/HI)	-40°C to 85°C
IC Junction Temperature (Tj) (IP179N/HI)	-40°C to 125°C

8.2 DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Core Supply Voltage	DVDD	1.02	1.05	1.10	V	
Analog Low Supply Voltage	AV10	1.02	1.05	1.10	V	
LDO output voltage	V_{VREG_LDO}	1.02	1.05	1.10	V	
LDO input voltage	V_{PVDD_LDO}	3.15	3.3	3.45	V	
Analog High Supply Voltage	AV33	3.15	3.3	3.45	V	
I/O pad Supply Voltage	PVDD	3.15	3.3	3.45	V	
RGMII/MII/RMII Supply Voltage	PVDD_RG	3.15 2.38 1.75	3.3 2.5 1.8	3.45 2.62 1.89	V	RGMII 3.3/2.5/1.8V for IP179H RGMII 3.3/2.5V for IP179HI
MDC/MDIO Supply Voltage	PVDD_RGSMI	3.15 2.38	3.3 2.5	3.45 2.62	V	
Band Gap Supply Voltage	BGVCC	3.15	3.3	3.45	V	
PLL Supply Voltage	PLLVCC	3.15	3.3	3.45	V	
LDO output current	I_{LDO}	-	-	220	mA	
Fiber Rx common mode Voltage	VFRC	-	0.6* AV33	-	V	
Fiber Rx Differential mode Voltage	VFRD	0.4	-	-	V	
Power Consumption	P_{100MF}		1000		mW	All port link 100M Full active
	P_{10MF}		1080			All port link 10M Full active
	P_{IDLE}		750			All port unlink

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency	F		25		MHz	
Frequency Tolerance	F_T	-50		+50	PPM	

I/O Electrical Characteristics

Parameter	Sym	Min.	Max.	Unit	Conditions
Input Low Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	V_{IL}		0.39*PVDD 0.36*PVDD 0.4*PVDD	V	
Input High Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	V_{IH}	0.58*PVDD 0.58*PVDD 0.6*PVDD		V	
X1 Input Low Voltage	V_{ILosc}		0.2*PVDD	V	
X1 Input High Voltage	V_{IHosc}	0.8*PVDD		V	
Output Low Voltage	V_{OL}		0.1*PVDD	V	
Output High Voltage	V_{OH}	0.8*PVDD		V	
RESETB Input Low Voltage	V_{IL}		0.25*PVDD	V	
RESETB Input High Voltage	V_{IH}	0.75*PVDD		V	

RGMII Electrical Characteristics

Parameter	Sym	Min.	Max.	Unit	Conditions
Input Low Voltage PVDD_RG=1.8V PVDD_RG=2.5V PVDD_RG=3.3V	V_{IL}		0.65 1.00 1.32	V	RGMII 3.3/2.5/1.8V for IP179H RGMII 3.3/2.5V for IP179HI
Input High Voltage PVDD_RG=1.8V PVDD_RG=2.5V PVDD_RG=3.3V	V_{IH}	1.15 1.50 1.98		V	RGMII 3.3/2.5/1.8V for IP179H RGMII 3.3/2.5V for IP179HI

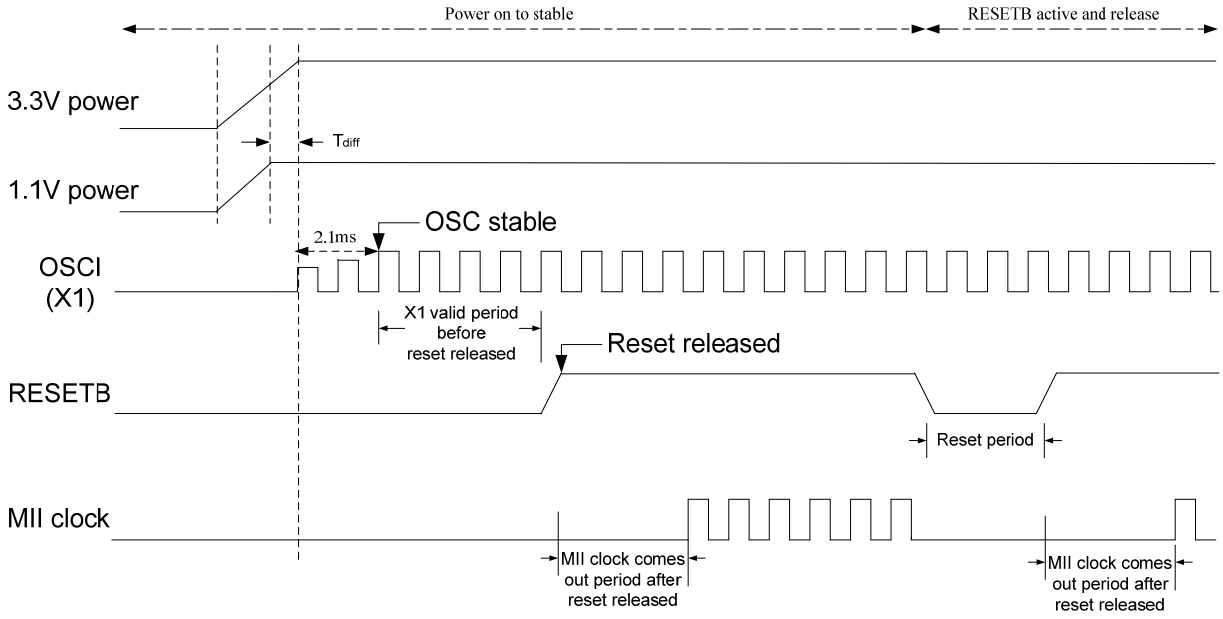
MDC/MDIO Electrical Characteristics

Parameter	Sym	Min.	Max.	Unit	Conditions
Input Low Voltage PVDD_RGSMI=2.5V PVDD_RGSMI=3.3V	V_{IL}		1.00 1.32	V	
Input High Voltage PVDD_RGSMI=2.5V PVDD_RGSMI=3.3V	V_{IH}	1.50 1.98		V	

8.3 AC Timing

8.3.1 Power On Sequence and Reset Timing

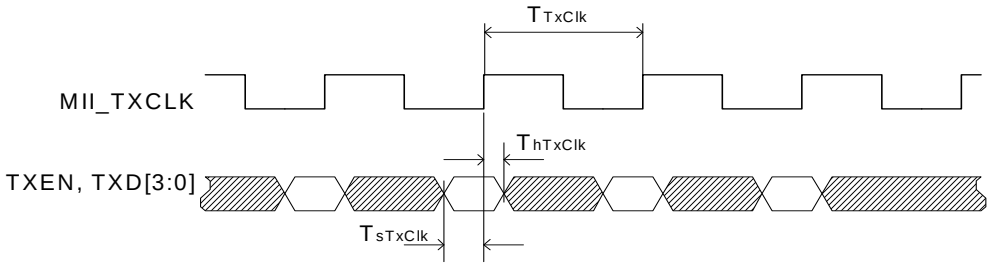
Description	Min.	Typ.	Max.	Unit
X1 valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
All power source ready before reset released	10	-	-	ms
Time difference between VCC3.3 and VCC1.1 (T_{diff})	-2	-	-	ms
MII clock comes out period after reset released	-	1	-	µs



8.3.2 PHY Mode MII Timing

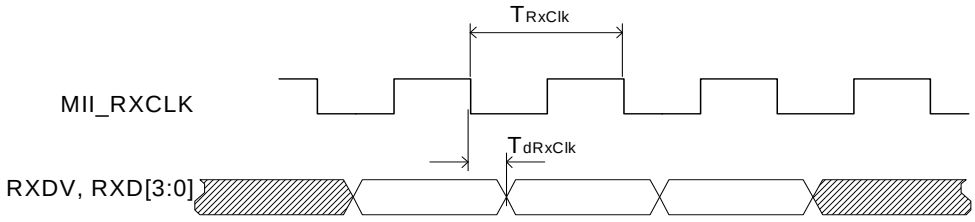
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN, TXD to MII_TXCLK setup time	10	-	-	ns
T_{hTxClk}	TXEN, TXD to MII_TXCLK hold time	10	-	-	ns



b. Transmit Timing Requirements

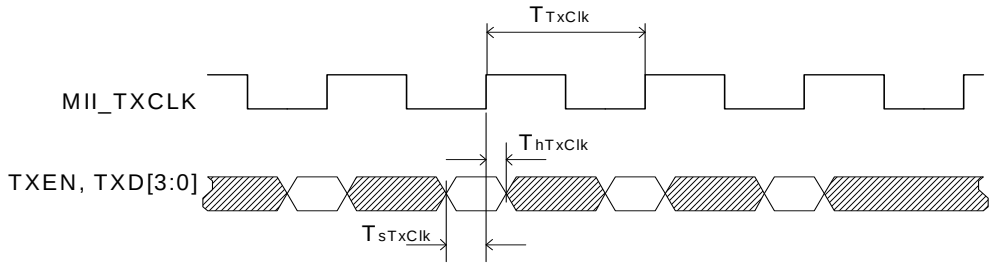
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII_RXCLK falling edge to RXDV, RXD	0	-	25	ns



8.3.3 MAC Mode MII Timing

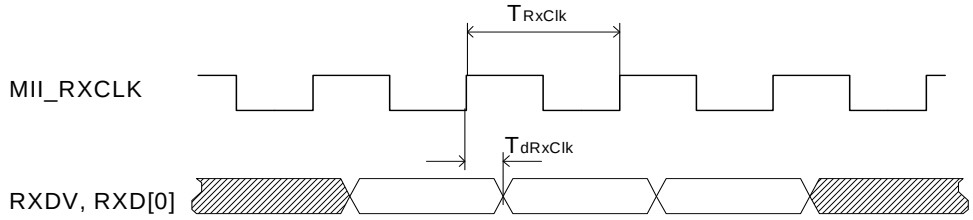
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN, TXD to MII_TXCLK setup time	10	-	-	ns
T_{hTxClk}	TXEN, TXD to MII_TXCLK hold time	10	-	-	ns



b. Transmit Timing Requirements

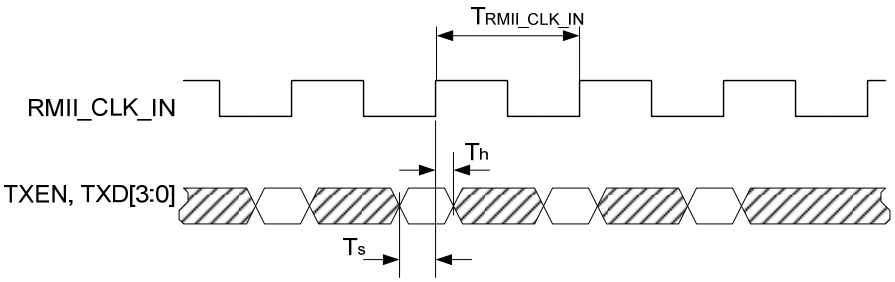
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII_RXCLK rising edge to RXDV, RXD	0	-	25	ns



8.3.4 RMII Timing

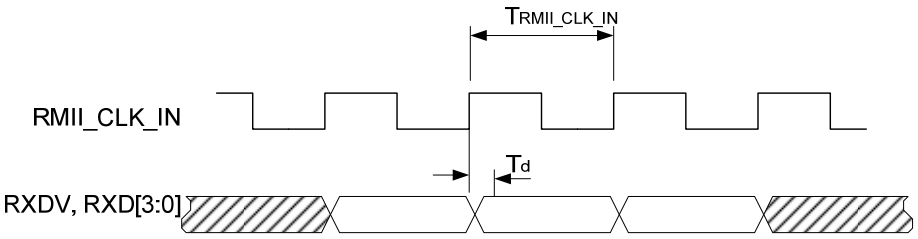
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RMII\_CLK\_IN}$	Receive clock period	-	20	-	ns
T_s	TXEN, TXD to RMII_CLK_IN setup time	4	-	-	ns
T_h	TXEN, TXD to RMII_CLK_IN hold time	2	-	-	ns



b. Transmit Timing

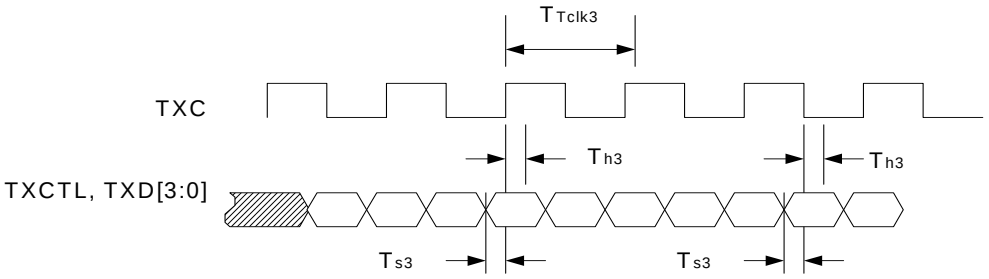
Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RMII\_CLK\_IN}$	Transmit clock period	-	20	-	ns
T_d	RMII_CLK_IN rising edge to RXDV, RXD	4.5	-	10	ns



8.3.5 RGMII Timing

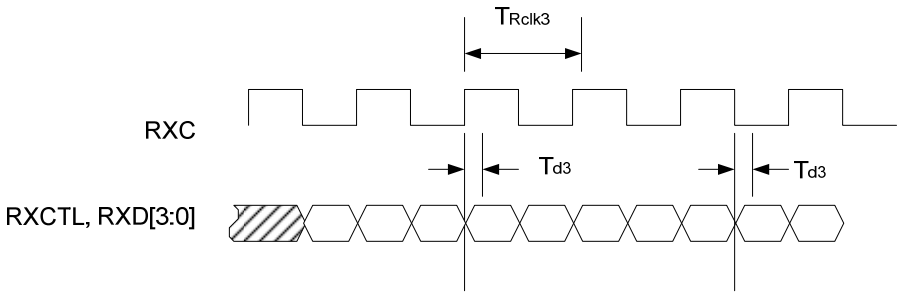
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tclk3}	Period of transmit clock in Giga mode	-	8	-	ns
T_{Tclk3}	Period of transmit clock in 100M mode	-	40	-	ns
T_{Tclk3}	Period of transmit clock in 10M mode	-	400	-	
T_{s3}	TXEN, TXD to TXC setup time	1	-	-	
T_{h3}	TXEN, TXD to TXC hold time	0.5	-	-	ns



b. Transmit Timing Requirements

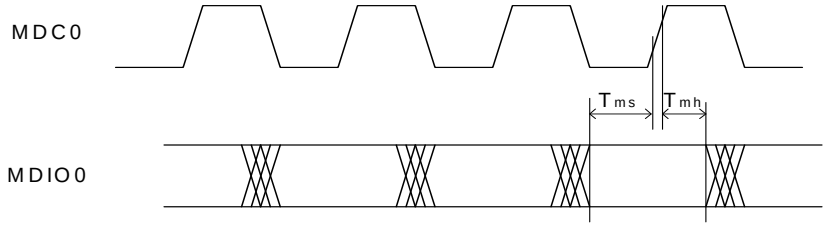
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk3}	Period of receive clock in Giga mode	-	8	-	ns
T_{Rclk3}	Period of receive clock in 100M mode	-	40	-	
T_{Rclk3}	Period of receive clock in 10M mode	-	400	-	
T_{d3}	RXC edge to RXCTL, RXD	-0.5	0	0.5	ns



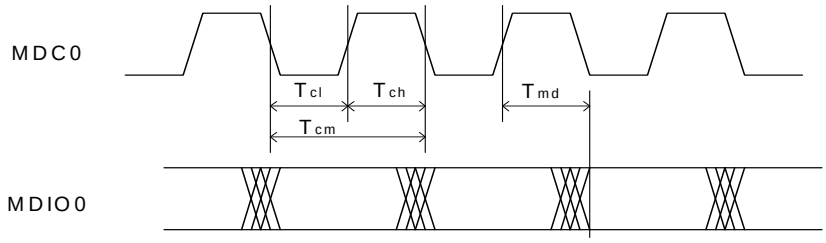
8.3.6 SMI Timing

a. MDC/MDIO Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time	-	200	-	ns
T_{cl}	MDC Low Time	-	200	-	ns
T_{cm}	MDC period	-	400	-	ns
T_{md}	MDIO output delay	13	-	31	ns
T_{ms}	MDIO setup time	10	-	-	ns
T_{mh}	MDIO hold time	10	-	-	ns



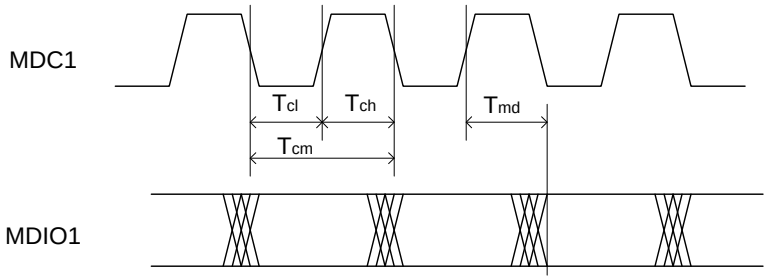
Write Cycle



Read Cycle

b. MDC1/ MDIO1 Timing Requirements - Access MDC1/MDIO1 via EEPROM

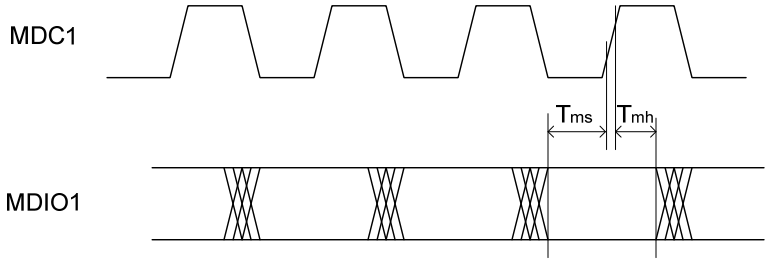
Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC1 High Time	-	160	-	ns
T_{cl}	MDC1 Low Time	-	160	-	ns
T_{cm}	MDC1 period	-	320	-	ns
T_{md}	MDIO1 output delay	10	-	40	ns



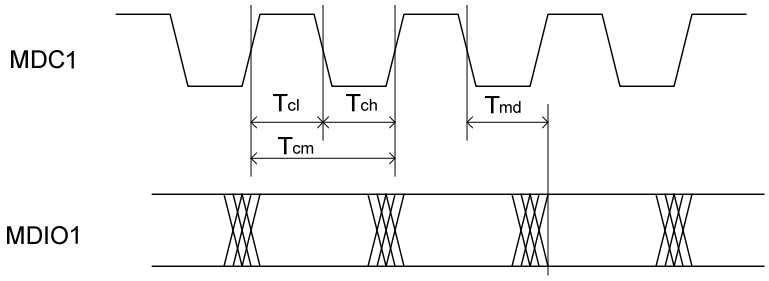
Write Cycle

c. MDC1/ MDIO1 Timing Requirements - MDC1/MDIO1 Polling External PHY

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC1 High Time	-	200	-	ns
T_{cl}	MDC1 Low Time	-	200	-	ns
T_{cm}	MDC1 period	-	400	-	ns
T_{md}	MDC1 falling edge to MDIO1 output delay	0.5	-	2	ns
T_{mh}	MDIO1 setup time	10	-	-	ns
T_{ms}	MDIO1 hold time	10	-	-	ns



Read Cycle

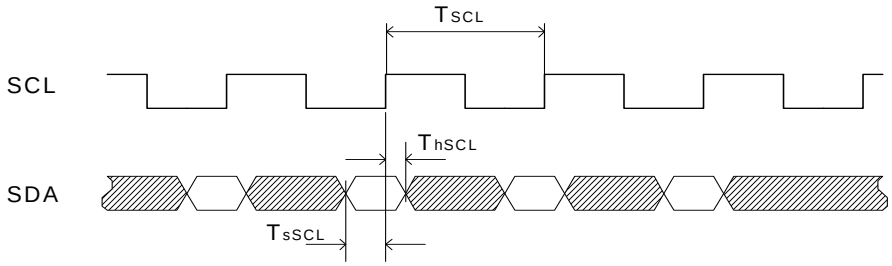


Write Cycle

8.3.7 EEPROM Timing

a.

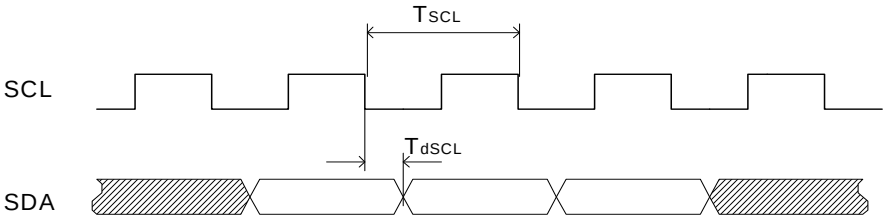
Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	10240	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns



Read data cycle

b.

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	10240	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	2600	ns



Comand cycle

8.4 Thermal Data

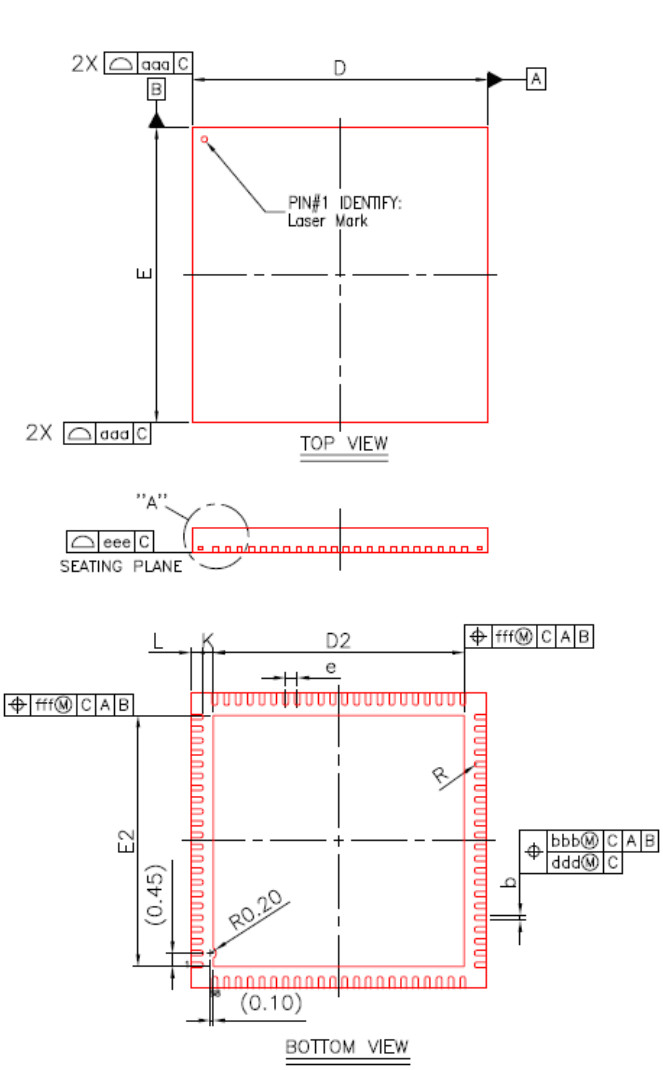
Part No.	Theta Ja	Theta Jc	Conditions	Units
IP179N	51.3	10.0	2 Layer PCB	^{o}C/W
IP179N	20.0	8.7	4 Layer PCB	^{o}C/W
IP179H	57.2	17.4	2 Layer PCB	^{o}C/W
IP179H	23.8	12.5	4 Layer PCB	^{o}C/W

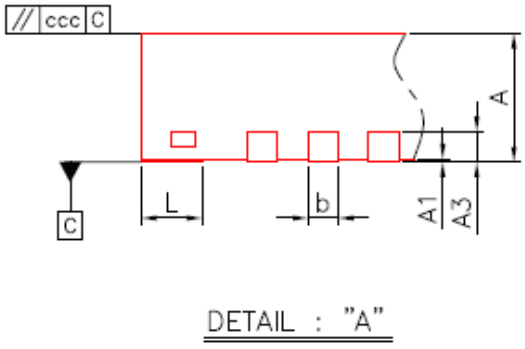
9 Order Information

Part No.	Package	Notice
IP179N	88-PIN QFN	0°C to 70°C
IP179NI	88-PIN QFN	-40°C to 85°C
IP179H	128-PIN LQFP	0°C to 70°C
IP179HI	128-PIN LQFP	-40°C to 85°C

10 Package Detail

QFN88 Outline Dimensions



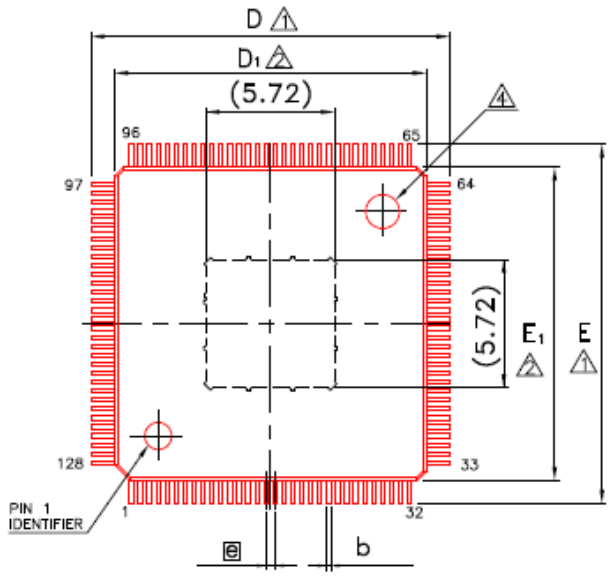


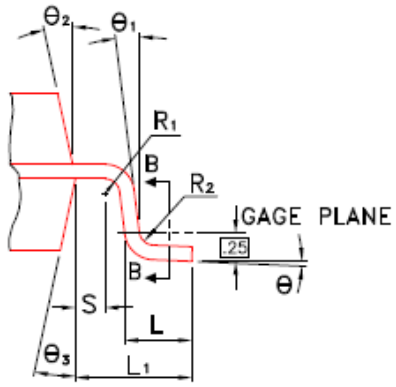
DETAIL : "A"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.13	0.18	0.23	0.005	0.007	0.009
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	8.40	8.50	8.60	0.331	0.335	0.339
E2	8.40	8.50	8.60	0.331	0.335	0.339
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.065	---	0.115	0.003	---	0.005
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

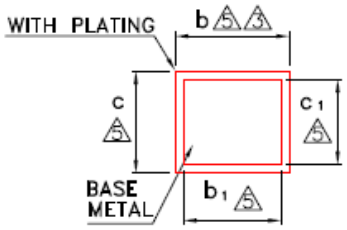
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

LQFP128 Outline Dimensions





DETAIL "A"



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

IC Plus Corp.

Headquarters
10F., No.47, Ln. 2, Sec. 2, Guangfu Rd.,
East Dist., Hsinchu City 30071, Taiwan (R.O.C.)
TEL：886-3-575-0275 FAX：886-3-575-0475
Website: www.icplus.com.tw

Sales Office
4F., No.106, Sec. 1, Xintai 5th Rd.,
Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
TEL：886-2-2696-1669 FAX：886-2-2696-2220