IP8008 4-Port IEEE 802.3bt PSE Controller for PoE Systems

Features

- IEEE 802.3af-2003 and 802.3at-2009 802.3bt -2018 type3, type4 compliant
- 4 ports for 4 pairs/2 channels per port
- 8 ports for 2 pairs/1 channel per port
- 8 independent power channels
- Configurations: 45W x 8 ports
  : or 90W x 4 ports
- Single DC power supply voltage input (44~57V)
- I^2C Bus to access up to 16 x IP8008 devices
- Cascade mode dynamic power management
- Continuous system monitoring for every channel
- Independent system parameters setting per channel
- Thermal monitoring and protection
- Auto-class discovery and power measurement
- Built-in 8 power FETs
- Built-in 8 pcs 0.1ohm sensing resistor, low power dissipation
- Built-in 3.3V regulators for internal system
- Built-in Power on Reset
- Built-in LEDs control for multi-port use
- Built-in EEPROM interface for dumb application
- Wide temperature range: -40℃~+85℃
- Package:
  56 Lead QFN 8mm x 8mm x 0.85mm,
  (0.5mm pitch, with EPAD)

Application

- 8 port PSE Switch
- 24 port PSE Switch

General Description

IP8008 is an 8-channel PSE (Power Sourcing Equipment) controller IC for PoE (Power over Ethernet) systems. It integrates power, analog and logic circuits into a single chip, and can be used for Midspans and Endpoint PSE applications.

IP8008 meets all IEEE 802.3bt-2018 single-signature PD/dual-signature PD requirements, such as multi-point resistor detection, connection check, five-event PD classification, Autoclass, and DC Disconnect. It also meets all IEEE 802.3af-2003, & 802.3at-2009 requirements, such as two-event classification and supply maximum 48W per port.

IP8008 comprises internal temperature monitoring and thermal protection to protect against junction overheating. The 3.3V regulator is built-in to support internal system. Multiple IP8008 can integrate to build a maximum 8 x 16 ports PSE 802.3at, or 4 x 16 ports PSE 802.3bt system, and I^2C bus uses to collect PD power status from each IP8008 to support global power managements.

Management switch host has options to communicate IP8008 via I^2C bus non-isolation for PSE management activities, or optocouplers can be implemented to provide electrical isolations between the host and IP8008 for signal communication.

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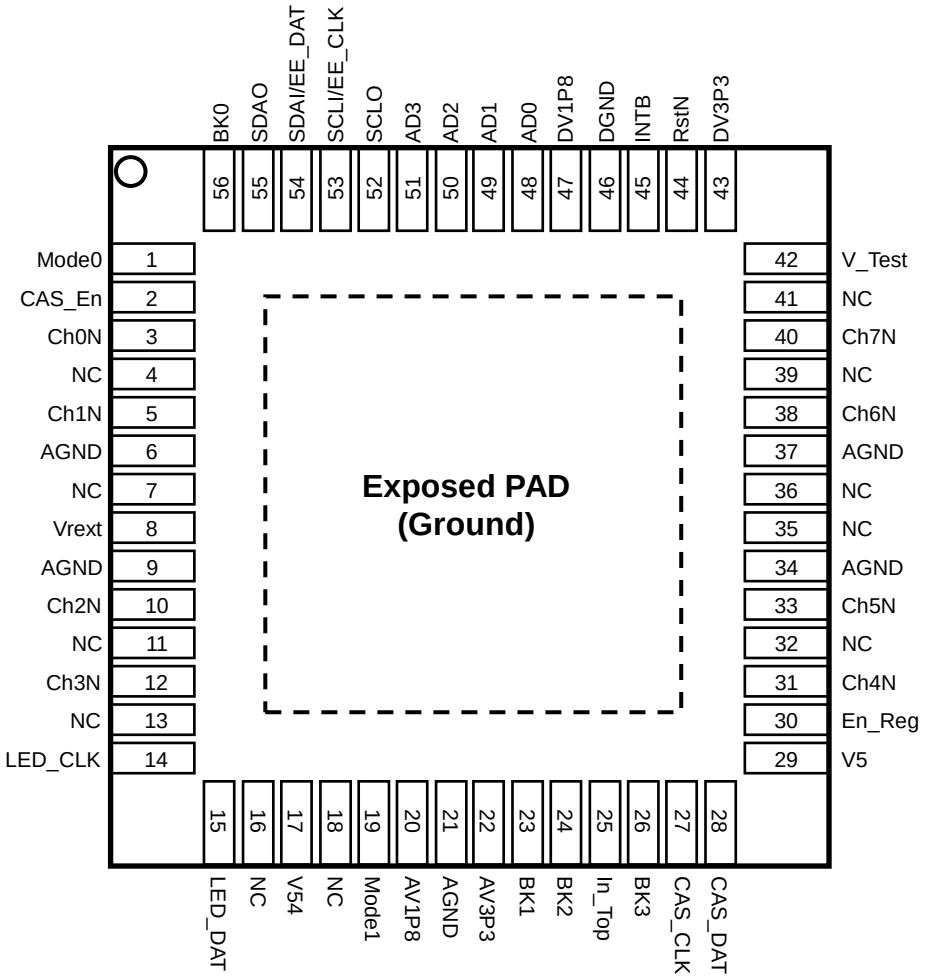
Revision History

Revision #	Date	Change Description
IP8008-DS-R01	2022/06	Initial release

1 Pin diagram

1.1 IP8008 Pin diagram (56-Lead QFN)

(8mm X 8mm X 0.85mm Top view)



Exposed pad is system GND, must be soldered to PCB ground plane

Figure 1 Pin Diagram

2 IP8008 application diagram

2.1 Dumb & Smart device application

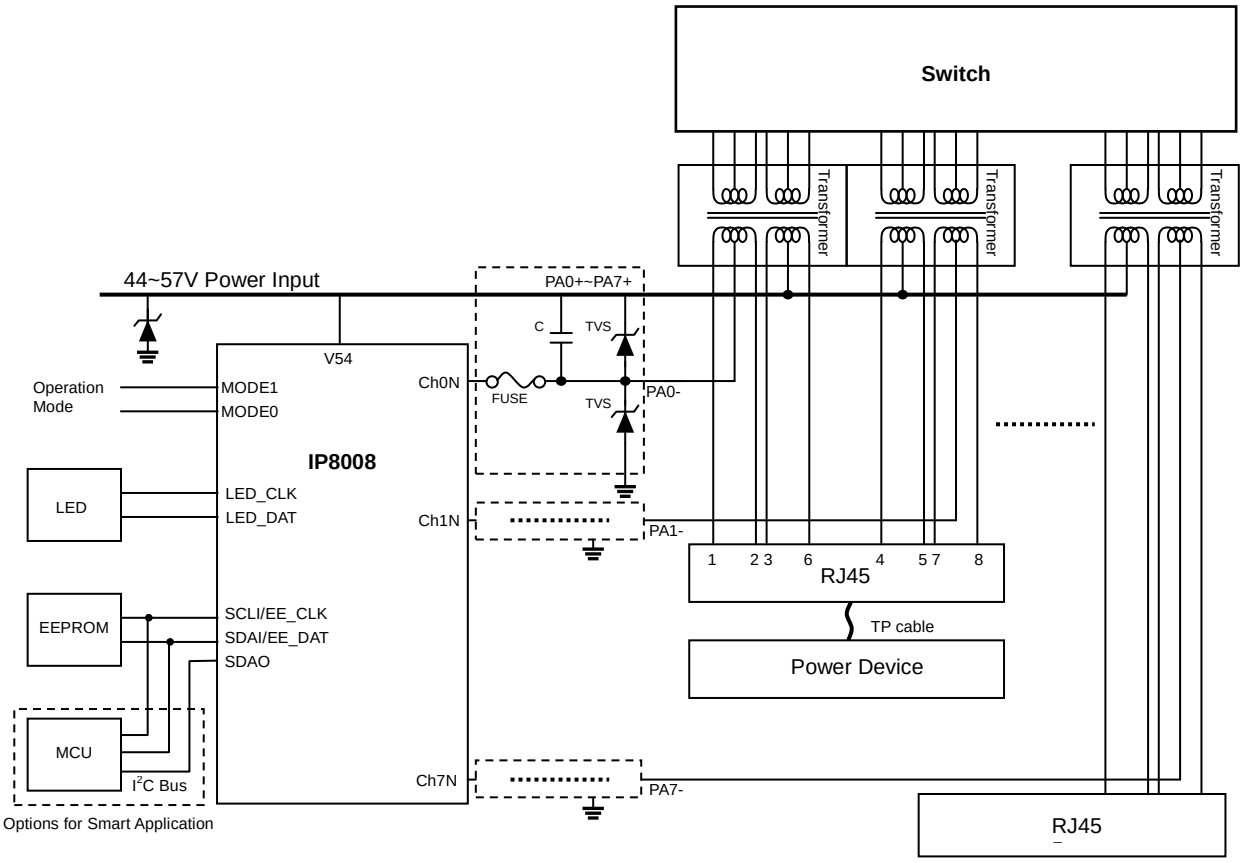


Figure 2 Application Diagram

Application	MCU	EEPROM	IP8008 Mode setting	Reference
Smart	V	X	Manual mode	Section 5.3
Dumb	X	V: update default value	Auto mode	Section 5.4
		X: use default value		

V: necessary; X: unnecessary

3 Block diagram

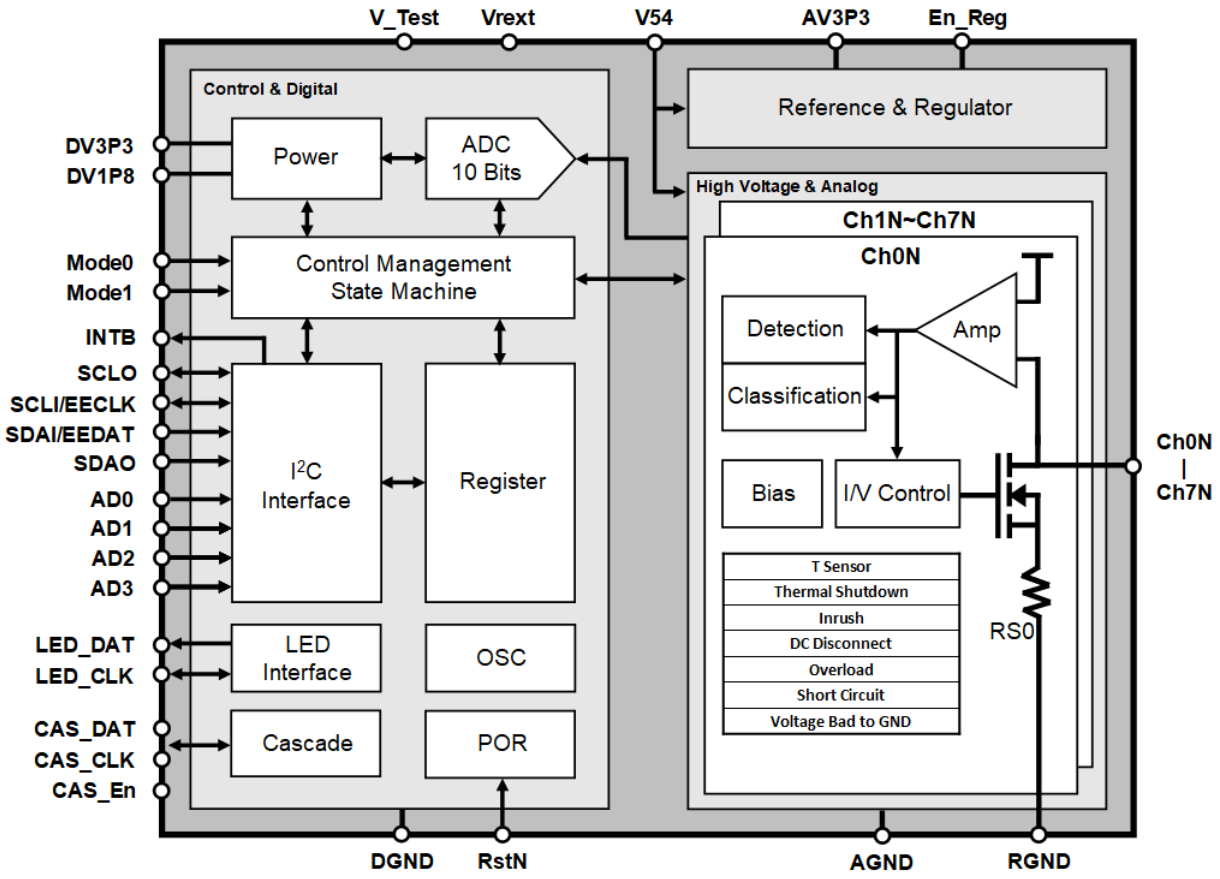


Figure 3 Block Diagram

3.1 Blocks Description

The blocks of IP8008 include global blocks for and per port blocks as below:

Global blocks for 8 ports:

- Reference & Regulator
- I²C Interface
- Registers
- Control Management & State Machine
- Power Management
- 10 Bits ADC
- POR & OSC

Per port blocks for individual port:

- Detection
- Classification
- I/V Control & Fold-back
- Amp
- DC Disconnect
- T sensor & Thermal Shutdown
- Bias
- Power MOSFET
- Autoclass
- Cascade

3.1.1 Global Blocks

- **Reference & Regulator:**

  The Reference & Regulator generates 1.8V, 3.3V and 5V power for internal use and 3.3V power also can supply typical current on V3P3 pin for internal system if En_Reg pin is NC(internal pull high 3.3V). If En_Reg is conncted to GND, the internal 3.3V regulator is disabled and V3P3 pin should be connected to an external 3.3V power source.

- **Registers**:

  The “Registers” provides the 8 bits data for Ilim, Icut programming registers, and all other needing registers per port.

- **Control Management & State Machine:**

  This block provides all the control procedures to perform PoE function. The “State Machine” implements as specified in the IEEE802.3af/at/bt.

- **Power Management:**

  The “Power Management” provides power management method to meet PD power requirement, or not to power PD if power is not enough.

- **10 Bits ADC:**

  The 10 Bits ADC used to convert analog signals into digital bus for Control Management, State Machine, and Power Management for request. ADC1 is for detection, connection check, and classification. ADC2 is for Inrush, Icut, Ilim, and power up.

- **POR & OSC:**

  The POR generates an internal power on reset signal when V54 is power on. The POR also monitors V3P3, DV3P3, V5, & V54 voltage level. If these voltages level are below specific thresholds, a reset signal generates and resets IP8008.

  The OSC is an internal oscillator to generate 8MHz clock for IP8008 timing source.

- **I^2C Interface:**

  A host (master) can communicates with multiple IP8008 (slave) via I^2C Interface (SCL/EE_CLK, SDAO, SDAI/EE_DAT) to collect PD power status to support global power managements and all control requirements.

3.1.2 Per Port Block

- **Detection:**

The IP8008 uses 4 steps detection method to discover PD. It shall accepted resistance as a valid "af/at/bt PD" between 19KΩ and 26.5KΩ, with a paralleled capacitance small than 0.15uF.

It shall rejects resistance with paralleled capacitance as an invalid "af/at/bt BT PD" smaller than 15KΩ, larger than 33KΩ, or capacitance larger than 10uF.

The specification is as specified in the IEEE802.3af/at/bt.

- **Classification:**

The "Classification" is to distinguish the requested power of PD as specified in the IEEE802.3 af/at/bt.

In IEEE 802.3af, classification is 1-event method.
In IEEE 802.3at, classification is 2-event method.
In IEEE 802.3bt, classification is 5-event method.

- **I/V Control:**

The "I/V Control" is to control the slew rate during "detection, classification, inrush, short circuit, power off … and so on", as specified in IEEE802.3af/at/bt.

When short circuit event occurs, the "I/V control" will reduce the port current instantaneously to protect the power MOSFET from damages.

- **Amp:**

The "AMP" is used to convert the differential voltage between V54 and ChNx into single end voltage. This voltage will be fed into the "Detection, Classification, I/V Control" blocks to perform the IEEE802.3af/at/bt specifications.

- **DC Disconnect:**

The IP8008 supports DC Disconnect function according to IEEE 802.3af-2003 & IEEE 802.3at-2009 & IEEE 802.3bt-2018 requirement.

This DC Disconnect continuously monitors port current after port inrush time, and disconnects port current when port current is below Ihold for more time than Tmpdo. The Power device shall deliver to prevent DC disconnect. Please refer to Ihold & Tmpdo in table 8 for detail information.

- **T sensor & Thermal Shutdown:**

The "T sensor" senses the temperature of each port, and will shutdown the port current as temperature beyond 160℃. When temperature goes down to 129℃, the port will start again.

- **Bias:**

The "Bias" provides the current & voltage bias for all ports according to control signals.

➢ **Autoclass:**

The 802.3bt PSEs have the new feature that implements an extension of Physical Layer classification known as Autoclass. The Autoclass purpose is to determine the actual maximum power of the connected PD by PSE for more effective supplying power.

Autoclass is only defined for single-signature PDs. PSE shall determine Autoclass level during Tauto_pse1 to Tauto_pse2 from power device to deliver maximum power consumption.

Tauto_pse1 and Tauto_pse2 define in table8.The Figure11 defines the enable autoclass timing. The classification event1 follows Tlce in table8.

➢ **Cascade:**

IP8008 provides a cascade interface which can communicate one master IP8008 device with up to 5 slave IP8008 devices and manage the system power/current allocation. This interface consists of 2 signals, CAS_CLK and CAS_DATA. To enter the cascade mode, the CAS_DATA must be pull up by an external resistor. Otherwise, the system operates on the single mode. Because the master device will download the initial register value of each device from EEPROM and upload those register value to related devices by the cascade bus, so the master device will delay 150ms to start the initialization procedure after reset. This means the power-on timing between different IP8008 devices in the bus should be within 150 ms. The following diagram shows the system hardware architecture.

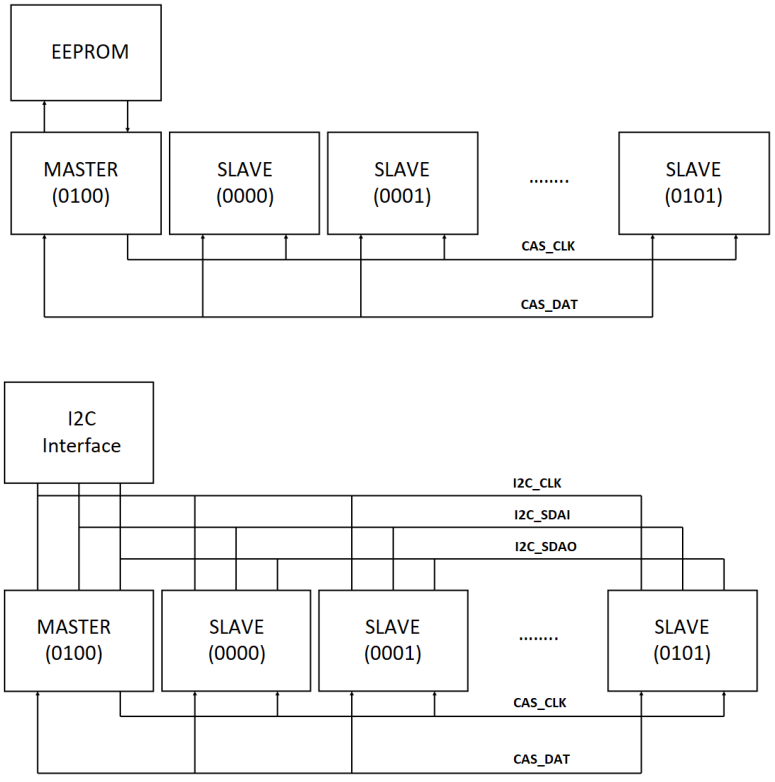


Figure 4 Cascade Block Diagram

There are four jobs which the cascade interface can take charge of.

In auto mode, the master device can download the initial register values from EEPROM and update register values to the related slave devices. Then it will detect the slave devices connected to the cascade bus and report the active status in Cascade Interface Initialization registers. The slave devices exit the idle state only when it receives a successful active query command from the master.

To prevent the system crash from the power lack, when a slave has a power-on request of incoming PD, the master will query and calculate the summation of the system consumed current and the PD current requirement. If the total current requirement is greater than the system available current defined in the registers, the master will reject the power-on request. Otherwise, the master will send a successful response to the slave to power on the incoming PD. To avoid the condition that slave does not receive the response coming from the master, slave request expiration time are defined and the slave will reject the request automatically after the time is expired. IP8008 provides 4 kinds of power up mode and 3 kinds of current allocation mode to fit the most conditions. And it also provides some registers to monitor the power-on sequence of incoming PD in Port Priority Registers.

When one port is turned off, the master will broadcast the information to all slave and they will re-order the power-on and victim sequence number.

When the system current monitor is enabled, the master device will query every active slave and calculate the total system consumed current periodically. The polling period is defined in the Master Current Query Time registers. For master device if it does not receive a successful response for some number of current query commands defined in the Master Disconnection Number registers, master will think the PSE is in a disconnect condition and report the event in the Slave inactive status registers. For slave device if it does not receive a successful current query command for a long time defined in the Slave Disconnection Time, the slave will think it disconnect the cascade interface and do two treatments of “keep current condition” and “cut off all ports” selected by the Slave Disconnection Mode.

When the system current limiter is enabled, master device will check the present system consumed current and the system available current. If the system consumed current is less than the system available current, the limiter will cut off one port selected by the victim strategy. The victim strategy of each PSE should the same one.

- **Multiple Power:**

IP8008 provides the entire system total power management function. According to four BK pins level, IP8008 has sixteen power banks that refer to power bank register. When the system consumed power over power bank of limitation, PSE would turn off the port power by the victim strategy for one time.

Multiple power could manage power with CPU. And BK pin status base on power supplies of power good signal.

4 Pin description

Type	Description	Type	Description
P	Power or Ground	OD	Open drain
I	Input	NC	No connection
O	Output	IPH	Internal pull high 50kohm to 3.3V
IL	Input latched upon reset	IPL	Internal pull low 50kohm to GND

Table 1 56 Pin description

Pin no.	Label	Type	Description
	EPAD	P	Exposed pad, it should be connected to AGND.
1	Mode0	IPH	Operation modes and system configuration setting. Defined to enter mode that refers to Table2. Default internal pull high. (For Maunal mode)
2	CAS_En	IPH	Cascade mode setting. Enable: NC, internal pull high. Disable: pull low to GND.
3	Ch0N	I/O	Channel 0 return path.
4	NC	NC	No connection.
5	Ch1N	I/O	Channel 1 return path.
6	AGND	P	Analog ground.
7	NC	NC	No connection.
8	Vrext	NC	No connection.
9	AGND	P	Analog ground.
10	Ch2N	I/O	Channel 2 return path.
11	NC	NC	No connection.
12	Ch3N	I/O	Channel 3 return path.
13	NC	NC	No connection.
14	LED_CLK	OD	LED clock pin
15	LED_DAT	OD	LED data pin
16	NC	NC	No connection.
17	V54	P	Main power supply input for chip. The 1uF capacitor should be added between V54 and AGND.
18	NC	NC	No connection.
19	Mode1	IPL	Operation modes and system configuration setting Defined to enter mode that refers to Table2. Default internal pull low. (For Maunal mode)
20	AV1P8	P	Internal 1.8V for internal use only. Adding an 4.7uF capacitor between V1P8 and AGND.
21	AGND	P	Analog ground.
22	AV3P3	P	When En_Reg pull high internally, the built-in 3.3V regulator is active, and besides IP8008 itself, V3P3 can provide 3.3V (6mA) for internal device. When En_Reg is connected to AGND, V3P3 should be connected to an external power 3.3V (6mA minimum) for IP8008. A 4.7uF capacitor should be added between V3P3 and AGND.

(Continued)

Pin no.	Label	Type	Description
23	BK1	I	Bank1, multiple power moniter of power supply 1.
24	BK2	I	Bank2, multiple power moniter of power supply 2.
25	In_Top	IPL	Test mode. Default internal pull low.
26	BK3	I	Bank3, multiple power moniter of power supply 3.
27	CAS_CLK	I/O	Cascade clock pin Master: Output Slave: Input
28	CAS_DAT	OD	Cascade data pin
29	NC/5V	NC/P	No connection.
30	En_Reg	IPH	The internal 3.3V regulator Enable: NC, internal pull high. Disable: pull low to GND.
31	Ch4N	I/O	Channel 4 return path.
32	NC	NC	No connection.
33	Ch5N	I/O	Channel 5 return path.
34	AGND	P	Analog ground.
35	NC	NC	No connection.
36	NC	NC	No connection.
37	AGND	P	Analog ground.
38	Ch6N	I/O	Channel 6 return path.
39	NC	NC	No connection.
40	Ch7N	I/O	Channel 7 return path.
41	NC	NC	No connection.
42	V_Test	O	Voltage output for internal reference monitor. Keep floating.
43	DV3P3	P	Digital power 3.3V. A 4.7uF capacitor should be added between DV3P3 and GNDD and DV3P3 should be connected to V3P3.
44	RSTN	I	It is a low active signal to reset IP8008.
45	INTB	OD/IO	Interrupt output and low active.
46	DGND	P	Digital ground, it should be connected to AGND.
47	DV1P8	P	Internal 1.8V for internal use only. Adding a 4.7uF capacitor between V1P8 and AGND.
48	AD0	I	I^2C device address bus AD0. Default setting Master port.
49	AD1	I	I^2C device address bus AD1. Default setting Master port.

(Continued)

Pin no.	Label	Type	Description
50	AD2	I	I^2C device address bus AD2. Default setting Master port.
51	AD3	I	I^2C device address bus AD3. Default setting Master port.
52	SCLO	I/OD	No use
53	SCLI/EE_CLK	I/OD	In manual mode, this pin is I^2C clock input. In auto mode, this pin is clock out to EEPROM.
54	SDAI/EE_DAT	I/OD	In manual mode, this pin is I^2C serial data input. In auto mode, this pin is data input from EEPROM.
55	SDAO	OD	I^2C serial data output.
56	BK0	I	Bank0, multiple power moniter of power supply 0.

5 Functional Description

5.1 System Reset

System reset occurs in either of the following conditions:

1. Reset triggered by the built-in power-on-reset circuit

IP8008 generates an internal power on reset signal when V54 is power on. It didn't leave reset state until V54 reaching V54_UVL. After reset, IP8008 still keeps on monitoring voltage level of V3P3, DV3P3, and V54. If the voltage level of V54 (V3P3) is below V54_UVL (V3P3_UVL),or over V54_OVL (V3P3_OVL), IP8008 enters reset state. Please refer to section 7.3 for detail specification of V54_UVL, and V3P3_UVL. It is note that there are two values for one parameter because of hysteresis.

2. Reset triggered by the reset pin (RstN)

3. Reset triggered by the software

- **System Control Register @ 0x04 of Page 0**

Bit #	R/W	Default	Description
7:1	R	0	**Reserved.**
0	R/W	0	**Software Reset**. Writing 1 to this bit initiates a system reset. After system reset, this bit is automatically cleared. Writing 0 has no effects. Reading this bit always returns 0.

5.2 Operation Modes & System Configuration

IP8008 operates in four possible modes, namely the **Auto Mode**, **Manual Mode**. The mode in which the chip operates in is determined by the two pins **Mode<1:0>** at system reset.

- **Auto Mode** means the chip is operating in a stand alone fashion, i.e. without the need for software intervention. The state machine does the detection, classification, power configuration, and system event monitoring automatically. The system events and status will be recorded in the corresponding registers, however, no interrupt will be generated and I^2C bus in this mode could be used.

  If there is an EEPROM, the contents of the EEPROM are loaded into the register file as initial values. Please refer to the section 5.4 for the description of the syntax of the contents of the EEPROM.

- **Manual Mode** means the chip will not be working, that is all ports are disabled, until the software has (1) enabled the port by writing 0x01 to the **Port Power Control Register**, the state machine start doing the detection, classification, power configuration, and system event monitoring as does in auto mode. The interrupt output pin will be active if the interrupt masks are turned off by software and predefined events occur. The ports can be disabled (power turned off and no further detection activity) by writing 0x00 to the **Port Power Control Register**. If the operation mode is either in manual mode, the host CPU can read register 0 (I^2C LSB Device Address Register) to make sure that IP8008 has done the system start up procedure.

Mode / Pin setting	Auto Mode			Manual Mode		
	LED Master	LED Slave	LED Disable	LED Master	LED Slave	LED Disable
Mode0	0	0	0	1	1	1
Mode1	0	0	0	0	0	0
AD2	1	0	X	1	0	X
LED_CLK	1	1	0	1	1	0
LED_DAT	1	1	0	1	1	0

Please refer to Section 5.10 for LED mode setting.

Table 2 Mode Setting

A summary of available functions in different modes

Function	Auto mode	Manual mode	Reference
Auto start detection,classification, and power up	V	-	Section 5.2
Program to detection, classification, and power up	-	V	Section 5.2
Access register through I^2C	V	V	Section 5.3
Load EEPROM	V	-	Section 5.4
LED master & slave	V	V	Section 5.10

Table 3 Available functions in Operation modes

- **System Configuration Register @ 0x03 of Page 0**

Bit #	R/W	Default	Description
7:6	R	Pin Setting	**Operation Modes**. At system reset, these bits latch the input pins **Mode <1:0>** to determine the operation mode. 00b: Auto Mode. 01b: Manual Mode.
5	R	0	**LED Mode.** LED interface is enabled by pulling up LED_DAT pin with a resister. 0 = Enable LED interface. 1 = Disable LED interface.
4	R	Pin Setting	**Cascade Mode.** When cascade mode enable, the IP8008 could communicate with other IP8008. The master would receive the imformation of the slaves and send the command by CAS_DATA and CAS_CLK signal lines. 0 = Enable Cascade mode. 1 = Disable Cascade mode.
3:0	R	0x00	Enable multiple power mode would detect BK0~3 pin low or high to switch power bank. The bank number could monitor the register. 0000b: Bank 0. 0001b: Bank 1. 0010b: Bank 2. 0011b: Bank 3. 0100b: Bank 4. 0101b: Bank 5. 0110b: Bank 6. 0111b: Bank 7. 1000b: Bank 8. 1001b: Bank 9. 1010b: Bank 10. 1011b: Bank 11. 1100b: Bank 12. 1101b: Bank 13. 1110b: Bank 14. 1111b: Bank 15.

- **Scratch Register @ 0x05 of Page 0**

Bit #	R/W	Default	Description
7:0	R/W	0x00	**Scratch Register**. A scratch pad that can be written any value. The value will be reset to 0 when system reset occurs.

- **Watchdog Timer Register @ 0x06 of Page 0**

Bit #	R/W	Default	Description
7	R/W	0	**Enable Watchdog Timer**. 0 = Disable watchdog timer. 1 = Enable watchdog timer.
6:0	R/W	0x7F	**Watchdog Timer (unit: 100ms)**. When enabled, the watchdog timer starts counting down every 100ms, when the watchdog timer reaches 0, a watchdog reset will be generated to reset the whole chip.

- **bt Mode Register @ 0x07 of Page 0**

Bit #	R/W	Default	Description
3:0	R/W	0x0F	**bt/at&af Mode**. The 4 bits represent the 8 at port combine the 4 bt ports, where bit 0 corresponds to port 0&1combine bt port, and bit 1 corresponds to port 2&3 combine bt port, etc. 0 = at 2 pair mode. 1 = bt 4 Pair mode. In manual mode , this register could be written by host CPU. (Before the mode is changed, the related port should be disabled.)

- **at/af Mode Register @ 0x09 of Page 0**

Bit #	R/W	Default	Description
7:0	R/W	0xFF	**at/af Mode**. The 8 bits represent the af/at mode of the 8 ports, where bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc. 0 = af mode. 1 = at mode. In manual mode, this register could be written by host CPU. (The mode should be set at/af mode.)

- **Alternative A/B Register @ 0x0A of Page 0**

Bit #	R/W	Default	Description
7:0	R/W	0x00	**Alternative A/B**. At system reset, these bits can also be set by software in manual mode or by EEPROM in auto mode. 0: Alternative A 1: Alternative B Bit 0 corresponds to port 0, bit 1 corresponds to port 1, and so on.

5.3 I²C Slave Interface

Through the I²C slave interface of IP8008, host CPU can access the register file in IP8008. It consists of SCL, SDAO and SDAI pins, where SCL is Clock, SDAO is Serial Data Output and SDAI is Serial Data Input. It should be note that SDAO and SDAI could be connected to implement a bidirectional data pin. This I²C interface supports the 7-bit addressing mode of the I²C standard.

There can be up to eight IP8008 chips on one I²C bus, the LSB 4 bits of the I²C address can be assigned with the address pin AD3~AD0. The MSB 3 bits of the I²C address are fixed at **110b**.

The following diagram is the register read/write cycles of the I²C bus.

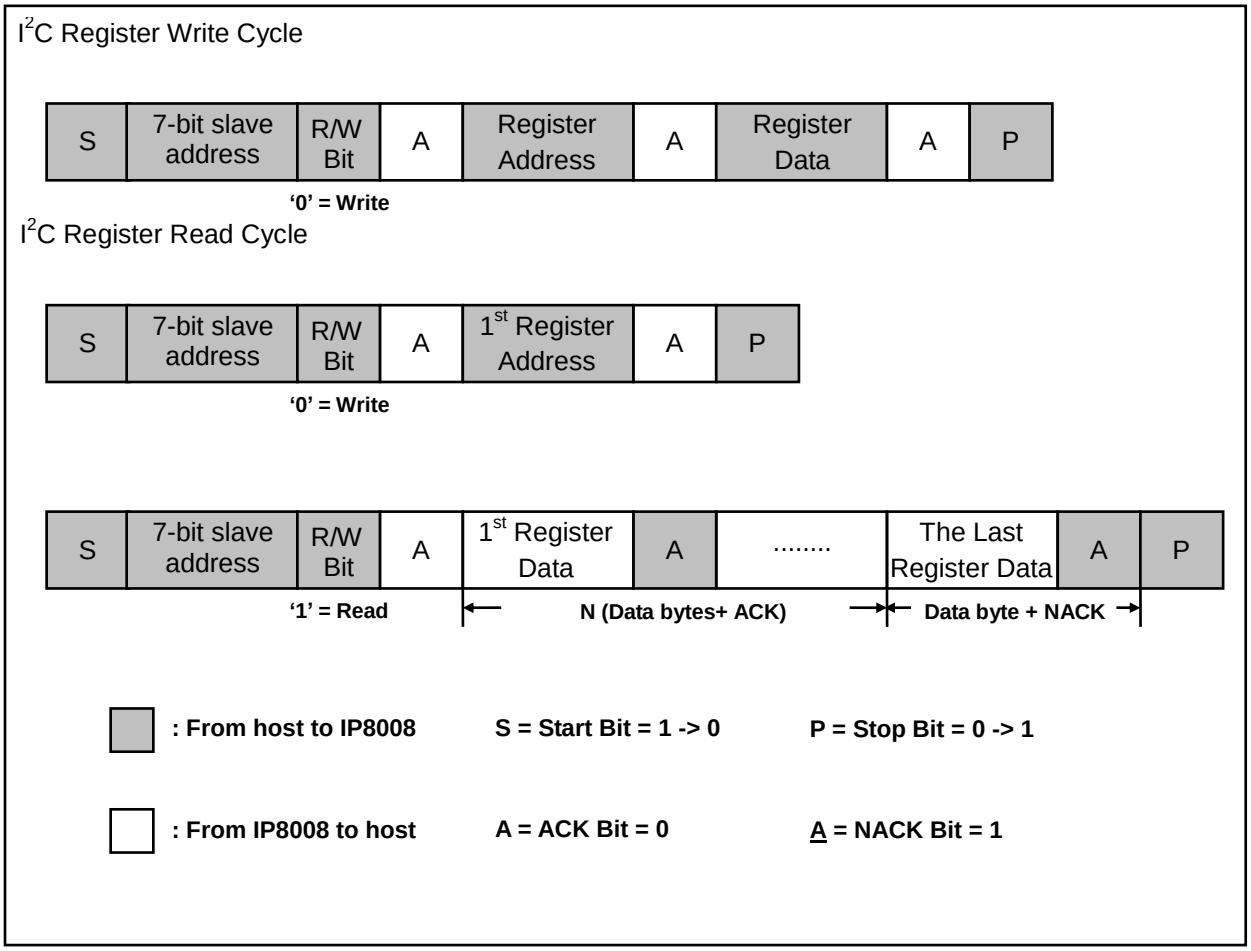


Figure 5 I² C bus write cycles diagram

Following the 7-bit slave address and read/write bit, the 1st data byte received by IP8008 is always interpreted as the register address to be accessed, thus named the address byte.

In a write cycle, following the address byte, there is only one byte, which contains the register data to be written. IP8008 replies an ACK to the host whenever it receives a data byte. After writing this byte, the host should terminate the write cycle by sending a STOP bit.

In a read cycle, the host writes only one byte, which contains the initial address of registers to be read, to the IP8008 firstly. Then the host needs to start another I²C cycle with its read/write bit set to 1. IP8008 will continue to send out the next data and increase the address by one automatically whenever the host acknowledges a data byte with an ACK, If the calculated register address is valid (within valid address range). The host can terminates a read cycle by sending a NACK following by a STOP bit. If the address of the data to be sent back falls out of valid register address range, IP8008 always returns 00h.

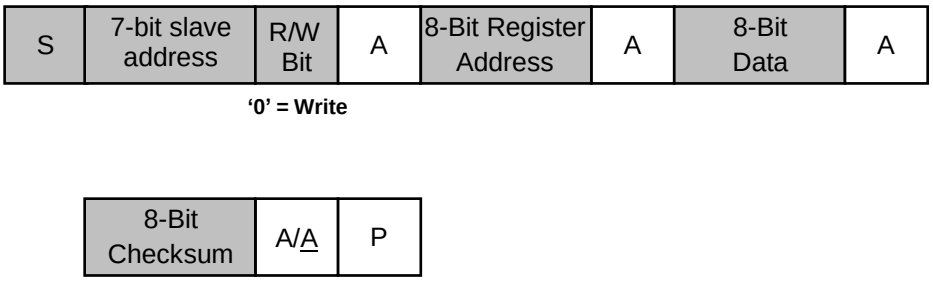
- **I²C Device Address Register @ 0x00 of all Pages**

Bit #	R/W	Default	Description
7:6	R/W	00	**Register Page**. This bit specifies the page number of the register to be accessed through the I²C interface. 0: page 0, 1: page 1, 2: page 2,
3:0	R	Pin setting	**I²C LSB Device Address**. Unique device address to identify this chip on the I²C bus. This address is latched in from the input pins AD3~AD0.

The highest I²C clock speed supported is 800KHz. However, in order to prevent abnormal activity on the I²C bus from hanging IP8008, the I²C interface implements a time out mechanism. Host CPU can stop the I²C clock when it's low and resume the clock within 30ms. If the clock does not resume within 10ms, the I²C interface will abort the current I²C cycle and wait for the next START condition.

To improve reliability, the I²C slave can optionally support checksum mechanism. The I²C checksum mechanism is enabled using the **System Configuration Register**. When the checksum mechanism is enabled, checksums will be added to the I²C read/write cycles. When checksum fails in write cycle, access to the register is ignored. When checksum fails in read cycle, the data read by the I²C master should be considered corrupted. The following diagrams are the register read/write cycles of the I²C interface with checksum enabled.

I²C Register Write Cycle with Checksum



The 8-bit checksum for I^{2}C write cycle is calculated as the following:

0xFF - (7-bit slave address and R/W bit + 8-bit register address + 8-bit data + carry out bits) = 8-bit checksum.

In write cycle, the IP8008 will verify the checksum bits and if the checksum fails, the data will not be written into the register and a NACK bit is sent back to the host. If the checksum succeeds, the register will be written and an ACK bit is sent back to the host.

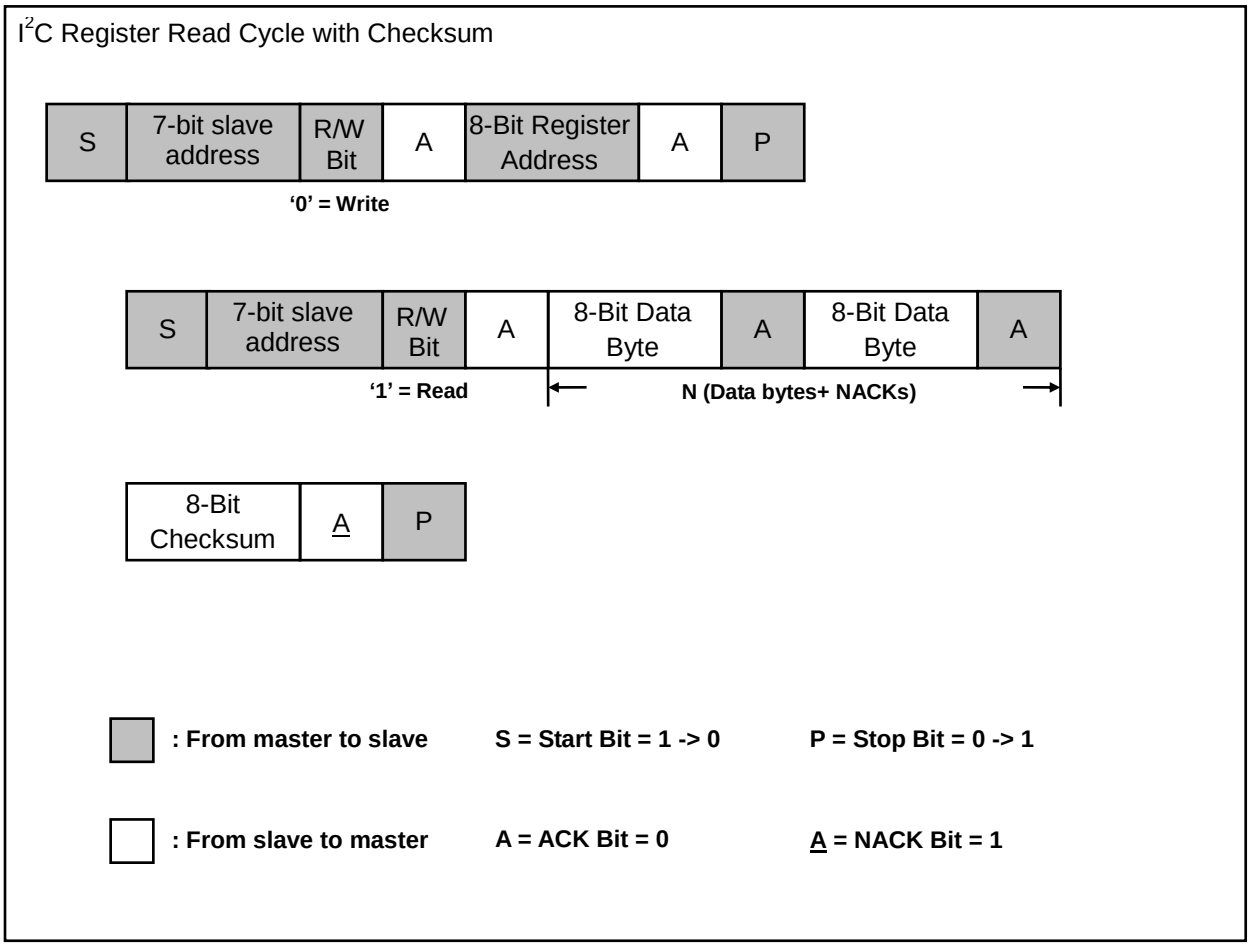


Figure 6 I^2 C bus read cycles diagram

The 8-bit checksum for I^{2}C read cycle is calculated as the following:

0xFF - (7-bit slave address and R/W bit + 8-bit data + carry out bits) = 8-bit checksum.

When the desired data byte is read by the host, the host can send a NACK bit to IP8008; in return, IP8008 will send out an 8-bit checksum. The host should again send a NACK bit to IP8008 and then the STOP bit. The checksum then can be used by the host to verify if the read data byte is corrupted.

5.4 EEPROM controller

When IP8008 operates in auto mode, the register file can be loaded with some initial value from external EEPROM (24xx series EEPROM, Maximum support to 24C16). IP8008 reads the EEPROM starting from address 0, parses the contents of the EEPROM command blocks, checks for integrity of the contents, and then writes the designated registers. This process continues until there is either no more data or the integrity check fails. EEPROM is necessary only if user wants to modify the default value of registers in auto mode.

To check the existence of EEPROM connected to the IP8008, the first byte of EEPROM (Byte 0) must be 0x5A.

The format of the EEPROM follows:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	1	0	1	0
1	Device ID				Number of Data Bytes			Valid
2	Starting Register Address							
3	Data Byte 0							
4	Data Byte 1							
…	…							
3 + N	Data Byte N							
4 + N	Checksum Byte							
5 + N	Next Data Block							
	…							
	Last Block							
EOP	0	0	0	0	0	0	0	0

Figure 7 EEPROM Format

Where:

- **Device ID**: 0100b = Master, 0000b = Slave0, 0001b = Slave1, 0010b = Slave2, 0011b = Slave3, other values of Device ID are invalid and the EEPROM loading process will be stopped.
- **Number Of Data Bytes**: the number of data bytes in this command block. 0 = 1 byte, 1 = 2 bytes, etc.
- **Valid Bit**: If the valid bit is 0x1, IP8008 will continue to process the data block. Otherwise if the valid bit is 0x0, the EEPROM download operation will be stopped.
- **Page Number**: the page number of the register to be loaded.
- **Starting Register Address**: the starting register address to be loaded by the following data bytes.
- **Data Bytes**: the data bytes to be loaded in to specified registers.
- **Checksum Byte**: the checksum byte is the checksum of all previous bytes in the command block. The checksum is calculated by adding all the previous bytes with the carry bit (if any) adding back to the sum. If the checksum fails, the system start up procedure fails and the system halt.

5.5 PSE State Machine

IP8008 has eight channels and each channel is mainly controlled by a state machine to perform the detection, classification, and powering up procedures. As the eight state machines run in parallel, they contend for ADC 1 in the detection and classification procedures. Thus an arbiter is needed to grant the access rights among the eight state machines.

Furthermore, to limit the chip inrush current, a maximum of two ports are allowed to start their classification procedures simultaneously. And only one port is allowed to turn on power at a time. After successful detection, classification, and power configuration, the port power is turned on.

The state machine is also designed to respond to abnormal power events, such as overload, short circuit, and overheat (thermal shutdown); basically port power will be turned off when such event happens. It takes time to cool off the device after power is turned off, so the state machine will delay a certain amount of time before starting next detection procedure for the port. The above mentioned programmable amount of time is set in the **Error Delay Register**.

- **Ch0~7N Power Control Registers @ 0x10~0x17 of Page 0**

Bit #	R/W	Default	Description
4	R/W	0	**Suspend Power Up.** When set to 1 at manual mode, the state machine will be suspended before entering the power up state (thus the port will not be powered up) until the **Port Power Up Suspend Control** bit is set to be 1.
3:2	R/W	01	**PSE Initial State in the Auto Mode.** **00** = **PSE port disabled**. The port is disabled, port power is turned off, and the PSE state machine returns to the IDLE state. **01** = **PSE port enabled**. The port is enabled, and the PSE state machine starts the detection process if the port is not in error condition and the **Start State Machine** bit in the **State Machine Control Register** is set to be 1. **10** = **PSE port force power on**. The port is forced to turn power on without going through the normal detection, classification, and power configuration processes. This is used for testing purpose, not for normal operation. **11** = **PSE port enabled (skip classification)**. The port is enabled, and the PSE state machine skips the classification process and turn on the power directly. This is only used for testing purpose and not for normal operation.
1:0	R/W	01	**PSE Enable.** **00** = **PSE port disabled**. The port is disabled, port power is turned off, and the PSE state machine returns to the IDLE state. **01** = **PSE port enabled**. The port is enabled, and the PSE state machine starts the detection process if the port is not in error condition and the **Start State Machine** bit in the **State Machine Control Register** is set to be 1. **10** = **PSE port force power on**. The port is forced to turn power on without going through the normal detection, classification, and power configuration processes. This is used for testing purpose, not for normal operation. **11** = **PSE port enabled (skip classification)**. The port is enabled, and the PSE state machine skips the classification process and turn on the power directly. This is only used for testing purpose and not for normal operation.

➢ **Port 0~7 State Machine Control Registers @ 0x18~0x1F of Page 0**

Bit #	R/W	Default	Description

5:0	R	0x00	**Current State of the State Machine.**
			Current state of the state machine.
			If (State Machine Indicator==0)
			00 = Disable
			01 = Idle
			03 = Test_Error
			04 = Start_Detect
			05 = Detect_Evaluate
			06 = Start_Cxn_Check
			07 = Cxn_Check_Evaluate
			0A = Back_Off
			0B = Classification
			0E = Class_EV1_LCE
			10 = Mark_EV1
			11 = Class_EV2
			12 = Mark_EV2
			13 = Class_EV3
			14 = Mark_EV3
			15 = Class_EV4
			16 = Mark_EV4
			17 = Class_EV5
			18 = Mark_EV_Last
			19 = Mark_EV_Last_Halt
			1A = Class_Evaluate
			1B = Power_Deny
			1C = Power_Up
			1D = Power_On
			1E = Primary_Semi_Power_On
			1F = Secondary_Semi_Power_On
			20 = Error_Delay
			21 = Next_Delay
			22 = ALT_AB_Wait
			23 = Power_Up_Suspend
			24 = Casc_Suspend
			If (State Machine Indicator==1)
			01 = Initial
			02 = Idle
			03 = Wait
			04 = Start_Detect
			05 = Detect_Evaluate
			06 = Classification
			07 = Class Probe
			08 = Class_Reset
			09 = Class_EV1_LCE
			0A = Mark_EV1
			0B = Class_EV2
			0C = Mark_EV2
			0D = Class_EV3
			0E = Mark_EV3
			0F = Class_EV4
			14 = Mark_EV_Last
			15 = Mark_EV_Last_Halt

Bit #	R/W	Default	Description
			16 = Class_Evaluate 17 = Power_Up 18 = Power On 19 = Power_Update **1A = Error_Delay** 1B = Power_Deny **1C = Next_Idle** 1D = Power_Up_Suspend 1E = Casc_Suspend

- **Port 0~7 Detected and Connection Check Signature Registers @ 0x20~0x27 of Page 0**

Bit #	R/W	Default	Description
5:4	R	0x0	**Connection Check Signature** 0 = Invalid 1 = Alternative A/B 2 = Single Signature 3 = Dual Signature
2:0	R	0x0	**Detected Signature**. 0 = Bad 1 = Good 2 = Open 3 = Short 4 = C Too Large 5 = R Too Low 6 = R Too High

- **Port 0~7 Invalid Signature Counter Registers @ 0xC0~0xC7 of Page 1**

Bit #	R/W	Default	Description
7:0	R	0x00	**Invalid Signature Counter**. When an invalid signature is detected in the detection process, this counter is increased by 1.

- **Port 0~7 PD Requested Class / Auto Class Status Registers @ 0x28~0x2F of Page 0**

Bit #	R/W	Default	Description
4	R/W	0x0	**Auto Class Status of Port0** 0: Enable 1: Disable
3:0	R	0xF	**PD of Requested Class of Port0** According to PD provide the class event, register record PD real classifcation. 0000: Class0 0001: Class1 0010: Class2 0011: Class3 0100: Class4 0101: Class5 0110: Class6 0111: Class7 1000: Class8 1001: Classification signature error 1010: Class error 1111 : Initial Class (Note: If PSE would not enough power, register would be incorrect.) (Note: Enable class probe to detect correct PD requested class)

- **Port 0~7 PD Allocated Registers @ 0x30~0x37 of Page 0**

Bit #	R/W	Default	Description
3:0	R	0x0F	**PD Allocated Class of of Port0** Based on PSE total power for per port and PD request class to define the PD currect classification. 0001: Class1 0010: Class2 0011: Class3 0100: Class4 0101: Class5 0110: Class6 0111: Class7 1000: Class8 1111 : Initial Class (Note: if PD requested class0 , PD allocate class3)

- **PSE 4 Pair Setting Register @ 0x0D of Page 0**

Bit #	R/W	Default	Description
2	R/W	0	**Force Auto Class Enable** 0: Disable 1: Enable
1	R/W	0	**Auto Class Enable** 0: Disable 1: Enable
0	R/W	0	**Enable Full Class Event** 0: Disable 1: Enable

- **Error Delay Register @ 0xAC of Page 2**

Bit #	R/W	Default	Description
7:0	R/W	0xAC	**Error Delay.** The programmable error delay in units of 100ms.

5.6 Power Manager

Power manager is responsible for two tasks: **power trunk, power configuration**, **power monitoring, power limiter**. Power trunk is task to limit PSE turn on threshold. Power configuration is the task to allocate power to the ports requesting for power. Power monitoring is the task to monitor power conditions (current, voltage, and temperature). When invalid conditions occur, proper actions will be taken to prevent hazardous consequences.

5.6.1 Power Trunks

Before doing power configuration, the total available power must be determined first. IP8008 supports two trunks of power, where each power trunk has its own set of parameters to facilitate the calculation of total available power. If PD turns on power, the real available power should be larger than class assigned power.

Power Trunk – PSE Power Estimation Mode = Real Available Power

- **Trunk Power Limit** is the maximum power supply capacity allocated to the power trunk.
- **PSE Power Estimation Mode** is the calculated mothed of total real load power.

- **Trunk 0/1 Select Register @ 0xD8 of Page 0**

Bit #	R/W	Default	Description
0	R/W	0	**Trunk Select**. Writing to this register will switch power trunk. Note that whenever the parameters of the power trunk currently in use are updated, this Trunk Select Register must also be written to make the newly updated parameters in effect. 0 = Trunk 0, 1 = Trunk 1.

- **Trunk 0 Power Limit Register @ 0xD9~0xDA of Page 0**

Bit #	R/W	Default	Description
1:0	R/W	01	**Trunk 0 Power Limit MSB**.
7:0	R/W	0x7C	**Trunk 0 Power Limit LSB**. Trunk Power Limit specifies the upper limit of the power supply. Default is 380 Watts. The MSB 10 bits are integer . Unit is in W.

- **Trunk 1 Power Limit Register @ 0xDB~0xDC of Page 0**

Bit #	R/W	Default	Description
1:0	R/W	01	**Trunk 1 Power Limit MSB**.
7:0	R/W	0x7C	**Trunk 1 Power Limit LSB**. Trunk Power Limit specifies the upper limit of the power supply. Default is 380 Watts. The MSB 10 bits are integer. Unit is in W.

- **PSE Power Estimation Mode Register @ 0x6C of Page 0**

Bit #	R/W	Default	Description
1:0	R/W	00	**PSE Power Estimation Mode** 0 = PSE Idea Class Power 1 = PSE Real Consumed Power 2 = PSE Max Consumed Power 3 = PSE Real Consumed Power and Auto Class Power

5.6.2 Power Configuration

Power manager is responsible to allocate powers to the ports that pass the detection and classification process. To do so, several parameters must be specified or be calculated in advance:

1) Power Allocation Mode (specified in register 0x6C, page0).

- **Power Allocation Mode** specifies the way to determine the requested port power in the power configuration process.

- **Power Allocation Mode Register 0 @ 0x6C of Page 0**

Bit #	R/W	Default	Description
3:2	R/W	01	**Power Allocation Mode** 1 = Class Power

5.6.3 Port Polling

Besides power configuration, power manager is also responsible for the monitoring of port current (I), port voltage (V), and port temperature (T). When either of IVT is out of its valid range, power manager will take prompt actions to prevent the system from hazardous consequences.

Power manager do the monitoring by periodically polling the IVT of each port. The poll period can be specified in the **IVT Poll Register**.

- **Force Poll Register @ 0x80 of Page 0**

Bit #	R/W	Default	Description
7:0	R/W	0x00	**Force Poll**. Writing 1 to a bit will force an IVT poll on the corresponding port. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc. When the polling completes, the bit will be cleared automatically.

- **IVT Poll Register @ 0x81 of Page 0**

Bit #	R/W	Default	Description
7	R	1	**IVT on Processing**.
4	R/W	1	**Auto Poll**. Enable automatically polling of IVT of powered ports. In auto mode, this bit will be set to 1 automatically after system reset.
3:0	R/W	0x00	**IVT Poll Interval**. Number of 1ms between each poll to the port IVT

- **Port 0~7 Current Registers @ 0x90~0x9F of Page 0**

Bit #	R/W	Default	Description
4:0	R	0x00	**Port 0 Current MSB**. The MSB 11 bits are integer and the LSB 2 bits are fractional. Unit is in mAmp. This value is updated every time the port is polled.
7:0	R	0x00	**Port 0 Current LSB**.
4:0	R	0x00	**Port 1 Current MSB**.
7:0	R	0x00	**Port 1 Current LSB**.
4:0	R	0x00	**Port 2 Current MSB**.
7:0	R	0x00	**Port 2 Current LSB**.
4:0	R	0x00	**Port 3 Current MSB**.
7:0	R	0x00	**Port 3 Current LSB**.
4:0	R	0x00	**Port 4 Current MSB**.
7:0	R	0x00	**Port 4 Current LSB**.
4:0	R	0x00	**Port 5 Current MSB**.
7:0	R	0x00	**Port 5 Current LSB**.
4:0	R	0x00	**Port 6 Current MSB**.
7:0	R	0x00	**Port 6 Current LSB**.
4:0	R	0x00	**Port 7 Current MSB**.
7:0	R	0x00	**Port 7 Current LSB**.

- **Port 0~7 Voltage Registers @ 0xA0~0xAF of Page 0**

Bit #	R/W	Default	Description
3:0	R	0x00	**Port 0 Voltage MSB**. The MSB 8 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Volts. This value is updated every time the port is polled. Note that the true port voltage is (**Supply Voltage - Port Voltage**). Please refer to Supply Voltage Registers.
7:0	R	0x00	**Port 0 Voltage LSB**.
3:0	R	0x00	**Port 1 Voltage MSB**.
7:0	R	0x00	**Port 1 Voltage LSB**.
3:0	R	0x00	**Port 2 Voltage MSB**.
7:0	R	0x00	**Port 2 Voltage LSB**.
3:0	R	0x00	**Port 3 Voltage MSB**.
7:0	R	0x00	**Port 3 Voltage LSB**.
3:0	R	0x00	**Port 4 Voltage MSB**.
7:0	R	0x00	**Port 4 Voltage LSB**.
3:0	R	0x00	**Port 5 Voltage MSB**.
7:0	R	0x00	**Port 5 Voltage LSB**.
3:0	R	0x00	**Port 6 Voltage MSB**.
7:0	R	0x00	**Port 6 Voltage LSB**.
3:0	R	0x00	**Port 7 Voltage MSB**.
7:0	R	0x00	**Port 7 Voltage LSB**.

- **Port 0~7 Temperature Registers @ 0xB0~0xBF of Page 0**

Bit #	R/W	Default	Description
4:0	R	0x00	**Port 0 Temperature MSB**. The MSB 9 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Celsius. This value is updated every time the port is polled.
7:0	R	0x00	**Port 0 Temperature LSB**.
4:0	R	0x00	**Port 1 Temperature MSB**.
7:0	R	0x00	**Port 1 Temperature LSB**.
4:0	R	0x00	**Port 2 Temperature MSB**.
7:0	R	0x00	**Port 2 Temperature LSB**.
4:0	R	0x00	**Port 3 Temperature MSB**.
7:0	R	0x00	**Port 3 Temperature LSB**.
4:0	R	0x00	**Port 4 Temperature MSB**.
7:0	R	0x00	**Port 4 Temperature LSB**.
4:0	R	0x00	**Port 5 Temperature MSB**.
7:0	R	0x00	**Port 5 Temperature LSB**.
4:0	R	0x00	**Port 6 Temperature MSB**.
7:0	R	0x00	**Port 6 Temperature LSB**.
4:0	R	0x00	**Port 7 Temperature MSB**.
7:0	R	0x00	**Port 7 Temperature LSB**.

- **Supply Voltage Registers @ 0x8E~0x8F of Page 0**

Bit #	R/W	Default	Description
3:0	R	0x00	**Supply Voltage**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0x00	**Supply Voltage**. The MSB 8 bits are the integer part, where the LSB 4 bits are the fractional part. The supply voltage in Volts.

5.6.4 Power Event Handling

After the IVTs are polled and recorded, the power manager checks the polled values against predefined valid ranges. If the polled values drop out of the predefined valid range, power events are recorded and handled. The power events triggered by power manager **Port Current Limit Event, Port Voltage Limit Event, and Port Temperature Limit Event**.

When a power event occurs, if its corresponding power event handle bit is 1, the port power is turned off. If IP8008 is in manual mode, and the power event's corresponding status mask bit is 1, an interrupt will be issued to the host CPU.

- **Port Currrent Limit Event.** After the port is polled and if the port current is above the value specified in **Port Currrent Limit Register**, a **Port Currrent Limit Event** occurs.
- **Port Voltage Limit Event.** After the port is polled and if the port voltage is above the value specified in **Port Voltage Limit Register**, a **Port Voltage Limit Event** occurs.
- **Port Temperature Limit Event.** After the port is polled and if the port temperature is above the value specified in **Port Temperature Limit Register**, a **Port Temperature Limit Event** occurs.
- **Port IVT Event Handler Registers @ 0x68 of Page 0**

Bit #	R/W	Default	Description
7:5	R/W	000	**Port IVT Event Handler.** [7] - Temperature Limit Event Handler [6] - Voltage Limit Event Handler [5] - Current Limit Event Handler

- **Port Current Limit Registers @ 0xB0~0xBF of Page 1**

Bit #	R/W	Default	Description
4:0	R/W	0x00	**Port 0 Current Limit MSB.** The MSB 11 bits are the integer part and the LSB 2 bits are the fractional part. The unit is mAmps. This value is updated every time the port is polled.
7:0	R/W	0x00	**Port 0 Current Limit LSB.**
4:0	R/W	0x00	**Port 1 Current Limit MSB.**
7:0	R/W	0x00	**Port 1 Current Limit LSB.**
4:0	R/W	0x00	**Port 2 Current Limit MSB.**
7:0	R/W	0x00	**Port 2 Current Limit LSB.**
4:0	R/W	0x00	**Port 3 Current Limit MSB.**
7:0	R/W	0x00	**Port 3 Current Limit LSB.**
4:0	R/W	0x00	**Port 4 Current Limit MSB.**
7:0	R/W	0x00	**Port 4 Current Limit LSB.**
4:0	R/W	0x00	**Port 5 Current Limit MSB.**
7:0	R/W	0x00	**Port 5 Current Limit LSB.**
4:0	R/W	0x00	**Port 6 Current Limit MSB.**
7:0	R/W	0x00	**Port 6 Current Limit LSB.**
4:0	R/W	0x00	**Port 7 Current Limit MSB.**
7:0	R/W	0x00	**Port 7 Current Limit LSB.**

- **Supply Voltage Limit Registers @ 0xA0~0xA3 of Page 1**

Bit #	R/W	Default	Description
3:0	R/W	0x00	**Supply Voltage Upper Limit MSB.** The MSB 8 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Volts. This value is updated every time the port is polled.
7:0	R/W	0x00	**Supply Voltage Upper Limit LSB.**
3:0	R/W	0x00	**Supply Voltage Lower Limit MSB.**
7:0	R/W	0x00	**Supply Voltage Lower Limit LSB.**

- **Port Temperature Limit Registers @ 0xA4~0xA5 of Page 1**

Bit #	R/W	Default	Description
4:0	R/W	0x0A	**Port Temperature Limit MSB.** The MSB 9 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Celsius. This value is updated every time the port is polled.
7:0	R/W	0x0A	**Port Temperature Limit LSB.**

5.7 Real time Monitor Power Event

Power event described in previous sections are discovered only when the ports are polled. The analog monitor can continuously watch over and report time-critical power events so that the power manager can take prompt actions. Power events from analog monitor include power deny, severe short circuit event, thermal shutdown event, voltage bad to GND event, MPS error event (DC Disconnect), short circuit event, overload event, power off event caused by max pairset power limit, power off event caused by auto class power limit, power off event caused by power bank limit, power off event caused by hgh priority port power up, power off event caused by total power limit.

- **Power Deny** is the event where the PSE occurs turn off port power about power limit include 100W power limiter, power trunk, power bank event, high priority port power up, and auto power limiter.
- **Power Up Suspend** is the event that PSE would suspend before entering the power up state. Detection, connection check, and classification are pass, IP8008 would suspend and trigger event before PSE turn on power at the manual mode.
- **Severe Short Circuit Event** is the event where the port current is over 1.7 Amp. Immediate action must be taken to eliminate such event. The power manager responds to this event by temporarily turn off port power.
- **Thermal Shutdown Event** is the event where the port temperature is over the pre-defined thermal shutdown threshold. The port power is turned off and the port is eligible for detection only after the port is cooled off (temperature drops below the threshold).
- **Voltage Bad to GND Event** is the event that port to ground voltage is over voltage bad to GND threshold. When voltage bad to GND occurs, port current will be limit immediately to protect IP8008.
- **MPS Event** is the event the port cannot maintain its power signature (MPS). If the event lasts for specified period of time (Tmpdo), this will be considered an **MPS error event** and the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Short Circuit** ($\mathbf{I_{LIM}}$) **Event** is the event where port current is greater than I_{LIM}. This event should be sampled by the power manager to determine if a **short circuit event** has occurred either during the power up process or after the port being powered up. When a short circuit condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Overload** ($\mathbf{I_{CUT}}$) **Event** is the event where port current is greater than I_{CUT}. If the event lasts for specified period of time, this will be considered an **overload event**. When an overload condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Power Off Event Caused by Max Pairset Power Limit** is the event that port power is over 100W. If the event lasts for specified period of time, this will be considered a power off event caused by max pairset power limit. When the event occurs, the port power will be turned off. Base on victim strategy register to turn off port when the event occurs.
- **Power Off Event Caused by Auto Class Power Limit** is the event that port power is over auto class margin at autoclass mode. Base on victim strategy register to turn off port when the event occurs.
- **Power Off Event Caused by Power Bank Limit** is the event that IP8008 switches the power bank to be over the bank threshold. When IP8008 would occur power off caused by power bank limit, PSE would turn off the lower priority port power one time. Base on victim strategy register to turn off port when the event occurs.
- **Power Off Event Caused by High Priority Port Power Up** is the event when IP8008 turned off the lower priority port power. When IP8008 power off event occurs, IP8008 should determine turn off port by setting port priority. Base on victim strategy register to turn off port when the event occurs.

- **Power Off Event Caused by Total Power Limit** is the event that port would be turned off power when PSE total current/power is over PSE available current/power thresholds. Base on victim strategy register to turn off port when the event occurs.
- **Temperature Threshold Event (IVT)** is the event when polling temperature over setting port temperature limitation. If enable temperature limit event handler, PSE would turn off port power immediately when the event occurs. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Voltage Threshold Event (IVT)** is the event when polling supply would be over setting port supply voltage upper/lower limitation. If enable voltage limit event handler, PSE would turn off port power immediately when the event occurs. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Current Threshold Event (IVT)** is the event when polling current would be over setting port current limitation. If enable current limit event handler, PSE would turn off all port power immediately when the event occurs. After the power is turned off the port start another detection process after about 1.6 seconds.

A summary of power off conditions

Condition	Item	Power off moment	Reference Section
Port I > 1.7A	Severe Short Circuit Event	Real-time monitor	5.7
Port T > 160℃	Thermal Shutdown Event	Real-time monitor	5.7
ChN V –GND > Voltage bad to GND threshold	Voltage Bad to GND Event	Real-time monitor	5.7
Port I < I_hold	MPS Event	Real-time monitor	5.7
Port I > Ilim	Short Circuit Event	Real-time monitor	5.7
Port I > Icut	Overload (I_{CUT}) Event	Real-time monitor	5.7
Port W > 100W	Power Off Event Caused By Max Pairset Power Limit	IVT polling	5.7
Port W > Autoclass margin	Power Off Event Caused By Auto Class Power Limit	Real-time monitor	5.7
PSE W > Power bank limit	Power Off Event Caused By Power Bank Limit	IVT polling	5.7
PSE turns off the lower priority port power	Power Off Event Caused By High Priority Port Power Up	Real-time monitor	5.7
PSE I/W > Total power limit	Power Off Event Caused By Total Power Limit	IVT polling	5.7
Port T > Port temperauture limit	Temperature Threshold Event (IVT)	IVT polling	5.7
Supply voltage > Supply Voltage Upper limit Supply voltage < Supply Voltage Lower limit	Voltage Threshold Event (IVT)	IVT polling	5.7
Port I > Port current limit	Current Threshold Event (IVT)	IVT polling	5.7

Table 4 Port power off conditions

5.8 Port Status and Interrupt

Port state and power events are recorded in the registers. In manual mode, these statuses can generate interrupts to host CPU for further processing.

➢ **Port Status Control Register @ 0x0F of Page 0**

Bit #	R/W	Default	Description
6	R/W	0	**Show Elim and Ecut Event On Both Pairsets When a single-signature PD has Elim or Ecut Event on one pairset.** Write 1 to disable, write 0 to enable.
5	R/W	0	**Disable Severe Short Circuit Event**. Write 1 to disable, write 0 to enable.
4	R/W	0	**Disable Thermal Shutdown Event**. Write 1 to disable, write 0 to enable.
3	R/W	0	**Disable Voltage Bad to GND Event**. Write 1 to disable, write 0 to enable.
2	R/W	0	**Disable MPS (DC Disconnect) Event**. Write 1 to disable, write 0 to enable.
1	R/W	0	**Disable Short Circuit Limit (I_{LIM}) Event**. Write 1 to disable, write 0 to enable.
0	R/W	0	**Disable Overload (I_{CUT}) Event**. Write 1 to disable, write 0 to enable.

➢ **Port 0~7 Port Status 0 Register @ 0x70~0x7F of Page 0**

Bit #	R/W	Default	Description
7	W1C	0	**Power Deny**. In manual mode, write 1 to clear the bit.
6	W1C	0	**Power Up Suspend**. In manual mode, write 1 to clear the bit.
5	W1C	0	**Severe Short Circuit Event**. In manual mode, write 1 to clear the bit.
4	W1C	0	**Thermal Shutdown Event**. In manual mode, write 1 to clear the bit.
3	W1C	0	**Voltage Bad to GND Event**. In manual mode, write 1 to clear the bit.
2	W1C	0	**MPS (DC Disconnect) Event**. In manual mode, write 1 to clear the bit.
1	W1C	0	**Short Circuit Limit (I_{LIM}) Event**. In manual mode, write 1 to clear the bit.
0	W1C	0	**Overload (I_{CUT}) Event**. In manual mode, write 1 to clear the bit.

➢ **Port 0~7 Port Status 1 Register @ 0x70~0x7F of Page 0**

Bit #	R/W	Default	Description
7	W1C	0	**Power Off Event Caused By Max Pairset Power**. In manual mode, write 1 to clear the bit.
6	W1C	0	**Power Off Event Caused By Auto Class Power Limit**. In manual mode, write 1 to clear the bit.
5	W1C	0	**Power Off Event Caused By Total Power Bank Limit**. In manual mode, write 1 to clear the bit.
4	W1C	0	**Power Off Event Caused By High Priority Port Power Up**. In manual mode, write 1 to clear the bit.
3	W1C	0	**Power Off Event Caused By Total Power Limit**. In manual mode, write 1 to clear the bit.
2	W1C	0	**Temperature Threshold Event**. In manual mode, write 1 to clear the bit.

Bit #	R/W	Default	Description
1	W1C	0	**Voltage Threshold Event**. In manual mode, write 1 to clear the bit.
0	W1C	0	**Current Threshold Event**. In manual mode, write 1 to clear the bit.
7:0	W1C	0x00	Port 1 Status 0
7:0	W1C	0x00	Port 1 Status 1
7:0	W1C	0x00	Port 2 Status 0
7:0	W1C	0x00	Port 2 Status 1
7:0	W1C	0x00	Port 3 Status 0
7:0	W1C	0x00	Port 3 Status 1
7:0	W1C	0x00	Port 4 Status 0
7:0	W1C	0x00	Port 4 Status 1
7:0	W1C	0x00	Port 5 Status 0
7:0	W1C	0x00	Port 5 Status 1
7:0	W1C	0x00	Port 6 Status 0
7:0	W1C	0x00	Port 6 Status 1
7:0	W1C	0x00	Port 7 Status 0
7:0	W1C	0x00	Port 7 Status 1

- **Port Power Status Register @ 0x60 of Page 0**

Bit #	R/W	Default	Description
7:0	R	0x00	**Power Status of the Ports**. 0 = power off. 1 = power on. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

- **Port MPS Present Status Register @ 0x61 of Page 0**

Bit #	R/W	Default	Description
7:0	R	0x00	**MPS Status of the Ports**. 0 = MPS not present. 1 = MPS present Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

- **Port Interrupt Status Mask 0 Register @ 0x62 of Page 0**

Bit #	R/W	Default	Description
7	R/W	0	**Power Deny Mask**. In manual mode, when mask bit is 0, no interrupt will be issued for this event.
6	R/W	0	**Power Up Suspend Mask**.
5	R/W	0	**Severe Short Circuit Event Mask**.
4	R/W	0	**Thermal Shutdown Event Mask**.
3	R/W	0	**Voltage Bad to GND Event Mask**.
2	R/W	0	**MPS (DC Disconnect) Event Mask**.
1	R/W	0	**Short Circuit Limit (I_{LIM}) Event Mask**.
0	R/W	0	**Overload (I_{CUT}) Event Mask**.

- **Port Interrupt Status Mask 1 Register @ 0x63 of Page 0**

Bit #	R/W	Default	Description
7	R/W	0	**Power Off Event Caused By Max Pairset Power Mask**. In manual mode mode, when mask bit is 0, no interrupt will be issued for this event.
6	R/W	0	**Power Off Event Caused By Auto Class Power Limit Mask**.
5	R/W	0	**Power Off Event Caused By Total Power Bank Limit Mask**.
4	R/W	0	**Power Off Event Caused By High Priority Port Power Up Mask**.

Bit #	R/W	Default	Description
3	R/W	0	**Power Off Event Caused By Total Power Limit Mask**.
2	R/W	0	**Temperature Threshold Event Mask**.
1	R/W	0	**Voltage Threshold Event Mask**.
0	R/W	0	**Current Threshold Event Mask**.

- **Port Interrupt Status Mask 0 Register @ 0x64 of Page 0**

Bit #	R/W	Default	Description
7	R/W	0	**Bank Changed Event Mask**. In manual mode, when mask bit is 0, no interrupt will be issued for this event.
6	R/W	0	**Port Disabled Event Mask**.
5	R/W	0	**System Overload Event Mask**.
4	R/W	0	**PSE Current/Power Overload Event Mask**.
0	R/W	0	**System Initialization Complete Event Mask**

- **Port 0~7 Invalid Signature Counter Registers @ 0xC0~0xC7 of Page 1**

Bit #	R/W	Default	Description
7:0	R	0x00	**Port 0 Invalid Signature Counter.** Number of times the port encounters an “Invalid Signature” in detection process.
7:0	R	0x00	**Port 1 Invalid Signature Counter.**
7:0	R	0x00	**Port 2 Invalid Signature Counter.**
7:0	R	0x00	**Port 3 Invalid Signature Counter.**
7:0	R	0x00	**Port 4 Invalid Signature Counter.**
7:0	R	0x00	**Port 5 Invalid Signature Counter.**
7:0	R	0x00	**Port 6 Invalid Signature Counter.**
7:0	R	0x00	**Port 7 Invalid Signature Counter.**

- **Port 0~7 Power Denied Counter Registers @ 0xC8~0xCF of Page 1**

Bit #	R/W	Default	Description
7:0	R	0x00	**Port 0 Power Denied Counter.** Number of times the port encounters a “Power Denied” in classification process.
7:0	R	0x00	**Port 1 Power Denied Counter.**
7:0	R	0x00	**Port 2 Power Denied Counter.**
7:0	R	0x00	**Port 3 Power Denied Counter.**
7:0	R	0x00	**Port 4 Power Denied Counter.**
7:0	R	0x00	**Port 5 Power Denied Counter.**
7:0	R	0x00	**Port 6 Power Denied Counter.**
7:0	R	0x00	**Port 7 Power Denied Counter.**

5.9 Total Current/Power Limit

When the IVT is polled, the port currents are summed up to get the total current consumption. And total current could calculate total power consumption by supply voltage. Total current/power limit Register can be specified and checked against the total current/power consumption. When this total current/voltage limit is exceeded, the last port powered on would be turned off. The total current/power limitis by default disabled and can be enabled by using the Total Current/Power Limit ControlRegister. The total current/power limit is specified in the PSE Available Current/Power Registers.

IP8008 have OverloadLED threshold register, when the PSE consumed current/power is more that the Overload LED Threshold, the Overload LED will be turn on. Please refer to the section 5.10 for LED interfaceDisplay setting description

- **Power Registers @ 0xDE of Page 0**

Bit #	R/W	Default	Description
6:0	R/W	0x00	[6] ~ Priority Power Up Enable (Port with low priority powered off) [5] ~ Power Off All Pairs of Port with Dual Signature 0 = Only the Pairs with violating condition. 1 = All Pairs [4] ~ Power Off Next Port After Current Updating [1] ~ Power Limiter or Current Limiter 0 = Select Power Limiter 1 = Select Current Limiter [0] ~ Enable Total Current/Power Limiter

- **Victim Strategy of Power off Port Registers @ 0xDF of Page 0**

Bit #	R/W	Default	Description
2:0	R/W	000	**Victim Strategy** 0 = Last Port Powered 1 = First Port Powered 2 = Port With The Lowest Current 3 = Port With The Highest Current 4 = Priority

- **PSE Available Current / Power Port Registers @ 0xE8~0xE9 of Page 0**

Bit #	R/W	Default	Description
4:0	R/W	0x00	**PSE Available Current / Power MSB** (13-bit integer, mA for Current) (11-bit integer, 2-bit fraction, W, for Power) (Power off threshold)
7:0	R/W	0x00	**PSE Available Current / Power LSB**

- **PSE Consumed Current Port Registers @ 0xD2~0xD3 of Page 0**

Bit #	R/W	Default	Description
5:0	R	0x00	**PSE Consumed Current MSB** (12-bit integer, 2-bit fraction mA for Current)
7:0	R	0x00	**PSE Consumed Current MSB**

- **PSE Consumed Power Port Registers @ 0xD4~0xD5 of Page 0**

Bit #	R/W	Default	Description
5:0	R	0x00	**PSE Consumed Power MSB** (10-bit integer, 4-bit fraction, W, for Power)
7:0	R	0x00	**PSE Consumed Power MSB**

- **PSE Overload LED Threshold Registers @ 0xD9~0xDA of Page 1**

Bit #	R/W	Default	Description
5:0	R/W	0x00	**PSE Overload LED Threshold MSB** (14-bit integer, mA for Current) (12-bit integer, 2-bit fraction, W, for Power)
7:0	R/W	0x00	**PSE Overload LED Threshold LSB**

5.10 LED Interface

In auto mode or manual mode, the LED interface can hook up with an IP403 (Serial-to-Parallel LED driver) to display the port status. A port status LED is lit up when IP8008 allocates power to the port.

LED interface is enabled by pulling up LED_DAT pin with a resister. One IP8008 can handle 8 LEDs and up to three IP8008s can share one IP403, where one IP8008 serves as the master to drive LED_CLK and the others are slaves. AD2 pin defines IP8008 to be a master or a slave. The index counter in all IP8008s counts from 0 to 55 repeatly with LED_CLK after reset and the value of index counter in all IP8008 are identical. An IP8008 will send out 8-bit LED information on LED_DAT when its index counter reaches start index defined in start index register (0xD0). The detail is illustrated in the LED start index register (0xD0) and figure 6.

If there is only one IP8008, user can replace IP403 with a 74LV164 to display port status for cost saving. IP8008 should be configured as a master.

- **Port LED Pattern Order @ 0xD0 of Page 1**

Bit #	R/W	Default	Description
7	R/W	1	**LED Order**. The order in which 8-bit LED information is shifted out. 0 = From Port0, Port1, …. Port7. 1 = From Port7, Port6, …. Port0.
6	R/W	0	**LED Active Level**. 0 = light up a LED by driving logic low 1 = light up a LED by driving logic high
5	R/W	1	**LED Initial Level**. The initial level of the LED. After reset, the LED will be driven to this initial value.
4	R/W	0/1	**Serial LED Master Device**. 0 = slave. IP8008 receives LED clock on LED_CLK pin. 1 = master. IP8008 drives LED_CLK pin. The default value of this bit is latched from AD2 pin.
3:2	R/W	1	**Serial LED Clock Frequency Select**. Clock rate of the LED clock. 0 = LED clock is 500k Hz 1 = LED clock is 1M Hz 2,3 = LED clock is 2M Hz
1	R	0	**Reserved**.
0	R/W	0/1	**LED Interface Enable**. Enable the LED interface. 0 = disable, 1 = enable. The default value of this bit is latched from LED_DAT pin.

➢ **LED Start Index Register @ 0xD4 of Page 1**

<table>
<tr><th>Bit #</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7:0</td><td>R/W</td><td></td><td>LED Start Index.
There are 4 default values can be selected with I^{2}C address pin AD3 ~ AD0.
<table>
<tr><th>AD3~AD0</th><th>default value of bit [7:0]</th></tr>
<tr><td>0,1,0,0(master)</td><td>0x30h (48d)</td></tr>
<tr><td>0,0,0,0(slave)</td><td>0x28h (40d)</td></tr>
<tr><td>0,0,0,1(slave)</td><td>0x20h (32d)</td></tr>
<tr><td>0,0,1,0(slave)</td><td>0x18h (24d)</td></tr>
<tr><td>0,0,1,1(slave)</td><td>0x10h (16d)</td></tr>
<tr><td>0,1,0,1(slave)</td><td>0x08h (08d)</td></tr>
</table>

The following table demostrates the LED applications for 1~3 IP8008.
<table>
<tr><th>3 x IP8008</th><th>Master</th><th>Slave1</th><th>Slave2</th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>0x20h</td></tr>
<tr><td>AD3~AD0</td><td>0,1,0,0</td><td>0,0,0,0</td><td>0,0,0,1</td></tr>
<tr><th>2 x IP8008</th><th>Master</th><th>Slave1</th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>--</td></tr>
<tr><td>AD3~AD0</td><td>0,1,0,0</td><td>0,0,0,0</td><td>--</td></tr>
<tr><th>1 x IP8008</th><th>Master</th><th></th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>--</td><td>--</td></tr>
<tr><td>AD3~AD0</td><td>0,1,0,0</td><td>--</td><td>--</td></tr>
</table>

In manual mode, because AD0~AD3 is used for I^{2}C address at the same time, the default setting of LED starts index may be incorrect. User has to correct the LED start index by writing this register to make sure that IP8008 can send out LED status correctly.

There is an alternative for LED implementation if there is a MCU in the system. The MCU reads the port status of IP8008 through I^{2}C and write the LED information to IP403, where IP403 works as a GPIO controller not a serial-to-parallel LED driver. Because LED is handled by MCU itself, the start index in IP8008 can be ignored.</td></tr>
</table>

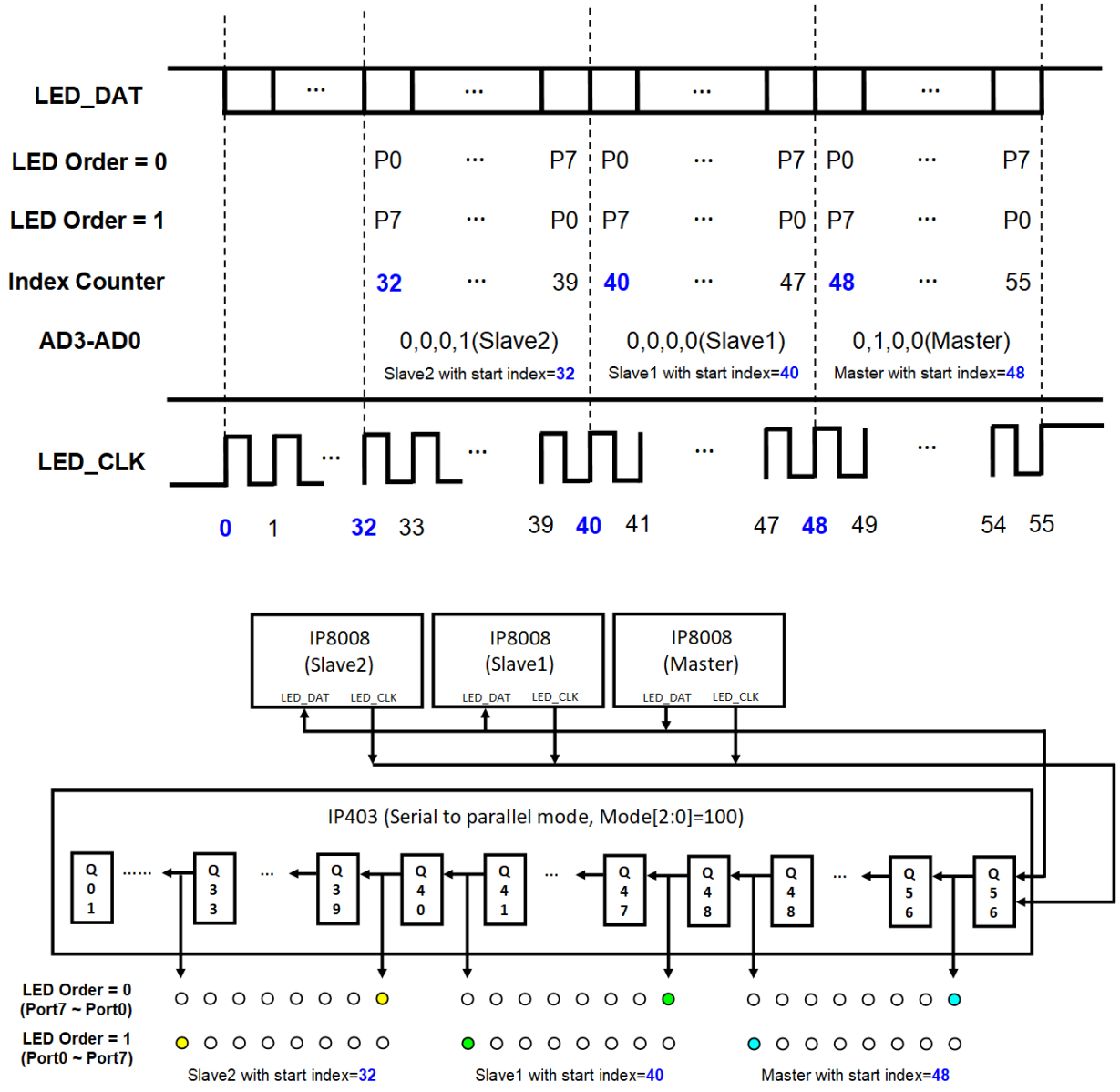


Figure 8 LED behavior and system diagram of multiple IP8008 application

- **Port LED Flash @ Page 1**

Bit #	Address	Default	Description
6:0	D1	0x00	Port LED Control [5] ~ Enable Port LED Flash for Thermal Event [4] ~ Enable Port LED Flash for Voltage Bad Event [3] ~ Enable Port LED Flash for Short Circuit Event [2] ~ Enable Port LED Flash for ICut Event [1] ~ Enable Port LED Flash for Temperature Overheat Event [0] ~ Enable Port LED Flash for Current/power Overload Event
7:0	D2	0x90	[7] ~ Disable LED Diagnostic Flash [5:4] ~ LED Diagnostic Flash Time Select 0 = 1s, 1 = 2s, 2 = 3s, 3 = 4s [2:0] ~ Port LED Flash Times Select 0 = disable, 1 = 1 time, 2 = 3 times, 3 = 5 times, 2 = 7 times, 5 = 9 times, 6 = 11 times, 7 = 13 times
5:0	D9	0x06	PSE Overload LED Threshold MSB
7:0	DA	0x60	PSE Overload LED Threshold LSB (14-bit integer, mA for Current) (12-bit integer, 2-bit fraction, W, for Power)
4:0	DB	0x06	[4:0] ~ PSE Temperature Overheat Threshold MSB
7:0	DC	0x40	[7:0] ~ PSE Temperature Overheat Threshold LSB

- **PSE Warning LED Flash @ Page 1**

Bit #	Address	Default	Description
3:0	D3	0x00	PSE Warning LED Control [3:1] ~ PSE Warning LED Display Mode 0 = Light (Current Overload) 1 = Light (Temp Overheat) 2 = Flash (Current Overload) 3 = Flash (Temperature Overload) 4 = Light (Current Overload), Flash (Temperature Overheat) 5 = Light (Temperature Overload), Flash (Current Overload) [0] ~ Enable PSE Warning LED
7:0	D5	0x2F	[5:0] ~ PSE Warning LED Start Index
7:0	D8	0x80	[7] ~ System Warning Target Threshold Select 0 = Current, 1 = Power [6:4] ~ System Warning LED1 Display Mode (no temp) [2:0] ~ System Warning LED0 Display Mode (no temp)

6 IP8008 Register descriptions

➢ **Register Map**

Page #	Register Address & Attribute		Register Name	Default Value
I2C Interface Registers				
0	00	R/W	[7:6] ~ Register Page. [3:0] ~ I^2C LSB Device Address	(00xx,PPPP)
0	01	R/W	Device ID[15:8]	(0011,1000) (0011,0100) (0010,1000)
0	02	R/W	Device ID[7:0]	(0000,0001)
0	03	R	System Configuration [7:6] ~ Operating Mode 0 = Auto Mode, 1 = Manual Mode [5] ~ LED Mode [4] ~ Cascade Mode [3:0] ~ Power Bank	(PPPP,PPPP)
0	04	R/W	[5] ~ Enable I2C Bus Checksum Checker [4] ~ Fast Simulation Enable [0] ~ Software Reset	(xx00,xxx0)
0	05	R/W	Scratch Register	(0000,0000)
0	06	R/W	Watch Dog Timer [7] ~ Enable Watch Dog Timer [6:0] ~ Watchdog Timer (unit: 100ms)	(0111,1111)
0	07	R/W	BT Mode 0 = AT/AF Mode 1 = BT Mode # Before the mode is changed; the related port should be disabled.	(xxxx,1111)
0	08	R/W	Primary Port Indicator 0 = Secondary Port 1 = Primary Port (writable only when 0C[0] = 1)	(0101,0101)
0	09	R/W	AT / AF Mode 0 = AF Mode 1 = AT Mode	(1111,1111)
0	0A	R/W	Alternative A/B 0 = Alternative A 1 = Alternative B	(0000,0000)
0	0B	R		
0	0C	R/W	[1] ~ Enable Power Bank Limiter [0] ~ Disable Primary/Secondary Port Auto Crossover	(xxxx,xx00)
0	0D	R/W	[2] ~ Force Auto Class Enable [1] ~ Auto Class Enable [0] ~ Enable Full Class Event	(xxxx,x000)
Port Power Control				
0	10	R/W	Port 0 Power Control [4] ~ Enable Power Up Suspend [3:2] ~ PSE Initial State in the Auto Mode	(xxx0,0100)

Page #	Register Address & Attribute		Register Name	Default Value
			0 = PSE Disable 1 = PSE Enable 2 = PSE Force Power On 3 = PSE Skip Classification [1:0] ~ PSE Enable 0 = PSE Disable 1 = PSE Enable 2 = PSE Force Power On 3 = PSE Skip Classification	
0	11	R/W	Port 1 Power Control	(xxx0,0100)
0	12	R/W	Port 2 Power Control	(xxx0,0100)
0	13	R/W	Port 3 Power Control	(xxx0,0100)
0	14	R/W	Port 4 Power Control	(xxx0,0100)
0	15	R/W	Port 5 Power Control	(xxx0,0100)
0	16	R/W	Port 6 Power Control	(xxx0,0100)
0	17	R/W	Port 7 Power Control	(xxx0,0100)
Detection / Connection Check Result				
0	20	R/W	[5:4] ~ SIG_{CXN} for Port 0 0 = Invalid 1 = Alternative A/B 2 = Single Signature 3 = Dual Signature [2:0] ~ R_{DET} for Port 0 0 = Bad 1 = Good 2 = Open 3 = Short 4 = C Too Large 5 = R Too Low 6 = R Too High	(xx00,x000)
0	21	R/W	[5:4] ~ SIG_{CXN} for Port 1 [2:0] ~ R_{DET} for Port 1	(xx00,x000)
0	22	R/W	[5:4] ~ SIG_{CXN} for Port 2 [2:0] ~ R_{DET} for Port 2	(xx00,x000)
0	23	R/W	[5:4] ~ SIG_{CXN} for Port 3 [2:0] ~ R_{DET} for Port 3	(xx00,x000)
0	24	R/W	[5:4] ~ SIG_{CXN} for Port 4 [2:0] ~ R_{DET} for Port 4	(xx00,x000)
0	25	R/W	[5:4] ~ SIG_{CXN} for Port 5 [2:0] ~ R_{DET} for Port 5	(xx00,x000)
0	26	R/W	[5:4] ~ SIG_{CXN} for Port 6 [2:0] ~ R_{DET} for Port 6	(xx00,x000)
0	27	R/W	[5:4] ~ SIG_{CXN} for Port 7 [2:0] ~ R_{DET} for Port 7	(xx00,x000)
PD Requested Class / Auto Class Status				
0	28	R	[4] ~ Auto Class Status of Port 0 [3:0] ~ PD Requested Class of Port 0 0~8 = PD Requested Class 9 = Class Signature Error	(xxx0,1111)

Page #	Register Address & Attribute		Register Name	Default Value
			A = Class Error F = Initial Class	
0	29	R	[4] ~ Auto Class Status of Port 1 [3:0] ~ PD Requested Class of Port 1	(xxx0,1111)
0	2A	R	[4] ~ Auto Class Status of Port 2 [3:0] ~ PD Requested Class of Port 2	(xxx0,1111)
0	2B	R	[4] ~ Auto Class Status of Port 3 [3:0] ~ PD Requested Class of Port 3	(xxx0,1111)
0	2C	R	[4] ~ Auto Class Status of Port 4 [3:0] ~ PD Requested Class of Port 0	(xxx0,1111)
0	2D	R	[4] ~ Auto Class Status of Port 5 [3:0] ~ PD Requested Class of Port 5	(xxx0,1111)
0	2E	R	[4] ~ Auto Class Status of Port 6 [3:0] ~ PD Requested Class of Port 6	(xxx0,1111)
0	2F	R	[4] ~ Auto Class Status of Port 7 [3:0] ~ PD Requested Class of Port 7	(xxx0,1111)
PD Allocated Class Status				
0	30	R	PD Allocated Class of of Port0 Based on PSE total power for per port and PD request class to define the PD currect classification. 0001: Class1 0010: Class2 0011: Class3 0100: Class4 0101: Class5 0110: Class6 0111: Class7 1000: Class8 1111 : Initial Class (Note: if PD requested class0 , PSE allocate class3)	(xxxx,1111)
0	31	R	[3:0] ~ PD Allocated Class of Port 1	(xxxx,1111)
0	32	R	[3:0] ~ PD Allocated Class of Port 2	(xxxx,1111)
0	33	R	[3:0] ~ PD Allocated Class of Port 3	(xxxx,1111)
0	34	R	[3:0] ~ PD Allocated Class of Port 4	(xxxx,1111)
0	35	R	[3:0] ~ PD Allocated Class of Port 5	(xxxx,1111)
0	36	R	[3:0] ~ PD Allocated Class of Port 6	(xxxx,1111)
0	37	R	[3:0] ~ PD Allocated Class of Port 7	(xxxx,1111)
Power On & Interrupt Events				
0	60	R	Port Power Status	(0000,0000)
0	61	R	Port MPS Present Status	(1111,1111)
0	62	R/W	Port Interrupt Status Mask 0 [7] ~ Power Deny Mask [6] ~ Power Up Suspend Mask [5] ~ Severe Short Circuit Event Mask [4] ~ Thermal Shutdown Event Mask [3] ~ Voltage Bad Event Mask [2] ~ MPS Error Event Mask [1] ~ Short Circuit Limit Event Mask [0] ~ Overload Event Mask	(0000,0000)

Page #	Register Address & Attribute		Register Name	Default Value
0	63	R/W	Port Interrupt Status Mask 1 [7] ~ Power Off Event Caused By Max Pairset Power Limit Mask [6] ~ Power Off Event Caused By Auto Class Power Limit Mask [5] ~ Power Off Event Caused By Power Bank Limit Mask [4] ~ Power Off Event Caused By High Priority Port Power Up Mask. [3] ~ Power Off Caused By Total Power Limiter Event Mask [2] ~ Temperature Limit Event Mask [1] ~ Voltage Limit Event Mask [0] ~ Current Limit Event Mask	(0000,0000)
0	64	R/W	Port Interrupt Mask	(0000,0000)
0	65	R	Port Interrupt Status	(0000,0000)
0	66	R/W	System Interrupt Status Mask [7] ~ Bank Changed Event Mask [6] ~ Port Disabled Event Mask [5] ~ System Power Overload Event Mask [4] ~ PSE Current/Power Overload Event Mask [0] ~ System Initialization Complete Event Mask	(0000,xxx0)
0	67	R/ W1C	System Status [7] ~ Bank Changed Event [6] ~ Port Disable Event (error come from PORT_DISABLE of analog) [5] ~ System Current/Power Overload Event (system consumed power > system available power) [4] ~ PSE Current/Power Overload Event (PSE consumed power > PSE available power) [2] ~ No EEPROM [1] ~ EPROM Load Error [0] ~ System Initialization Complete	(0000,x000)
0	68	R/W	Interrupt Event Handler [7] ~ Temperature Limit Event Handler [6] ~ Voltage Limit Event Handler [5] ~ Current Limit Event Handler [3] ~ Voltage Bad Event Handler	(000x,1xxx)
0	6A	R/W	Port Power Up Suspend Control 1 = Start Power Up (Auto Clear) # writable only when power up suspend status assert.	(0000,0000)
0	6B	R/W	Port Step by Step Operation 1 = Next Step (Auto Clear)	(0000,0000)
0	6C	R/W	[3:2] ~ Power Allocation Mode 1 = Class Power [1:0] ~ PSE Allocated Power Estimation Mode 0 = PSE Idea Class Power 1 = PSE Real Consumed Power 2 = PSE Max Consumed Power 3 = PSE Real Consumed Power and Auto Class Power	(xxxx,0100)
0	6D	R		

Page #	Register Address & Attribute		Register Name	Default Value
0	6E	R	Port Power Up Suspend Status	(0000,0000)
0	6F	R/W	[2] ~ Auto Clear Temperature Limit Event Enable [1] ~ Auto Clear Voltage Limit Event Enable [0] ~ Auto Clear Current Limit Event Enable	(xxxx,x111)
			Port Status	
0	70	R W1C	Port 0 Status 0 [7] ~ Power Deny [6] ~ Power Up Suspend [5] ~ Severe Short Circuit Event (E_{SC}) [4] ~ Thermal Shutdown Event (Etsd) [3] ~ Voltage Bad Event (Evg) [2] ~ MPS Error Event (Edis) [1] ~ Short Circuit Limit Event (I_{LIM}) [0] ~ Overload Current Event (I_{CUT})	(0000,0000)
0	71	R W1C	Port 0 Status 1 [7] ~ Power Off Event Caused By Max Pairset Power Limit [6] ~ Power Off Event Caused By Auto Class Power Limit [5] ~ Power Off Event Caused By Power Bank Limit [4] ~ Power Off Event Caused By High Priority Port Power Up. [3] ~ Power Off Event Caused By Total Power Limit [2] ~ Temperature Threshold Event (IVT) [1] ~ Voltage Threshold Event (IVT) [0] ~ Current Threshold Event (IVT)	(0000,0000)
0	72	W1C	Port 1 Status 0	(0000,0000)
0	73	W1C	Port 1 Status 1	(0000,0000)
0	74	W1C	Port 2 Status 0	(0000,0000)
0	75	W1C	Port 2 Status 1	(0000,0000)
0	76	W1C	Port 3 Status 0	(0000,0000)
0	77	W1C	Port 3 Status 1	(0000,0000)
0	78	W1C	Port 4 Status 0	(0000,0000)
0	79	W1C	Port 4 Status 1	(0000,0000)
0	7A	W1C	Port 5 Status 0	(0000,0000)
0	7B	W1C	Port 5 Status 1	(0000,0000)
0	7C	W1C	Port 6 Status 0	(0000,0000)
0	7D	W1C	Port 6 Status 1	(0000,0000)
0	7E	W1C	Port 7 Status 0	(0000,0000)
0	7F	W1C	Port 7 Status 1	(0000,0000)
			IVT Poll Control	
0	80	R/W	[7:0] ~ Forced IVT Port (ForceIVT)	(0000,0000)
0	81	R/W	[7] ~ IVT on Processing [4] ~ Auto Polling [3:0] ~ IVT Poll Interval (unit : 1mS)	(0xx1,0000)
0	82	R/W	[2:0] ~ IVT Sample Port	(xxxx,x000)
0	83	R	Supply Voltage Sample MSB	(xxxx,xx00)
0	84	R	Supply Voltage Sample LSB	(0000,0000)
0	85	R	Port Current Sample MSB	(xxxx,xx00)
0	86	R	Port Current Sample LSB	(0000,0000)

Page #	Register Address & Attribute		Register Name	Default Value
0	87	R	Port Voltage Sample MSB	(xxxx,xx00)
0	88	R	Port Voltage Sample LSB	(0000,0000)
0	89	R	Port Temperature Sample MSB	(xxxx,xx00)
0	8A	R	Port Temperature Sample LSB	(0000,0000)
0	8B	R/W	MSB of Temperature Display Offset	(0000,0000)
0	8C	R/W	LSB of Temperature Display Offset (1-bit sign, 7-bit integer, 1-bit fraction)	(xx,xxxx)
Supply Voltage				
0	8E	R	Supply Voltage MSB	(xxxx,0000)
0	8F	R	Supply Voltage LSB (8-bit integer, 4-bit fraction, unit: V)	(0000,0000)
Port Current				
0	90	R	Port 0 Current MSB	(xxxx,0000)
0	91	R	Port 0 Current LSB (**11-bit integer**, 2-bit fraction, unit: mA)	(0000,0000)
0	92	R	Port 1 Current MSB	(xxxx,0000)
0	93	R	Port 1 Current LSB	(0000,0000)
0	94	R	Port 2 Current MSB	(xxxx,0000)
0	95	R	Port 2 Current LSB	(0000,0000)
0	96	R	Port 3 Current MSB	(xxxx,0000)
0	97	R	Port 3 Current LSB	(0000,0000)
0	98	R	Port 4 Current MSB	(xxxx,0000)
0	99	R	Port 4 Current LSB	(0000,0000)
0	9A	R	Port 5 Current MSB	(xxxx,0000)
0	9B	R	Port 5 Current LSB	(0000,0000)
0	9C	R	Port 6 Current MSB	(xxxx,0000)
0	9D	R	Port 6 Current LSB	(0000,0000)
0	9E	R	Port 7 Current MSB	(xxxx,0000)
0	9F	R	Port 7 Current LSB	(0000,0000)
Port Voltage				
0	A0	R	Port 0 Voltage MSB	(xxxx,0000)
0	A1	R	Port 0 Voltage LSB (8-bit integer, 4-bit fraction, unit: V)	(0000,0000)
0	A2	R	Port 1 Voltage MSB	(xxxx,0000)
0	A3	R	Port 1 Voltage LSB	(0000,0000)
0	A4	R	Port 2 Voltage MSB	(xxxx,0000)
0	A5	R	Port 2 Voltage LSB	(0000,0000)
0	A6	R	Port 3 Voltage MSB	(xxxx,0000)
0	A7	R	Port 3 Voltage LSB	(0000,0000)
0	A8	R	Port 4 Voltage MSB	(xxxx,0000)
0	A9	R	Port 4 Voltage LSB	(0000,0000)
0	AA	R	Port 5 Voltage MSB	(xxxx,0000)
0	AB	R	Port 5 Voltage LSB	(0000,0000)
0	AC	R	Port 6 Voltage MSB	(xxxx,0000)
0	AD	R	Port 6 Voltage LSB	(0000,0000)
0	AE	R	Port 7 Voltage MSB	(xxxx,0000)
0	AF	R	Port 7 Voltage LSB	(0000,0000)
Port Temperature				

Page #	Register Address & Attribute		Register Name	Default Value
0	B0	R	Port 0 Temperature MSB	(xxx0,0000)
0	B1	R	Port 0 Temperature LSB (9-bit integer, 4-bit fraction, unit: C)	(0000,0000)
0	B2	R	Port 1 Temperature MSB	(xxx0,0000)
0	B3	R	Port 1 Temperature LSB	(0000,0000)
0	B4	R	Port 2 Temperature MSB	(xxx0,0000)
0	B5	R	Port 2 Temperature LSB	(0000,0000)
0	B6	R	Port 3 Temperature MSB	(xxx0,0000)
0	B7	R	Port 3 Temperature LSB	(0000,0000)
0	B8	R	Port 4 Temperature MSB	(xxx0,0000)
0	B9	R	Port 4 Temperature LSB	(0000,0000)
0	BA	R	Port 5 Temperature MSB	(xxx0,0000)
0	BB	R	Port 5 Temperature LSB	(0000,0000)
0	BC	R	Port 6 Temperature MSB	(xxx0,0000)
0	BD	R	Port 6 Temperature LSB	(0000,0000)
0	BE	R	Port 7 Temperature MSB	(xxx0,0000)
0	BF	R	Port 7 Temperature LSB	(0000,0000)
Port Consumed Power				
0	C0	R	Port 0 Consumed Power MSB	(xxxx,x000)
0	C1	R	Port 0 Consumed Power LSB (7-bit Integer, 4-bit fraction, W)	(0000,0000)
0	C2	R	Port 1 Consumed Power MSB	(xxxx,x000)
0	C3	R	Port 1 Consumed Power LSB	(0000,0000)
0	C4	R	Port 2 Consumed Power MSB	(xxxx,x000)
0	C5	R	Port 2 Consumed Power LSB	(0000,0000)
0	C6	R	Port 3 Consumed Power MSB	(xxxx,x000)
0	C7	R	Port 3 Consumed Power LSB	(0000,0000)
0	C8	R	Port 4 Consumed Power MSB	(xxxx,x000)
0	C9	R	Port 4 Consumed Power LSB	(0000,0000)
0	CA	R	Port 5 Consumed Power MSB	(xxxx,x000)
0	CB	R	Port 5 Consumed Power LSB	(0000,0000)
0	CC	R	Port 6 Consumed Power MSB	(xxxx,x000)
0	CD	R	Port 6 Consumed Power LSB	(0000,0000)
0	CE	R	Port 7 Consumed Power MSB	(xxxx,x000)
0	CF	R	Port 7 Consumed Power LSB	(0000,0000)
PSE Allocated Power				
0	D0	R	[7:0] ~ PSE Allocated Power MSB	(0000,0000)
0	D1	R	[7:0] ~ PSE Allocated Power LSB (The PSE allocated power is calculated based on PSE power estimation mode, page0_6C[1:0]) (12-bit integer, 4-bit fraction, W)	(0000,0000)
PSE Consumed Current				
0	D2	R	[6:0] ~ PSE Consumed Current MSB	(0000,0000)
0	D3	R	[7:0] ~ PSE Consumed Current LSB (13-bit integer, 2-bit fraction, mA)	(0000,0000)
PSE Consumed Power				
0	D4	R	[5:0] ~ PSE Consumed Power MSB	(0000,0000)
0	D5	R	[7:0] ~ PSE Consumed Power LSB	(0000,0000)

Page #	Register Address & Attribute		Register Name	Default Value
			(10-bit integer, 4-bit fraction, W)	
			Max PSE Consumed Power	
0	D6	R/WC	[5:0] ~ Max PSE Consumed Power MSB	(0000,0000)
0	D7	R/WC	[7:0] ~ Max PSE Consumed Power LSB (10-bit integer, 4-bit fraction, W)	(0000,0000)
			Power Trunk Control	
0	D8	R/W	[0] ~ Trunk Select	(xxxx,xxx0)
0	D9	R/W	[1:0] ~ Trunk 0 Power Limit MSB	(xxxx,xx01)
0	DA	R/W	[7:0] ~ Trunk 0 Power Limit LSB (10-bit integer, W)	(0111,1100)
0	DB	R/W	[1:0] ~ Trunk 1 Power Limit MSB	(xxxx,xx01)
0	DC	R/W	[7:0] ~ Trunk 1 Power Limit LSB	(0111,1100)
			Total Current / Power Limiter	
0	DE	R/W	[6] ~ Priority Power Up Enable (Port with low priority powered off) [5] ~ Power Off All Pairs of Port with Dual Signature 0 = Only the Pairs with violating condition. 1 = All Pairs [4] ~ Power Off Next Port After Current Updating [1] ~ Power Limiter or Current Limiter 0 = Enable Power Limiter 1 = Enable Current Limiter [0] ~ Enable Total Current/Power Limiter	(x000,0000)
0	DF	R/W	[2:0] ~ Victim Strategy 0 = Last Port Powered 1 = First Port Powered 2 = Port With The Lowest Current 3 = Port With The Highest Current 4 = Priority	(xxxx,x000)
			PSE Available Current / Power	
0	E8	R/W	[6:0] ~ PSE Available Current / Power MSB	(x001,1111)
0	E9	R/W	[7:0] ~ PSE Available Current / Power LSB (13-bit integer, mA for Current) (10-bit integer, 2-bit fraction, W, for Power) (Power off threshold)	(1111,0000)
			System Power Limit	
0	EA	R/W	[4:0] ~ System Power Limit MSB	(xxx0,1110)
0	EB	R/W	[7:0] ~ System Power Limit LSB (13-bit integer, W) (System power on threshold)	(1010,0110)
			System Consumed Power	
0	EC	R/W	[4:0] ~ System Consumed Power MSB	(xxx0,0000)
0	ED	R/W	[7:0] ~ System Consumed Power LSB (13-bit integer, W) (The value is calculated based on the PSE power estimation mode of each chip)	(0000,0000)
			System Available Power	
0	EE	R/W	[4:0] ~ System Available Power MSB	(xxx0,1110)

Page #	Register Address & Attribute		Register Name	Default Value
0	EF	R/W	[7:0] ~ System Available Power LSB (13-bit integer, W) (System power off threshold)	(1010,0110)
			PD Allocated Power	
0	F0	R	[7:0] ~ PD Allocated Power of Port 0 (6-bit Integer, 2-bit Fraction)	(0000,0000)
0	F1	R	[7:0] ~ PD Allocated Power of Port 1	(0000,0000)
0	F2	R	[7:0] ~ PD Allocated Power of Port 2	(0000,0000)
0	F3	R	[7:0] ~ PD Allocated Power of Port 3	(0000,0000)
0	F4	R	[7:0] ~ PD Allocated Power of Port 4	(0000,0000)
0	F5	R	[7:0] ~ PD Allocated Power of Port 5	(0000,0000)
0	F6	R	[7:0] ~ PD Allocated Power of Port 6	(0000,0000)
0	F7	R	[7:0] ~ PD Allocated Power of Port 7	(0000,0000)
			Auto Class Power Limit	
0	F8	R	[3:0] ~ Port 0 / Port 1 Auto Class Power Limit MSB	(0000,0000)
0	F9	R	[7:0] ~ Port 0 / Port 1 Auto Class Power Limit LSB 8-bit integer, 4-bit fraction, W	(0000,0000)
0	FA	R	[3:0] ~ Port 2 / Port 3 Auto Class Power Limit MSB	(0000,0000)
0	FB	R	[7:0] ~ Port 2 / Port 3 Auto Class Power Limit LSB	(0000,0000)
0	FC	R	[3:0] ~ Port 4 / Port 5 Auto Class Power Limit MSB	(0000,0000)
0	FD	R	[7:0] ~ Port 4 / Port 5 Auto Class Power Limit LSB	(0000,0000)
0	FE	R	[3:0] ~ Port 6 / Port 7 Auto Class Power Limit MSB	(0000,0000)
0	FF	R	[7:0] ~ Port 6 / Port 7 Auto Class Power Limit LSB	(0000,0000)
			Supply Voltage Limit	
1	A0	R/W	[3:0] ~ Supply Voltage Upper Limit MSB (8-bit Integer, 4-bit Fraction)	(0000,0011)
1	A1	R/W	[7:0] ~ Supply Voltage Upper Limit LSB	(1100,0000)
1	A2	R/W	[3:0] ~ Supply Voltage Lower Limit MSB	(0000,0010)
1	A3	R/W	[7:0] ~ Supply Voltage Lower Limit LSB	(1000,0000)
			Port Temperature Limit	
1	A4	R/W	[4:0] ~ Port Temperature Limit MSB (9-bit Integer, 4-bit Fraction)	(0000,1001)
1	A5	R/W	[7:0] ~ Port Temperature Limit LSB	(0110,0000)
			Port Current Limit	
1	B0	R/W	[4:0] ~ Port 0 Current Limit MSB (11-bit Integer, 2-bit Fraction)	(0000,1111)
1	B1	R/W	[7:0] ~ Port 0 Current Limit LSB	(1000,0000)
1	B2	R/W	[4:0] ~ Port 1 Current Limit MSB	(0000,1111)
1	B3	R/W	[7:0] ~ Port 1 Current Limit LSB	(1000,0000)
1	B4	R/W	[4:0] ~ Port 2 Current Limit MSB	(0000,1111)
1	B5	R/W	[7:0] ~ Port 2 Current Limit LSB	(1000,0000)
1	B6	R/W	[4:0] ~ Port 3 Current Limit MSB	(0000,1111)
1	B7	R/W	[7:0] ~ Port 3 Current Limit LSB	(1000,0000)
1	B8	R/W	[4:0] ~ Port 4 Current Limit MSB	(0000,1111)
1	B9	R/W	[7:0] ~ Port 4 Current Limit LSB	(1000,0000)
1	BA	R/W	[4:0] ~ Port 5 Current Limit MSB	(0000,1111)
1	BB	R/W	[7:0] ~ Port 5 Current Limit LSB	(1000,0000)
1	BC	R/W	[4:0] ~ Port 6 Current Limit MSB	(0000,1111)

Page #	Register Address & Attribute		Register Name	Default Value
1	BD	R/W	[7:0] ~ Port 6 Current Limit LSB	(1000,0000)
1	BE	R/W	[4:0] ~ Port 7 Current Limit MSB	(0000,1111)
1	BF	R/W	[7:0] ~ Port 7 Current Limit LSB	(1000,0000)
Invalid Signature Counter				
1	C0	R/WC	[7:0] ~ Port 0 Invalid Signature Counter	(0000,0000)
1	C1	R/WC	[7:0] ~ Port 1 Invalid Signature Counter	(0000,0000)
1	C2	R/WC	[7:0] ~ Port 2 Invalid Signature Counter	(0000,0000)
1	C3	R/WC	[7:0] ~ Port 3 Invalid Signature Counter	(0000,0000)
1	C4	R/WC	[7:0] ~ Port 4 Invalid Signature Counter	(0000,0000)
1	C5	R/WC	[7:0] ~ Port 5 Invalid Signature Counter	(0000,0000)
1	C6	R/WC	[7:0] ~ Port 6 Invalid Signature Counter	(0000,0000)
1	C7	R/WC	[7:0] ~ Port 7 Invalid Signature Counter	(0000,0000)
Power Denied Counter				
1	C8	R/WC	[7:0] ~ Port 0 Power Denied Counter	(0000,0000)
1	C9	R/WC	[7:0] ~ Port 1 Power Denied Counter	(0000,0000)
1	CA	R/WC	[7:0] ~ Port 2 Power Denied Counter	(0000,0000)
1	CB	R/WC	[7:0] ~ Port 3 Power Denied Counter	(0000,0000)
1	CC	R/WC	[7:0] ~ Port 4 Power Denied Counter	(0000,0000)
1	CD	R/WC	[7:0] ~ Port 5 Power Denied Counter	(0000,0000)
1	CE	R/WC	[7:0] ~ Port 6 Power Denied Counter	(0000,0000)
1	CF	R/WC	[7:0] ~ Port 7 Power Denied Counter	(0000,0000)
Serial LED Interface Control				
1	D0	R/W	Serial LED Interface Control [7] ~ Port LED Pattern Order [6] ~ LED Active Level [5] ~ LED Initial Level [4] ~ Serial LED Master Device [3:2] ~ Serial LED Clock Frequency Select [1] ~ Reserved [0] ~ Enable Serial LED Interface	(1011,010P)
1	D1	R/W	Port LED Control [6] ~ One LED Display for Four-Pair on BT Mode [5] ~ Enable Port LED Flash for Thermal Event [4] ~ Enable Port LED Flash for Voltage Bad Event [3] ~ Enable Port LED Flash for Short Circuit Event [2] ~ Enable Port LED Flash for ICut Event [1] ~ Enable Port LED Flash for Temperature Overheat Event [0] ~ Enable Port LED Flash for Current Overload Event	(x000,0000)
1	D2	R/W	[7] ~ Disable LED Diagnostic Flash [5:4] ~ LED Diagnostic Flash Time Select 0 = 1s, 1 = 2s, 2 = 3s, 3 = 4s [2:0] ~ Port LED Flash Times Select 0 = disable, 1 = 1 time, 2 = 3 times, 3 = 5 times, 4 = 7 times, 5 = 9 times, 6 = 11 times, 7 = 13 times	(1x01,x000)
1	D3	R/W	PSE Warning LED Control	(xxxx,0000)

Page #	Register Address & Attribute		Register Name	Default Value
			[3:1] ~ PSE Warning LED Display Mode 0 = Light (Current Overload) 1 = Light (Temp Overheat) 2 = Flash (Current Overload) 3 = Flash (Temperature Overload) 4 = Light (Current Overload), Flash (Temperature Overheat) 5 = Light (Temperature Overload) Flash (Current Overload) [0] ~ Enable PSE Warning LED	
1	D4	R/W	[5:0] ~ Port LED Start Index	(0011,0000)
1	D5	R/W	[5:0] ~ PSE Warning LED Start Index	(0010,1111)
1	D6	R/W	[5:0] ~ LED Pattern Number	(0011,0111)
1	D7	R/W	[7:2] ~ LED Flash Speed [1:0] ~ LED Refresh Time	(0101,0001)
1	D8	R/W	[7] ~ PSE Warning Target Threshold Select 0 = Current, 1 = Power (default) [6:4] ~ System Warning LED1 Display Mode [2:0] ~ System Warning LED0 Display Mode	(1000,x000)
1	D9	R/W	[5:0] ~ PSE Overload LED Threshold MSB	(x000,0110)
1	DA	R/W	[7:0] ~ PSE Overload LED Threshold LSB (14-bit integer, mA for Current) (12-bit integer, 2-bit fraction, W, for Power)	(0110,0000)
1	DB	R/W	[4:0] ~ PSE Temperature Overheat Threshold MSB	(xxx0,0110)
1	DC	R/W	[7:0] ~ PSE Temperature Overheat Threshold LSB	(0100,0000)
1	DD	R/W	[7] ~ Enable System Warning LED0 [5:0] ~ System Warning LED0 Index	(0010,1111)
1	DE	R/W	[7] ~ Enable System Warning LED1 [5:0] ~ System Warning LED1 Index	(0010,1110)
1	DF	R/W	[2] ~ Enable System Warning LED4 [1] ~ Enable System Warning LED3 [0] ~ Enable System Warning LED2	(xxxx,x000)
1	E0	R/W	[6:0] ~ System Overload LED Threshold01 MSB	(x011,1010)
1	E1	R/W	[7:0] ~ System Overload LED Threshold01 LSB (13-bit integer, 2-bit fraction, W, for Power)	(1001,1000)
1	E2	R/W	[6:0] ~ System Overload LED Threshold2 MSB	(x011,1010)
1	E3	R/W	[7:0] ~ System Overload LED Threshold2 LSB	(1001,1000)
1	E4	R/W	[6:0] ~ System Overload LED Threshold3 MSB	(x011,1010)
1	E5	R/W	[7:0] ~ System Overload LED Threshold3 LSB	(1001,1000)
1	E6	R/W	[6:0] ~ System Overload LED Threshold4 MSB	(x011,1010)
1	E7	R/W	[7:0] ~ System Overload LED Threshold4 LSB	(1001,1000)
1	E8	R/W	[6:4] ~ Port LED Event Delay (unit: 100ms) [3:2] ~ Port LED Event Type 0 = pi_powered. 1 = power_applied 2 = delayed power applied [1] ~ System Warning LED Multi-Frequency Flash [0] ~ PSE Warning LED Multi-Frequency Flash	(x100,0000)
1	E9	R/W	[7] ~ Enable Overload Threshold 01 Flash	(0000,0000)

Page #	Register Address & Attribute		Register Name	Default Value
			[5:0] ~ Flash Speed for Overload Threshold 01 (unit: 80ms)	
1	EA	R/W	[7] ~ Enable Overload Threshold 2 Flash [5:0] ~ Flash Speed for Overload Threshold 2 (unit: 80ms)	(0000,0101)
1	EB	R/W	[7] ~ Enable Overload Threshold 3 Flash [5:0] ~ Flash Speed for Overload Threshold 3 (unit: 80ms)	(0000,1010)
1	EC	R/W	[7] ~ Enable Overload Threshold 4 Flash [5:0] ~ Flash Speed for Overload Threshold 4 (unit: 80ms)	(0001,1010)
Cascade Interface Control				
2	10	R	[3:0] ~ Device Active (Device 11, … , Device 8)	(xxxx,0000)
2	11	R	[7:0] ~ Device Active (Device 7, Device 6, … , Device 1, Device 0)	(0000,0000)
2	12	R	[0] ~ My Cascade Status	(xxxx,xxx0)
2	13	R/W	[5] ~ Cascade Clock Open Drain Enable [4] ~ Cascade Bus Clock Frequency 0 = 1Mhz, 1 = 1.5Mhz [2] ~ Cascade Power Limiter Enable [1:0] ~ Power Up Mode 0 = Master controls the power-on requirement of incoming PD according to the system available power. 1 = Master controls the power-on requirement of incoming PD according to the system available power and port priority. If the incoming PD own higher priority, the PD with low priority which already power on will be powered off. 2,3 = Slave PSE control the power-on requirement of incoming PD and report the power-on status to Master.	(xx01,0000)
2	14	R/W	[3:0] ~ System Power Refresh Time (Unit : 5ms) [7:4] ~ Cascade Mode Class Evaluation Time (Unit : 0.5ms)	(0010,1000)
2	15	R		
2	16	R	[4:0] ~ System Allocated Power MSB	(xxx0,0000)
2	17	R	[7:0] ~ System Allocated Power LSB (13-bit integer, W) (The value is calculated based on the PSE power estimation mode of each chip)	(0000,0000)
2	18	R	[5:0] ~ PSE Static Power MSB	(0000,0000)
2	19	R	[7:0] ~ PSE Static Power LSB (10-bit integer, 4-bit fraction, W)	(0000,0000)
Port Power Up Sequence				
2	44	R/W	[6:4] ~ The 2nd Priority Port [2:0] ~ The Highest Priority Port	(x010,x000)

Page #	Register Address & Attribute		Register Name	Default Value
2	45	R/W	[6:4] ~ The 4th Priority Port [2:0] ~ The 3rd Priority Port	(x110,x100)
2	46	R/W	[6:4] ~ The 6th Priority Port [2:0] ~ The 5th Priority Port	(x011,x001)
2	47	R/W	[6:4] ~ The lowest Priority Port [2:0] ~ The 7th Priority Port	(x111,x101)
Port Priority				
2	48	R/W	[6:0] ~ Port 0 Priority	(x000,0111)
2	49	R/W	[6:0] ~ Port 1 Priority	(x000,0110)
2	4A	R/W	[6:0] ~ Port 2 Priority	(x000,0101)
2	4B	R/W	[6:0] ~ Port 3 Priority	(x000,0100)
2	4C	R/W	[6:0] ~ Port 4 Priority	(x000,0011)
2	4D	R/W	[6:0] ~ Port 5 Priority	(x000,0010)
2	4E	R/W	[6:0] ~ Port 6 Priority	(x000,0001)
2	4F	R/W	[6:0] ~ Port 7 Priority	(x000,0000)
Multiple Power Bank Control				
2	50	R/W	[7:0] ~ Bank 0 Power Limit (Unit: 2W)	(1111,1000)
2	51	R/W	[7:0] ~ Bank 1 Power Limit	(1111,1000)
2	52	R/W	[7:0] ~ Bank 2 Power Limit	(1111,1000)
2	53	R/W	[7:0] ~ Bank 3 Power Limit	(1111,1000)
2	54	R/W	[7:0] ~ Bank 4 Power Limit	(1111,1000)
2	55	R/W	[7:0] ~ Bank 5 Power Limit	(1111,1000)
2	56	R/W	[7:0] ~ Bank 6 Power Limit	(1111,1000)
2	57	R/W	[7:0] ~ Bank 7 Power Limit	(1111,1000)
2	58	R/W	[7:0] ~ Bank 8 Power Limit	(1111,1000)
2	59	R/W	[7:0] ~ Bank 9 Power Limit	(1111,1000)
2	5A	R/W	[7:0] ~ Bank 10 Power Limit	(1111,1000)
2	5B	R/W	[7:0] ~ Bank 11 Power Limit	(1111,1000)
2	5C	R/W	[7:0] ~ Bank 12 Power Limit	(1111,1000)
2	5D	R/W	[7:0] ~ Bank 13 Power Limit	(1111,1000)
2	5E	R/W	[7:0] ~ Bank 14 Power Limit	(1111,1000)
2	5F	R/W	[7:0] ~ Bank 15 Power Limit	(1111,1000)
I2C Timeout Selectionl				
2	9B	R/W	[1:0] ~ I2C Timeout Selection 0 = Disable 1 = 10ms, 2 = 30ms, 3 = 150ms	(xxxx,xx10)

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

(Note: Beyond these ratings can cause damage to the device)

Table 5 Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Supply Voltage	V54 – AGND	-0.3		+75	V
ChN0~ChN7	ChN– AGND @n=0~7	-0.3		+75	V
RS0~RS7	RSn – AGND @n=0~7	-0.3		+5.5	V
V5	V5 – AGND	-0.3		+5.5	V
All other Pins	All other Pin – (AGND, or DGND)	-0.3		+3.6	V
RGND, AGND	DGND – AGND	-0.3		+0.3	V
Maximum Junction Temperature				150	℃
Storage Temperature Range		-65		150	℃
Lead Temperature	Soldering 10 seconds			260	℃
ESD at all Pins	HBM	±2			KV

7.2 Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
Ta	Ambient temperature	-40		+85	℃
V54	V54~AGND @af Type1	44		57	V
	V54~AGND @at Type2	50		57	V
	V54~AGND @bt Type3	50		57	V
	V54~AGND @bt Type4	52		57	V

7.3 Electrical Characteristics for Analog I/O Pins

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V54	Power Input Supply voltage	44V~57V @af Type1	44		57	V
		50V~57V @at Type2	50		57	V
		50V~57V @bt Type3	50		57	V
		52V~57V @bt Type4	52		57	V
V_noise	Vport ripple voltage	f<500Hz			0.5	Vpp
		500Hz to 150kHz			0.2	
		150kHz to 500kHz			0.15	
		500kHz to 1MHz			0.1	
I54	V54 operating current	All ports on @w/o peripheral load current & port load current		10	18	mA
V3P3	V3P3 voltage	External Capacitance=4.7uF @short V3P3 and DV3P3	3.10	3.30	3.46	V
Iout_v3p3	En_Reg=low	V3P3 providing to peripheral device @short V3P3 and DV3P3			6	mA
Iin_v3p3	En_Reg=high	External 3.3V provides to V3P3 @short V3P3 and DV3P3	6			mA
V5	Internal use only	External Capacitance=4.7uF (Reserve footprint)	5	5.25	5.5	V

V1P8	Internal use only	External Capacitance=4.7uF	1.7	1.8	1.9	V
Port Disabled	Port Disabled Threshold	Rising V54 – AGND		30		V
		Falling V54 – AGND		27		V
V54_OVL	V54 overvoltage lockout	Rising V54 – AGND		63		V
		Falling V54 – AGND		60		V
V3P3_Rise	V3P3 Rise, Release	Rising V3P3 – AGND @short DV3P3		2.8		V
V3P3_Fall	V3P3 Fall Reset	Falling V3P3 – AGND @short DV3P3		1.9		V

7.4 IEEE802.3 af/at/bt Mode Parameters

Table 6 IEEE802.3 af/at/bt Mode Parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Detection Specifications						
Voc	Open circuit voltage	V54 – , (n=0~7) @Port open circuit			30	V
Ropen	Open circuit resistance	V54 – ChN, (n=0~7) @Port open circuit	500			KΩ
Vdet1	Primary detection voltage	V54 – ChN, (n=0~7) @Rdet=25KΩ	2.8		10	V
Vdet2	Secondary detection voltage	V54 – ChN, (n=0~7) @Rdet=25KΩ	2.8		10	V
Vvalid	Valid test voltage	V54 – ChN, (n=0~7) @Rdet=25KΩ	2.8		10	V
Ishort	Short detection current	V54=ChN, (n=0~7)			5	mA
Rdet_min	Minimum accepted resistance range	@Cdet=0.15uF	15	17	19	KΩ
Rdet_max	Maximum accepted resistance range	@Cdet=0.15uF	26.5	29	33	KΩ
Rdet_open	Open circuit resistance	Rdet @Cdet=0.15uF	100			KΩ
Cdet_good	Accepted capacitance range	@Rdet=25KΩ	0		3	uF
Cdet_bad	Rejected capacitance range	@Rdet=25KΩ	10			uF
Tdet	Detection timing	Time to complete detection		235	500	ms
Tdet2det	Detection to detection time	@Rdet=25KΩ, Cdet=0.15uF		181	400	ms
Classification Specifications						
Vclass	Classification voltage	V54 – ChN, (n=0~7) @0mA≦Iclass≦50mA	15.5	19.3	20.5	V
Vmark	Mark voltage	V54 – ChN, (n=0~7) @0mA≦Imark≦10mA	7	9.0	10	V
Iclasslim	Classification current limitation	V54=ChN, (n=0~7)	51		100	mA
Imarklim	Mark current limitation	V54=ChN, (n=0~7)	5		100	mA
Iclass	Classification current	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
Treset	Classification reset timing	Classification reset for class probe	15	20		ms

Tclass	Classification time	Class event Class measurement timing	6			ms
Tclass_lce	Long class event time	LCE Class measurement timing	Tclass		75	ms
Tlce	Classification event1 time	Long first class event timing	88		105	ms
Tclass_acs	Classification event1 time with autoclass	Autoclass Class measurement timing	88			ms
Tce	Classification event2~5 time	Second through fifth class event timing	6		20	ms
Tme	Mark event time	Mark event timing (except last mark event)	6	10	12	ms
Tlme	Last mark event time	Last mark event timing	6	10		ms
Tpon	Power turn on time	Finish detection to turn on power to port			400	ms
Trise	Turn on rise time	From 10 % to 90 % of the voltage difference from the beginning of power up	0.015			ms
Toff	Turn off time	From VChN to V54-2.8V			500	ms
Inrush Specifications						
Iinrush	Total limit current of both pairs during power up	Single signature PD Class0-4	400	425	450	mA
		Single signature PD Class5-6	400	425	900	
		Single signature PD Class7-8	800	850	900	
Iinrush_2p	Per pairset limit current during power up	Single signature PD Class0-4		222.5	450	mA
		Single signature PD Class5-6		425	450	
		Single signature PD Class7-8		425	600	
		Dual signature PD Class0-5	400	425	450	
Tinrush	Inrush time	Inrush time	50	62.5	75	ms
Overload Specifications						
Icut	Overload power limitation per port (Power input=V54)	Class0		185		mA
		Class1		51		
		Class2		94		
		Class3		185		
		Class4		388		
		Class5		478		
		Class6		638		
		Class7		754		
		Class8		927		
100W Pcut	100W limitation (Power input=V54)	IEEE802.3bt Type4 standard		96	100	W
Tcut	Overload Time	Iport > Icut @Type1-4	50	62.5	75	ms
Short Circuit Specifications						
Ilim	Output current limitation per pairset at short circuit condition single signature	Class0 to 3	200	484		mA
		Class4	397	851		
		Class5	580	851		
		Class6	720	851		
		Class7	850	1065		
		Class8	1005	1162		
	Output current limitation per pairset at short circuit condition dual signature	Class0 to 3	400	484		mA
		Class4	684	851		
		Class5	990	1162		
Tlim	Output current time at short circuit condition	Type1	50	62.5	75	ms
		Type2	10	32.25	75	
		Type3	10	16	75	
		Type4	6	10	75	
Ted	Error delay time	Error shutdown to next detection time	750			ms

DC Disconnect						
Ihold_sig	DC MPS current bt single signature	Single signature PD Class0-4, 4pair	4	6	9	mA
		Single signature PD Class5-8, 4pair	4	6	14	
Ihold_dual	DC MPS current bt dual signature	Dual signature PD @ per port	2	3	7	mA
Tmpdo	MPS dropout time	PD MPS dropout time limitation	320	340	400	ms
Tmps	Valid MPS time	Accepted MPS duration time from PD	6			ms
Voltage Bad to GND						
Voltage bad to GND	Voltage of ChN to GND too large	For all class		33.5		V
Tvbtg	Voltage bad to GND Time	For all class	10	31.25	40	ms
Autoclass Specifications						
Tauto_pse1	Autoclass power measurement start	@PD provide the maximum power during measurement	1400		1600	ms
Tauto_pse2	Autoclass power measurement end	@PD provide the maximum power during measurement	3100		3500	ms
Pac_margin	Autoclass power margin	Class0 to 4	0.5	2		W
		Class5 to 6	0.75	2		
		Class7 to 8	1.5	2		
Temperature Sensor						
Thermal shutdown	Internal temperature for thermal shutdown			170		℃
Thermal shutdown hysteresis	Internal temperature for release thermal shutdown			130		℃
IV Accuracy						
Vport	Voltage Read Accuracy	Supply Voltage	-2		2	%
Iport	Current Read Accuracy	ChxN Current = 50 mA	-3		3	mA
		ChxN Current = 200 mA	-2		2	%
		ChxN Current = 800 mA	-2		2	

	Type4									
	Type3									
	Type1		Type2							
PD Assign Classification	Event1		Event2		Event3		Event4		Event5	
	Class	Power(W)	Class	Power(W)	Class	Power(W)	Class	Power(W)	Class	Power(W)
Class0	0	15.4								
Class1	1	4								
Class2	2	7								
Class3	3	15.4								
Class4	4	15.4	4	30	4	30				
Class5	4	15.4	4	30	0	30	0	45		
Class6	4	15.4	4	30	1	30	1	60		
Class7	4	15.4	4	30	2	30	2	60	2	75
Class8	4	15.4	4	30	3	30	3	60	3	90

Table 7 IEEE 802.3bt single signature classification event flow

	Type4							
	Type3							
	Type1		Type2					
PD Assign Classification	Event1		Event2		Event3		Event4	
	Class	Power(W)	Class	Power(W)	Class	Power(W)	Class	Power(W)
Class0	0	15.4						
Class1D	1	4	1	4	0 1(Type1)	4		
Class2D	2	7	2	7	0 2(Type1)	7		
Class3D	3	15.4	3	15.4	0 3(Type1)	15.4		
Class4D	4	15.4	4	30	0 4(Type2)	30		
Class5D	4	15.4	4	30	3	30	3	45

Table 8 IEEE 802.3bt dual signature classification event flow

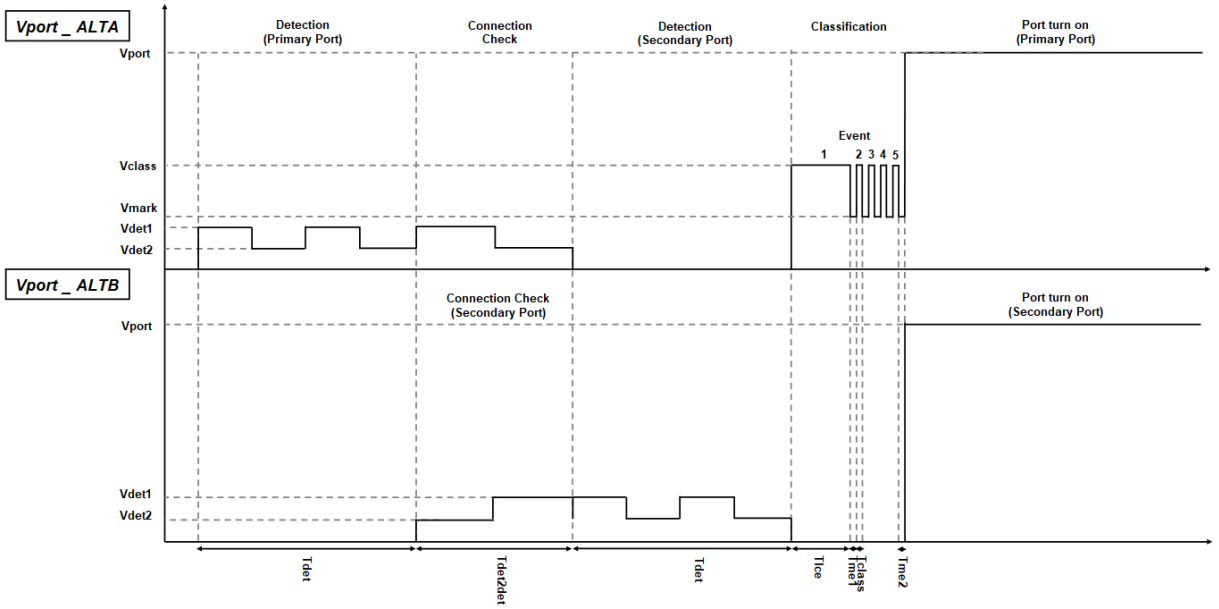


Figure 9 4 pair single signature class8 power sequence

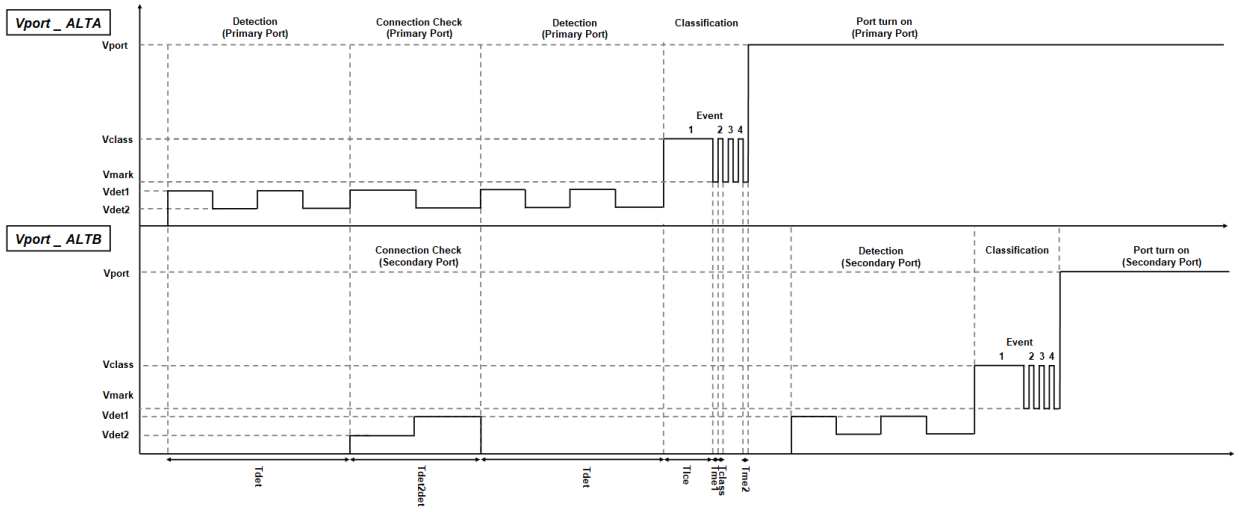


Figure 10 4 pair dual signature class5 power sequence

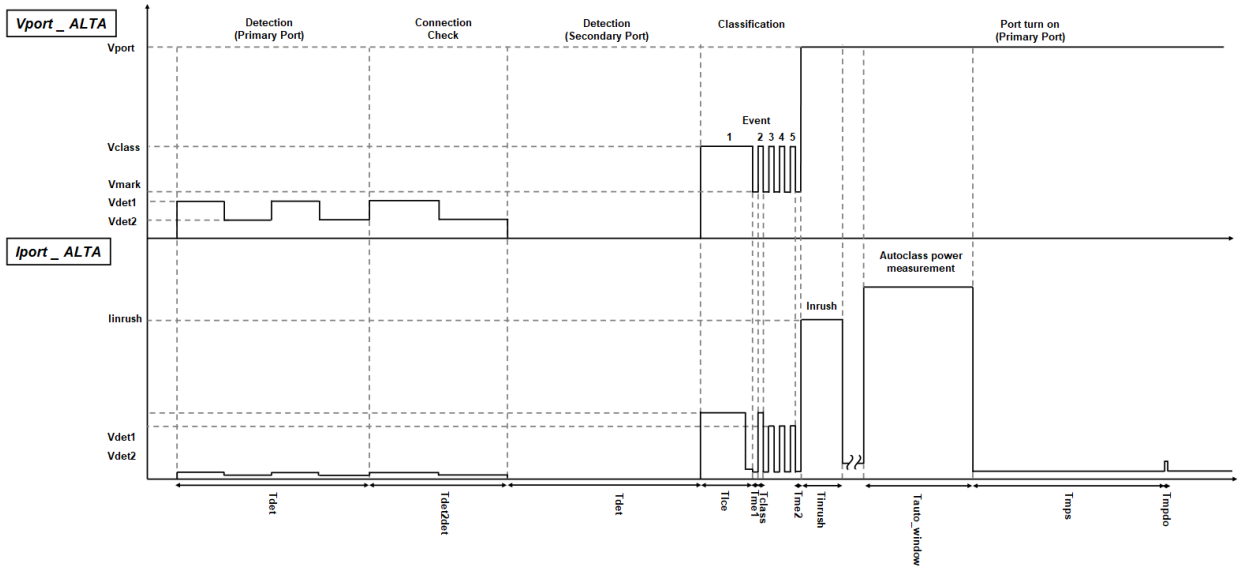


Figure 11 4 pair single signature class8 power sequence with autoclass, MPS

7.5 Digital Electrical Characteristics

Table 9 Digital Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I^2C & EEPROM interface						
Tscl	SCL/EE_CLK input	I^2C input clock		800		KHz
Tee	SCL/EE_CLK output	Output clock for EEPROM		62.5		KHz
T_{SCLH}	SCL high period		625			ns
T_{SCLL}	SCL low period		625			ns
T_{IDLE}	Idle time	from SDAI ↑ to SDAI ↓, when SCL =1. SCL and SDAI should keep at logic high during T_{IDLE}.	750			ns
T_{START}	Start bit time	from SDAI ↓ to SCL ↓ SCL should keep at logic high during T_{START}	500			ns
T_{STOP}	Stop bit time	from SCL ↑ to SDAI ↑ SCL should keep at logic high during T_{STOP}	500			ns
T_{SDAOO}	SDAO output delay	from SCL ↓ to SDAO output	125		350	ns
T_{SDAI}	SDAI input setup time	from SDAI ↑ to SCL ↑	50			ns
T_{SDAIH}	SDAI input hold time	from SCL ↓ to SDAI invalid	50			ns
T_{TO}	Time out time	IP8008 will abort the I2C cycle, if SCL is idle for longer than $T_{TO.}$			7	ms
VIL	Input low voltage	AD0~AD3 & I2C			0.8	V
VIH	Input high voltage	AD0~AD3 & I2C	2.2			V
VOL	Open drain output low voltage	SCL/EE_CLK,SDAI/EE_DAT@auto mode @ Isink =5mA			0.7	V
VOL	Open drain output low voltage	SDAO,INTB,LED_CLK,LED_DAT @ Isink =5mA			0.7	V

7.6 AC Timing

7.6.1 Power On Sequence and Reset Timing

Description	Min.	Typ.	Max.	Unit
V54_Power on time@ V54 rising time from 0V to 57V		100	-	ms
V54 stable to RstN release	100			ms
Reset to System up time	100			ms

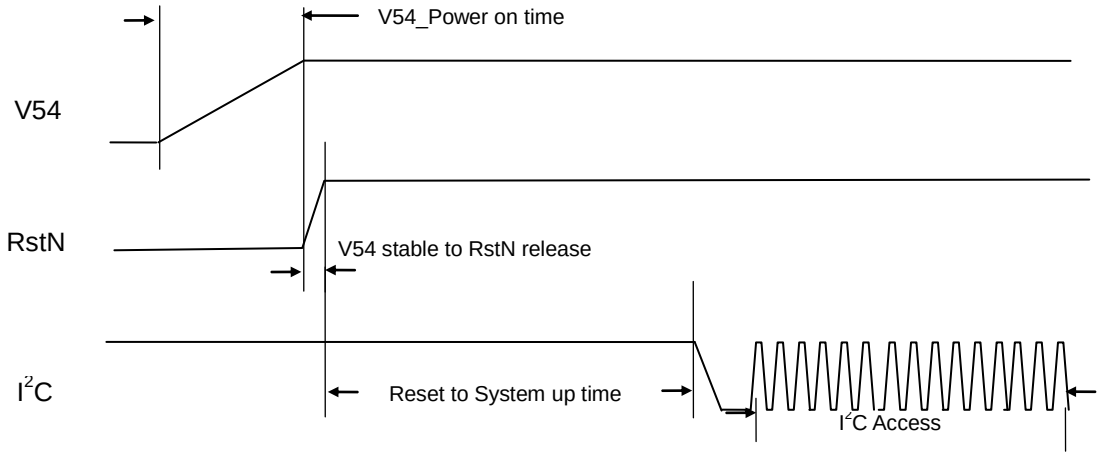


Figure 12 Power on sequence and reset timing diagram

7.6.2 EEPROM Timing

7.6.2.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	16000	-	ns
T_{sSCL}	SDA to SCL setup time	250	-	-	ns
T_{hSCL}	SDA to SCL hold time	250	-	-	ns

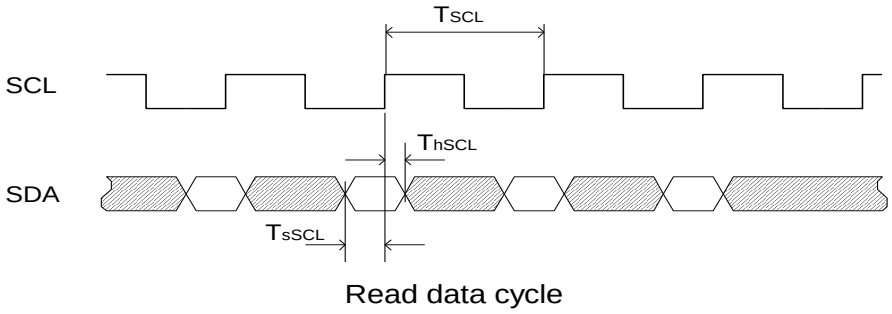


Figure 13 EEPROM read cycle timing diagram

7.6.2.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	16000	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	400	ns

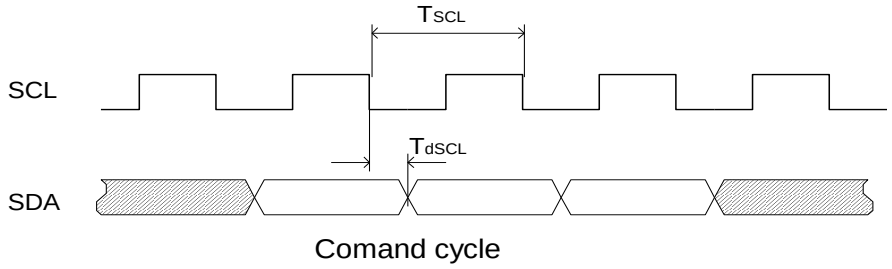


Figure 14 EEPROM wirte cycle timing diagram

7.6.3 I²C Command Cycle Timing Diagram

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	I²C clock period		1250	-	ns
T_{SCLH}	SCL high period	625	-		ns
T_{SCLL}	SCL low period	625			ns
T_{IDLE}	Idle time: from SDAI ↑ to SDAI ↓, when SCL =1. SCL and SDAI should keep at logic high during T_{IDLE}.	750			ns
T_{START}	Start bit time: from SDAI ↓ to SCL ↓ SCL should keep at logic high during T_{START}.	500			ns
T_{STOP}	Stop bit time: from SCL ↑ to SDAI ↑ SCL should keep at logic high during T_{STOP}.	500			ns
T_{SDAOO}	IP8008 SDAO output delay: from SCL ↓ to SDAO output	125		350	ns
T_{SDAI}	SDAI input setup time: from SDAI ↑ to SCL ↑	50			ns
T_{SDAIH}	SDAI input hold time: from SCL ↓ to SDAI invalid	50			ns
T_{TO}	Time out time: IP8008 will abort the I2C cycle, if SCL is idle for longer than T_{TO}.			7	ms
V_{IH}	Input high threshold voltage of SCL and SDAI	2.2			V
V_{IL}	Input low threshold voltage of SCL and SDAI			0.8	V

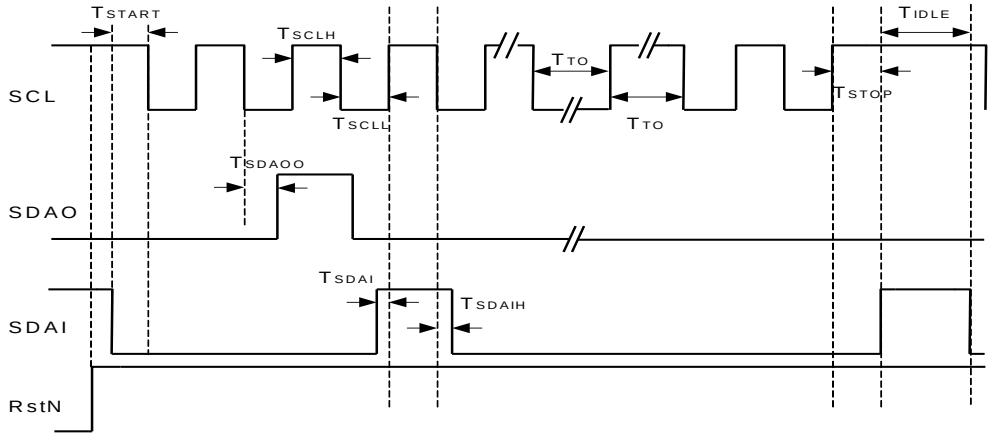


Figure 15 I²C Command Cycle Timing Diagram

7.7 Thermal Data

	θ_{JA}	θ_{JC}	Ψ_{JT}	Conditions	Units
Theta 4L	24.8	14.2	0.7	4 Layer PCB	°C/W
Theta 2L	55.0	26.5	1.7	2 Layer PCB	

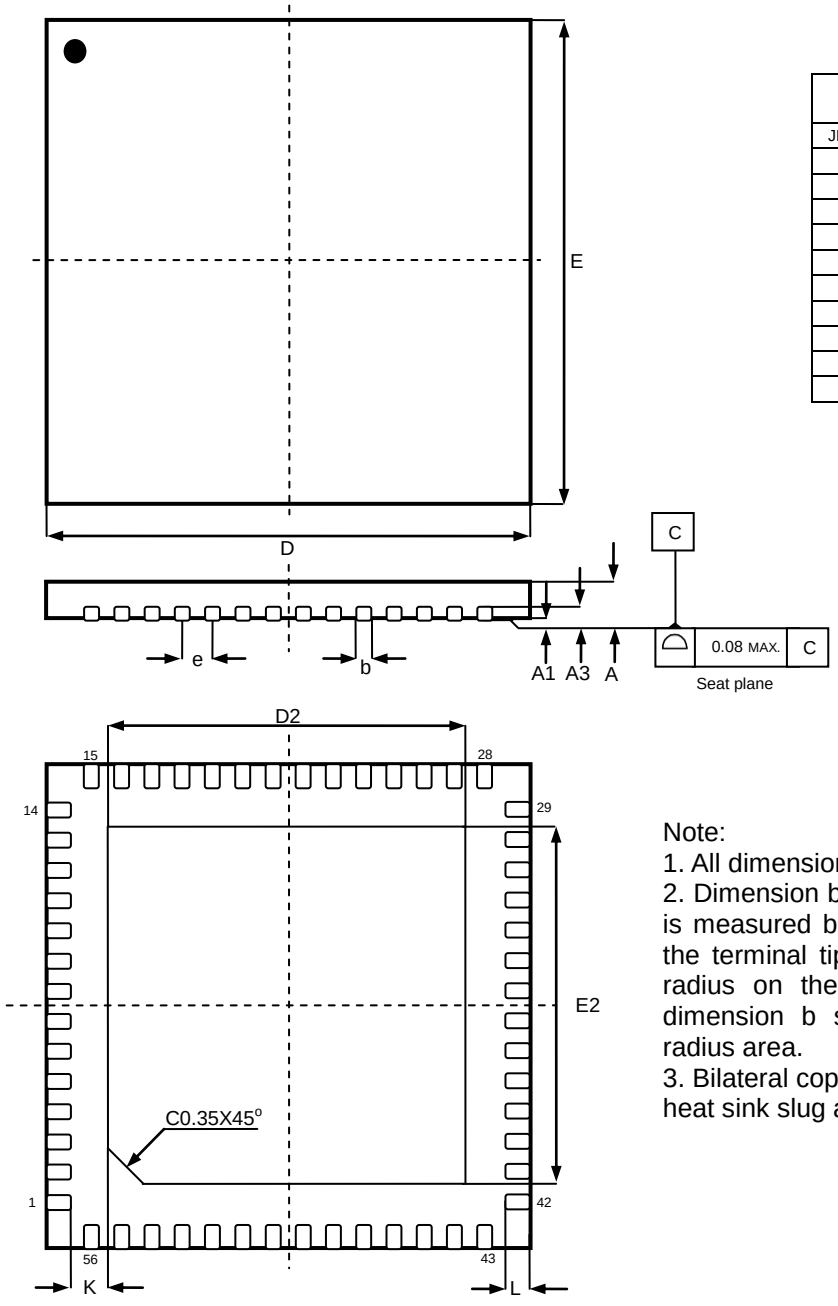
8 Order Information

Table 10 Order Information

Part No.	Package	Operating Temperature	Notice
IP8008	56-Lead QFN	-40°C to 85°C	

9 Package Detail

9.1 56 QFN Outline Dimensions (mm)



	PACKAGE TYPE		
JED OUTLINE	MO-220		
PKG CODE	WQFN(Y856)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	8.00 BSC		
E	8.00 BSC		
e	0.50 BSC		
K	0.20	-	-

Note:
1. All dimensions are in milimeters.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm frim the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the expose heat sink slug as well as the terminals.

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
240X24* MIL	5.85	5.90	5.95	5.85	5.90	5.95	0.30	0.40	0.50	V	X	(W)VLLD-5

Figure 16 Package outline dimensions

9.2 PCB foortprint (mm)

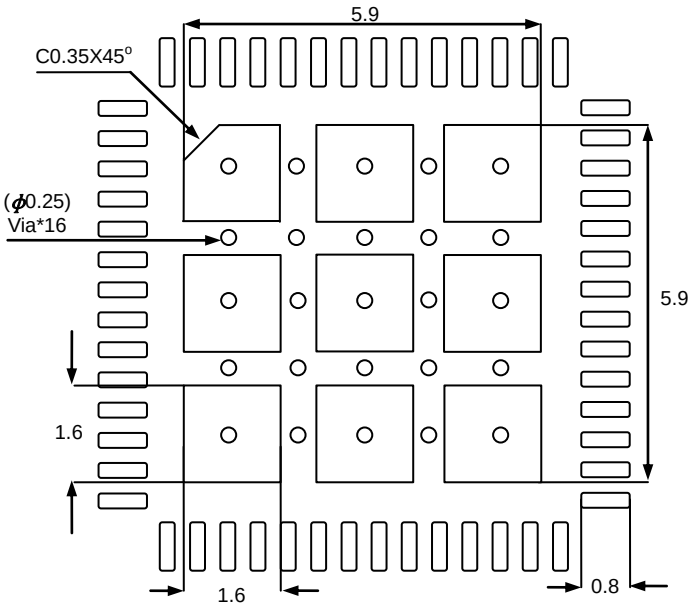


Figure 17 PCB footprint

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